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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082ahh020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

Zilog's Z8 Encore! MCU family of products are the first in a line of Zilog microcontroller products based upon the 8-bit eZ8 CPU. Zilog's Z8 Encore! XP F082A Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8 instructions. The rich peripheral set of the Z8 Encore! XP F082A Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices and sensors.

Features

The key features of Z8 Encore! XP F082A Series products include:

- 20 MHz eZ8 CPU
- 1KB, 2KB, 4KB, or 8KB Flash memory with in-circuit programming capability
- 256B, 512B, or 1KB register RAM
- Up to 128B nonvolatile data storage (NVDS)
- Internal precision oscillator trimmed to $\pm 1\%$ accuracy
- External crystal oscillator, operating up to 20MHz
- Optional 8-channel, 10-bit analog-to-digital converter (ADC)
- Optional on-chip temperature sensor
- On-chip analog comparator
- Optional on-chip low-power operational amplifier (LPO)
- Full-duplex UART
- The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared Data Association (IrDA)-compliant infrared encoder/decoders, integrated with the UART
- Two enhanced 16-bit timers with capture, compare and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- Up to 20 vectored interrupts
- 6 to 25 I/O pins depending upon package
- Up to thirteen 5 V-tolerant input pins

operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT modes.

General-Purpose Input/Output

The Product Line MCUs feature 6 to 25 port pins (Ports A–D) for general- purpose input/ output (GPIO). The number of GPIO pins available is a function of package and each pin is individually programmable. 5 V tolerant input pins are available on all I/Os on 8-pin devices and most I/Os on other package types.

Direct LED Drive

The 20- and 28-pin devices support controlled current sinking output pins capable of driving LEDs without the need for a current limiting resistor. These LED drivers are independently programmable to four different intensity levels.

Flash Controller

The Flash Controller programs and erases Flash memory. The Flash Controller supports several protection mechanisms against accidental program and erasure, plus factory serialization and read protection.

Non-Volatile Data Storage

The nonvolatile data storage (NVDS) uses a hybrid hardware/software scheme to implement a byte programmable data memory and is capable of over 100,000 write cycles.

Note: Devices with 8KB of Flash memory do not include the NVDS feature.

Interrupt Controller

The Z8 Encore! XP F082A Series products support up to 20 interrupts. These interrupts consist of 8 internal peripheral interrupts and 12 general-purpose I/O pin interrupt sources. The interrupts have three levels of programmable interrupt priority.

Reset Controller

The Z8 Encore! XP F082A Series products can be reset using the RESET pin, Power-On Reset, Watchdog Timer (WDT) time-out, STOP Mode exit, or Voltage Brown-Out (VBO)

Signal Mnemonic	I/O	Description
Analog		
ANA[7:0]	Ι	Analog Port. These signals are used as inputs to the analog-to-digital converter (ADC).
VREF	I/O	Analog-to-digital converter reference voltage input, or buffered output for internal reference.
Low-Power Operati	ional Ar	nplifier (LPO)
AMPINP/AMPINN	Ι	LPO inputs. If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	0	LPO output. If enabled, this pin is driven by the on-chip LPO.
Oscillators		
XIN	I	External Crystal Input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the X_{OUT} pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X _{OUT}	0	External Crystal Output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the XIN pin to form the oscillator.
Clock Input		
CLKIN	Ι	Clock Input Signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger.
		Caution: The DBG pin is open-drain and requires a pull-up resistor to ensure proper operation.
Notes: 1. PB6 and PB7 are	only ava	ensure proper operation.

Table 2. Signal Descriptions (Continued)

replaced by AV_{DD} and AV_{SS} . 2. The AV_{DD} and AV_{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Program Memory Address (Hex)	Function
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-03FF	Program Memory
Note: *See Table 32 on page 56 for a list of	the interrupt vectors.

Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 6 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

Table 6. Z8 Encore! XP F082A Series Flash Memory Information Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog Option Bits/Calibration Data
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FFH
FE54–FE5F	Reserved
FE60–FE7F	Zilog Calibration Data
FE80–FFFF	Reserved



Figure 5. Power-On Reset Operation

Voltage Brown-Out Reset

The devices in the Z8 Encore! XP F082A Series provide low Voltage Brown-Out (VBO) protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold (V_{POR}), the VBO block holds the device in the Reset.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the device progresses through a full System Reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1. Figure 6 displays Voltage Brown-Out operation. See the <u>Electrical</u> <u>Characteristics</u> chapter on page 226 for the VBO and POR threshold voltages (V_{VBO} and V_{POR}).

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operation during STOP Mode is set by the VBO_AO Flash option bit. See the <u>Flash</u> <u>Option Bits</u> chapter on page 159 for information about configuring VBO_AO.

General-Purpose Input/Output

The Z8 Encore! XP F082A Series products support a maximum of 25 port pins (Ports A–D) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

GPIO Port Availability By Device

Table 14 lists the port pins available with each device and package type.

Devices	Package	ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F082ASB, Z8F082APB, Z8F082AQB Z8F042ASB, Z8F042APB, Z8F042AQB Z8F022ASB, Z8F022APB, Z8F022AQB Z8F012ASB, Z8F012APB, Z8F012AQB	8-pin	Yes	[5:0]	No	No	No	6
Z8F081ASB, Z8F081APB, Z8F081AQB Z8F041ASB, Z8F041APB, Z8F041AQB Z8F021ASB, Z8F021APB, Z8F021AQB Z8F011ASB, Z8F011APB, Z8F011AQB	8-pin	No	[5:0]	No	No	No	6
Z8F082APH, Z8F082AHH, Z8F082ASH Z8F042APH, Z8F042AHH, Z8F042ASH Z8F022APH, Z8F022AHH, Z8F022ASH Z8F012APH, Z8F012AHH, Z8F012ASH	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F081APH, Z8F081AHH, Z8F081ASH Z8F041APH, Z8F041AHH, Z8F041ASH Z8F021APH, Z8F021AHH, Z8F021ASH Z8F011APH, Z8F011AHH, Z8F011ASH	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F082APJ, Z8F082ASJ, Z8F082AHJ Z8F042APJ, Z8F042ASJ, Z8F042AHJ Z8F022APJ, Z8F022ASJ, Z8F022AHJ Z8F012APJ, Z8F012ASJ, Z8F012AHJ	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F081APJ, Z8F081ASJ, Z8F081AHJ Z8F041APJ, Z8F041ASJ, Z8F041AHJ Z8F021APJ, Z8F021ASJ, Z8F021AHJ Z8F011APJ, Z8F011ASJ, Z8F011AHJ	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25

Table 14. Port Availability by Device and Package Type

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Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port A ^{1,2}	PA0	T0IN/T0OUT	Timer 0 Input/Timer 0 Output Complement	N/A
		Reserved		-
	PA1	TOOUT	Timer 0 Output	-
		Reserved		-
	PA2	DE0	UART 0 Driver Enable	-
		Reserved		-
	PA3	CTS0	UART 0 Clear to Send	-
		Reserved		-
	PA4	RXD0/IRRX0	UART 0/IrDA 0 Receive Data	-
		Reserved		-
	PA5	TXD0/IRTX0	UART 0/IrDA 0 Transmit Data	-
		Reserved		-
	PA6	T1IN/T1OUT	Timer 1 Input/Timer 1 Output Complement	-
		Reserved		-
	PA7	T1OUT	Timer 1 Output	-
		Reserved		-

Table 15. Port Alternate Function Mapping (Non 8-Pin Parts)

Notes:

- Because there is only a single alternate function for each Port A pin, the Alternate Function Set registers are not implemented for Port A. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 2. Whether PA0/PA6 takes on the timer input or timer output complement function depends on the timer configuration. See the <u>Timer Pin Signal Operation</u> section on page 84 for details.
- Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the Port <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- 4. V_{REF} is available on PB5 in 28-pin products and on PC2 in 20-pin parts.
- Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set Register AFS2 is not used to select the function. Alternate function selection must also be enabled. See the Port <u>A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.
- Because there is only a single alternate function for the Port PD0 pin, the Alternate Function Set registers are not implemented for Port D. Enabling alternate function selections automatically enables the associated alternate function. See the <u>Port A–D Alternate Function Subregisters (PxAF)</u> section on page 47 for details.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Select Register AFS1	Alternate Function Select Register AFS2
Port A	PA0	TOIN	Timer 0 Input	AFS1[0]: 0	AFS2[0]: 0
		Reserved		AFS1[0]: 0	AFS2[0]: 1
		Reserved		AFS1[0]: 1	AFS2[0]: 0
		TOOUT	Timer 0 Output Complement	AFS1[0]: 1	AFS2[0]: 1
	PA1	TOOUT	Timer 0 Output	AFS1[1]: 0	AFS2[1]: 0
		Reserved		AFS1[1]: 0	AFS2[1]: 1
		CLKIN	External Clock Input	AFS1[1]: 1	AFS2[1]: 0
		Analog Functions ¹	ADC Analog Input/V _{REF}	AFS1[1]: 1	AFS2[1]: 1
	PA2	DE0	UART 0 Driver Enable	AFS1[2]: 0	AFS2[2]: 0
		RESET	External Reset	AFS1[2]: 0	AFS2[2]: 1
		T1OUT	Timer 1 Output	AFS1[2]: 1	AFS2[2]: 0
		Reserved		AFS1[2]: 1	AFS2[2]: 1
	PA3	CTS0	UART 0 Clear to Send	AFS1[3]: 0	AFS2[3]: 0
		COUT	Comparator Output	AFS1[3]: 0	AFS2[3]: 1
		T1IN	Timer 1 Input	AFS1[3]: 1	AFS2[3]: 0
		Analog Functions ²	ADC Analog Input/LPO Input (P)	AFS1[3]: 1	AFS2[3]: 1
	PA4	RXD0	UART 0 Receive Data	AFS1[4]: 0	AFS2[4]: 0
		Reserved		AFS1[4]: 0	AFS2[4]: 1
		Reserved		AFS1[4]: 1	AFS2[4]: 0
		Analog Functions ²	ADC/Comparator Input (N)/LPO Input (N)	AFS1[4]: 1	AFS2[4]: 1
	PA5	TXD0	UART 0 Transmit Data	AFS1[5]: 0	AFS2[5]: 0
		T1OUT	Timer 1 Output Complement	AFS1[5]: 0	AFS2[5]: 1
		Reserved		AFS1[5]: 1	AFS2[5]: 0
		Analog Functions ²	ADC/Comparator Input (P) LPO Output	AFS1[5]: 1	AFS2[5]: 1

Table 16. Port Alternate Function Mapping (8-Pin Parts)

Notes:

1. Analog functions include ADC inputs, ADC reference, comparator inputs and LPO ports.

2. The alternate function selection must be enabled; see the Port A–D Alternate Function Subregisters (PxAF) section on page 47 for details.

Port A–D Address Registers

The Port A–D Address registers select the GPIO port functionality accessible through the Port A–D Control registers. The Port A–D Address and Control registers combine to provide access to all GPIO port controls; see Tables 18 and 19.

Bit	7	6	5	4	3	2	1	0
Field				PADD	R[7:0]			
RESET				00)H			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address			FI	D0H, FD4H,	FD8H, FDC	Ή		

Table 18. Port A–D GPIO Address Registers (PxADDR)

Bit	Description
[7:0]	Port Address
PADDRx	The Port Address selects one of the subregisters accessible through the Port Control Register.
Note: x inc	dicates the specific GPIO port pin number (7–0).

Table 19. Port A–D GPIO Address Registers by Bit Description

PADDR[7:0]	Port Control Subregister accessible using the Port A–D Control Registers
00H	No function. Provides some protection against accidental port reconfiguration.
01H	Data Direction.
02H	Alternate Function.
03H	Output Control (Open-Drain).
04H	High Drive Enable.
05H	Stop Mode Recovery Source Enable.
06H	Pull-up Enable.
07H	Alternate Function Set 1.
08H	Alternate Function Set 2.
09H–FFH	No function.

enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Observe the following steps for configuring a timer for COUNTER Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer.
 - Configure the timer for COUNTER Mode.
 - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER Mode. After the first timer Reload in COUNTER Mode, counting always begins at the reset value of 0001H. In COUNTER Mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control Register to enable the timer.

In COUNTER Mode, the number of Timer Input transitions since the timer start is computed via the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value-Start Value

COMPARATOR COUNTER Mode

In COMPARATOR COUNTER Mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPAR-ATOR COUNTER Mode, the prescaler is disabled.

- Set the Capture edge (rising or falling) for the Timer Input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control Register to enable the timer.
- 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte Register are placed in a holding register. A subsequent read from the Timer Low Byte Register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte Register returns the actual value in the counter.

Timer Pin Signal Operation

The timer output function is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

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Table 63. UART Control 0 Register (U0CTL0)

Bit	7	6	5	4	3	2	1	0				
Field	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN				
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	F42H											
D:4												
BI												
TEN	This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is Low and the CTSE bit is 1, the transmitter is enabled. 0 = Transmitter disabled. 1 = Transmitter enabled.											
[6] REN	Receive Enable This bit enables or disables the receiver. 0 = Receiver disabled. 1 = Receiver enabled.											
[5] CTSE	CTS Enabl 0 = The CT 1 = The UA	<u>e</u> S signal has RT recogniz	s no eff <u>ect o</u> tes the CTS	n the transm signal as ar	nitter. n enable cor	ntrol from the	e transmitter					
[4] PEN	 Parity Enable This bit enables or disables parity. Even or odd is determined by the PSEL bit. 0 = Parity is disabled. 1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit 											
[3] PSEL	Parity Select 0 = Even parity is transmitted and expected on all received data. 1 = Odd parity is transmitted and expected on all received data.											
[2] SBRK	Send Break This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. 0 = No break is sent. 1 = Forces a break condition by setting the output of the transmitter to zero.											
[1] STOP	Stop Bit Se 0 = The trai 1 = The trai	e lect nsmitter sen nsmitter sen	ds one stop ds two stop	bit. bits.								
[0] LBEN	Loop Back Enable 0 = Normal operation. 1 = All transmitted data is looped back to the receiver.											

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the infrared endec. The infrared endec data rate is calculated using the following equation:

Infrared Data Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16 clocks wide. If the data to be transmitted is 1, the IR_TXD signal remains low for the full 16 clock period. If the data to be transmitted is 0, the transmitter first outputs a 7 clock low period, followed by a 3 clock high pulse. Finally, a 6 clock low pulse is output to complete the full 16 clock data period. Figure 17 displays IrDA data transmission. When the infrared endec is enabled, the UART's TXD signal is internal to the Z8 Encore! XP F082A Series products while the IR_TXD signal is output through the TXD pin.



Figure 17. Infrared Data Transmission

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

SINGLE-ENDED Mode:

0000 = ANA0 (transimpedance amp output when enabled) 0001 = ANA1 (transimpedance amp inverting input) 0010 = ANA2 (transimpedance amp noninverting input) 0011 = ANA3 0100 = ANA4 0101 = ANA5 0110 = ANA6 0111 = ANA7 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Hold transimpedance input nodes (ANA1 and ANA2) to ground. 1101 = Reserved 1110 = Temperature Sensor.

1111 = Reserved.

DIFFERENTIAL Mode (noninverting input and inverting input respectively):

- 0000 = ANA0 and ANA1 0001 = ANA2 and ANA3 0010 = ANA4 and ANA5 0011 = ANA4 and ANA5 0011 = ANA1 and ANA0 0100 = ANA3 and ANA2 0101 = ANA5 and ANA4 0110 = ANA6 and ANA5 0111 = ANA0 and ANA5 1001 = ANA0 and ANA3 1001 = ANA0 and ANA4 1010 = ANA0 and ANA5 1011 = Reserved 1100 = Reserved 1101 = Reserved 1101 = Reserved1110 = Reserved
- 1111 = Manual Offset Calibration Mode

ADC Control/Status Register 1

The ADC Control/Status Register 1 (ADCCTL1) configures the input buffer stage, enables the threshold interrupts and contains the status of both threshold triggers. It is also used to select the voltage reference configuration.

Bit	Description (Continued)
[5:2] REFLVL	Internal Reference Voltage LevelThis reference is independent of the ADC voltage reference. Note: 8-pin devices contain twoadditional LSBs for increased resolution.For 20-/28-pin devices:0000 = $0.0 \vee$ 0001 = $0.2 \vee$ 0010 = $0.4 \vee$ 0011 = $0.6 \vee$ 0100 = $0.8 \vee$ 0101 = $1.0 \vee$ (Default)0111 = $1.4 \vee$ 1000 = $1.6 \vee$ 10101 = $1.8 \vee$
	1010–1111 = Reserved

Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0×1000) . At the return from the sub-routine, the read byte resides in working register R0 and the read status byte resides in working register R1. The contents of the status byte are undefined for read operations to illegal addresses. Also, the user code must pop the address byte off the stack.

The read routine uses 9 bytes of stack space in addition to the one byte of address pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between 44 μ s and 489 μ s (assuming a 20MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return 0xff. Illegal read operations have a 2 μ s execution time.

The status byte returned by the NVDS read routine is zero for successful read, as determined by a CRC check. If the status byte is nonzero, there was a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have a CRC error.

Power Failure Protection

The NVDS routines employ error checking mechanisms to ensure a power failure endangers only the most recently written byte. Bytes previously written to the array are not perturbed.

A system reset (such as a pin reset or Watchdog Timer reset) that occurs during a write operation also perturbs the byte currently being written. All other bytes in the array are unperturbed.

Optimizing NVDS Memory Usage for Execution Speed

NVDS read time can vary drastically. This discrepancy is a trade-off for minimizing the frequency of writes that require post-write page erases, as indicated in Table 107. The NVDS read time of address N is a function of the number of writes to addresses other than N since the most recent write to address N, plus the number of writes since the most recent page erase. Neglecting effects caused by page erases and results caused by the initial condition in which the NVDS is blank, a rule of thumb is that every write since the most recent page erase causes read times of unwritten addresses to increase by 1 µs up to a maximum of (511-NVDS_SIZE)µs.

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Assembly		Add Mo	ress ode	Oncode(s)	Flags						Fetch	Instr. Cycle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	V	D	Н	S	S
SUB dst, src	$dst \gets dst - src$	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23	-						2	4
		R	R	24	-						3	3
		R	IR	25	-						3	4
		R	IM	26	-						3	3
		IR	IM	27	-						3	4
SUBX dst, src	$dst \leftarrow dst - src$	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29	-						4	3
SWAP dst	$dst[7:4] \leftrightarrow dst[3:0]$	R		F0	Х	*	*	Х	-	_	2	2
		IR		F1	-						2	3
TCM dst, src	(NOT dst) AND src	r	r	62	-	*	*	0	_	_	2	3
		r	Ir	63	-						2	4
		R	R	64	-						3	3
		R	IR	65	-						3	4
		R	IM	66	-						3	3
		IR	IM	67	-						3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	_	*	*	0	_	_	4	3
		ER	IM	69	-						4	3
TM dst, src	dst AND src	r	r	72	-	*	*	0	_	-	2	3
		r	Ir	73	-						2	4
		R	R	74	-						3	3
		R	IR	75	-						3	4
		R	IM	76	-						3	3
		IR	IM	77	-						3	4

Table 128. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 =Set to 1.

UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.



Figure 3	37. U	ART	Timing	With	CTS
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		Delay (ns)					
Parameter	Abbreviation	Minimum	Maximum				
UART							
T ₁	CTS Fall to DE output delay	2 * X _{IN} period	2 * X _{IN} period + 1 bit time				
T ₂	DE assertion to TXD falling edge (start bit) delay	±	: 5				
T ₃	End of Stop Bit(s) to DE deassertion delay	± 5					

Tahla	1/6	IIART	Timina	With	CTS
lable	140.	UARI	runng	VVILII	613

Part Number	Flash	RAM	SDVN	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 8KB Flash											
Standard Temperatu	re: 0°C 1	to 70°C									
Z8F081APB020SG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020SG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020SG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020SG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperatu	ıre: –40°	°C to 10	5°C								
Z8F081APB020EG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020EG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020EG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020EG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package

Table 148. Z8 Encore! XP F082A Series Ordering Matrix