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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082ahh020sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Chapter/Section	Description	Page No.
Dec 2012	27	Port Alternate Function Map- ping (Non 8-Pin Parts), Port Alternate Function Mapping (8- Pin Parts)	Added missing Port D data to Table 15; cor- rected active Low status (set overlines) for PA0 (TOOUT), PA2 (RESET) and PA5 (T1OUT) in Table 16.	<u>40, 43</u>
Sep 2011	26	LED Drive Enable Register	Clarified statement surrounding the Alternate Function Register as it relates to the LED function; revised Flash Sector Protect Regis- ter description; revised Packaging chapter.	<u>53,</u> <u>157,</u> <u>245</u>
Sep 2008	25	Overview, Address Space, Register Map, General-Pur- pose Input/Output, Available Packages, Ordering Informa- tion	Added references to F042A Series back in Table 1, Table 5, Table 7 and Table 14.	<u>2, 8,</u> <u>16, 18,</u> <u>36,</u> <u>246</u>
May 2008	24	Overview, Address Space, Register Map, General-Pur- pose Input/Output, Available Packages, Ordering Informa- tion	Changed title to Z8 Encore! XP F082A Series and removed references to F042A Series in Table 1, Table 5, Table 7 and Table 14.	<u>2, 8,</u> <u>16, 18,</u> <u>36,</u> <u>246</u>
Dec 2007	23	Pin Description, General-Pur- pose Input/Output, Watchdog Timer	Updated Figure 3, Table 15, Tables 60 through 62.	<u>9, 40,</u> <u>97</u>
Jul 2007	22	Electrical Characteristics	Updated Tables 16 and 132; power con- sumption data.	<u>43,</u> 229
Jun 2007	21	n/a	Revision number update.	All

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Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code.

Universal Asynchronous Receiver/Transmitter

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and

Table 4. Pin Characteristics (8-Pin Devices)								
Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
PA1	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
RESET/ PA2	I/O	I/O (defaults to RESET)	Low (in Reset mode)	Yes	Programma- ble for PA2; alw <u>ays on f</u> or RESET	Yes	Programma- ble for PA2; alw <u>ays on f</u> or RESET	Yes, unless pull-ups enabled
PA[5:3]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
V _{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
V _{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Program Memory Address (Hex)	Function				
0002–0003	Reset Vector				
0004–0005	WDT Interrupt Vector				
0006–0007	Illegal Instruction Trap				
0008–0037	Interrupt Vectors*				
0038–0039	Reserved				
003A-003D	Oscillator Fail Trap Vectors				
003E-03FF	Program Memory				
lote: *See Table 32 on page 56 for a list of the interrupt vectors.					

Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 6 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

Table 6. Z8 Encore! XP F082A Series Flash Memory Information Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog Option Bits/Calibration Data
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FFH
FE54–FE5F	Reserved
FE60–FE7F	Zilog Calibration Data
FE80–FFFF	Reserved

GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). See the <u>GPIO Mode Interrupt Controller</u> chapter on page 55 for more information about interrupts using the GPIO pins.

GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data. Table 17 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

Port Register Mnemonic	Port Register Name			
P <i>x</i> ADDR	Port A–D Address Register; selects subregisters.			
P <i>x</i> CTL	Port A–D Control Register; provides access to subregisters.			
PxIN	Port A–D Input Data Register.			
P <i>x</i> OUT	Port A–D Output Data Register.			
Port Subregister Mnemonic	Port Register Name			
PxDD	Data Direction.			
P <i>x</i> AF	Alternate Function.			
P <i>x</i> OC	Output Control (Open-Drain).			
P <i>x</i> HDE	High Drive Enable.			
P <i>x</i> SMRE	Stop Mode Recovery Source Enable.			
P <i>x</i> PUE	Pull-up Enable.			
PxAFS1	Alternate Function Set 1.			
PxAFS2	Alternate Function Set 2.			

Table 17. GPIO Port Registers and Subregisters

Interrupt Control Register

The Interrupt Control (IRQCTL) Register, shown in Table 49, contains the master enable bit for all interrupts.

Bit	7	6	5	4	3	2	1	0
Field	IRQE		Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R
Address		FCFH						
Bit	Description							
[7] IRQE	Interrupt Request Enable This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction,							

Table 49. Interrupt Control Register (IRQCTL)

Description
Interrupt Request Enable
 This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, Reset or by a direct register write of a 0 to this bit. 0 = Interrupts are disabled. 1 = Interrupts are enabled.
Reserved These bits are reserved and must be programmed to 0000000.



Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer Reload. If

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- Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control Register to enable the timer and initiate counting.

In COMPARE Mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

COMPARE Mode Time (s) = (Compare Value – Start Value) × Prescale System Clock Frequency (Hz)

GATED Mode

In GATED Mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following steps for configuring a timer for GATED Mode and initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

- 1. Checks the UART Status 0 Register to determine the source of the interrupt error, break, or received data.
- 2. Reads the data from the UART Receive Data Register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) Mode, further actions may be required depending on the MULTIPROCESSOR Mode bits MPMD[1:0].
- 3. Clears the UART Receiver interrupt in the applicable Interrupt Request Register.
- 4. Executes the IRET instruction to return from the interrupt-service routine and await more data.

Clear To Send (CTS) Operation

The CTS pin, if enabled by the CTSE bit of the UART Control 0 Register, performs flow control on the outgoing transmit datastream. The Clear To Send ($\overline{\text{CTS}}$) input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert $\overline{\text{CTS}}$ at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this action is typically performed during Stop Bit transmission. If $\overline{\text{CTS}}$ deasserts in the middle of a character transmission, the current character is sent completely.

MULTIPROCESSOR (9-bit) Mode

The UART features a MULTIPROCESSOR (9-bit) Mode that uses an extra (9th) bit for selective communication when a number of processors share a common UART bus. In MULTIPROCESSOR Mode (also referred to as *9-bit Mode*), the multiprocessor bit (MP) is transmitted immediately following the 8-bits of data and immediately preceding the Stop bit(s) as displayed in Figure 13. The character format is:



Figure 13. UART Asynchronous MULTIPROCESSOR Mode Data Format

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit Shift Register has shifted the first bit of data out. The Transmit Data Register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data Register before the Transmit Shift Register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following actions occur:

• A data byte is received and is available in the UART Receive Data Register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data Register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

Note: In MULTIPROCESSOR Mode (MPEN=1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received.
- An overrun is detected.
- A data framing error is detected.

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and must be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status

The UART data rate is calculated using the following equation:

UART Baud Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

For a given UART data rate, calculate the integer baud rate divisor value using the following equation:

UART Baud Rate Divisor Value (BRG) = Round $\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$

The baud rate error relative to the acceptable baud rate is calculated using the following equation:

UART Baud Rate Error (%) = $100 \times \left(\frac{\text{Actual Data Rate} - \text{Desired Data Rate}}{\text{Desired Data Rate}}\right)$

For reliable communication, the UART baud rate error must never exceed 5 percent. Table 72 provides information about the data rate errors for popular baud rates and commonly used crystal oscillator frequencies.

10.0MHz System Clock				5.	5296MHz Sys	tem Clock	
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	1	625.0	0.00	625.0	N/A	N/A	N/A
250.0	3	208.33	-16.67	250.0	1	345.6	38.24
115.2	5	125.0	8.51	115.2	3	115.2	0.00
57.6	11	56.8	-1.36	57.6	6	57.6	0.00
38.4	16	39.1	1.73	38.4	9	38.4	0.00
19.2	33	18.9	0.16	19.2	18	19.2	0.00
9.60	65	9.62	0.16	9.60	36	9.60	0.00
4.80	130	4.81	0.16	4.80	72	4.80	0.00
2.40	260	2.40	-0.03	2.40	144	2.40	0.00
1.20	521	1.20	-0.03	1.20	288	1.20	0.00
0.60	1042	0.60	-0.03	0.60	576	0.60	0.00
0.30	2083	0.30	0.2	0.30	1152	0.30	0.00
					0.400 MUL 0		

Table 72. UART Baud Rates

3.579545 MHz System Clock

1.8432MHz System Clock

#3	#3	#3	#3

4. Round the result and discard the least significant two bytes (equivalent to dividing by 2^{16}).

#3	#3	#3	#3
_			
0x00	0x00	0x80	0x00
=			
T	Γ	_	
#4 MSB	#4 LSB		

5. Determine the sign of the gain correction factor using the sign bits from <u>Step 2</u>. If the offset-corrected ADC value *and* the gain correction word both have the same sign, then the factor is positive and remains unchanged. If they have differing signs, then the factor is negative and must be multiplied by -1.

#5 MSB	#5 LSB
--------	--------

6. Add the gain correction factor to the original offset corrected value.

#5 MSB	#5 LSB
+	
#1 MSB	#1 LSB
=	
#6 MSB	#6 LSB
1	1

7. Shift the result to the right, using the sign bit determined in <u>Step 1</u>, to allow for the detection of computational overflow.

	$s \rightarrow$	#6 MSB	#6 LSB
--	-----------------	--------	--------

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In the above equation, T is the temperature in °C; V is the sensor output in volts.

Assuming a compensated ADC measurement, the following equation defines the relationship between the ADC reading and the die temperature:

 $T = (25/128) \times (ADC - TSCAL[11:2]) + 30$

In the above equation, T is the temperature in C; ADC is the 10-bit compensated ADC value; and TSCAL is the temperature sensor calibration value, ignoring the two least significant bits of the 12-bit value.

See the <u>Temperature Sensor Calibration Data</u> section on page 171 for the location of TSCAL.

Calibration

The temperature sensor undergoes calibration during the manufacturing process and is maximally accurate at 30°C. Accuracy decreases as measured temperatures move further from the calibration point.

Watchdog Timer Calibration Data

Table 100. Watchdog Calibration High Byte at 007EH (WDTCALH)

Bit	7	6	5	4	3	2	1	0			
Field	WDTCALH										
RESET	U	U	U	U	U	U	U	U			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address	ess Information Page Memory 007EH										
Note: 11 -	Linchanged b	W Reset R/M	/ – Road/Writ	ō.							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit Description

[7:0] Watchdog Timer Calibration High Byte
 WDTCALH
 The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second time-out at room temperature and 3.3V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDT-CALH and WDTL with WDTCALL.

Serial Break leaves the device in DEBUG Mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns High. Because of the open-drain nature of the DBG pin, the host can send a Serial Break to the OCD even if the OCD is transmitting a character.

OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

- 1. Hold PA2/RESET Low.
- 2. Wait 5ms for the internal reset sequence to complete.
- 3. Send the following bytes serially to the debug pin:

```
DBG \leftarrow 80H (autobaud)
DBG \leftarrow EBH
DBG \leftarrow 5AH
DBG \leftarrow 70H
DBG \leftarrow CDH (32-bit unlock key)
```

- Release PA2/RESET. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20-/28-pin device. To enter DEBUG Mode, reautobaud and write 80H to the OCD Control Register (see the <u>On-Chip Debugger Commands</u> section on page 186).
- **Caution:** Between <u>Steps 3</u> and <u>4</u>, there is an interval during which the 8-pin device is neither in RE-SET nor DEBUG Mode. If a device has been erased or has not yet been programmed, all program memory bytes contain FFH. The CPU interprets this value as an illegal instruction; therefore some irregular behavior can occur before entering DEBUG Mode, and the register values after entering DEBUG Mode will differ from their specified reset values. However, none of these irregularities prevent the programming of Flash memory. Before beginning system debug, Zilog recommends that some legal code be programmed into the 8-pin device and that a RESET occurs.

Breakpoints

Execution Breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the On-Chip Debugger. If Breakpoints are enabled, the OCD enters DEBUG Mode and idles the eZ8 CPU. If Breakpoints are not

Notation	Description	Operand	Range
Vector	Vector address	Vector	Vector represents a number in the range of 00H to FFH.
Х	Indexed	#Index	The register or register pair to be indexed is off- set by the signed Index value (#Index) in a +127 to –128 range.

Table 118. Notational Shorthand (Continued)

Table 119 lists additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.

Symbol	Definition
dst	Destination Operand
SIC	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
В	Binary Number Suffix
%	Hexadecimal Number Prefix
Н	Hexadecimal Number Suffix

Table 119. Additional Symbols

Assignment of a value is indicated by an arrow, as shown in the following example.

 $dst \leftarrow dst + src$

This example indicates that the source data is added to the destination data; the result is stored in the destination location.

eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit Manipulation

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 126. Program Control Instructions

Table 127. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

				-	•			-				
Assembly	_	Add Mo	lress ode	_ Opcode(s)			Fla	ags			Fetch Cycle	Instr. Cvcle
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	s	s
RRC dst	「	R		C0	*	*	*	*	-	-	2	2
	► <u>D7D6D5D4D3D2D1D0</u> ►_C dst	IR		C1	-						2	3
SBC dst, src	$dst \gets dst - src - C$	r	r	32	*	*	*	*	1	*	2	3
	-	r	Ir	33							2	4
	-	R	R	34							3	3
	-	R	IR	35	-						3	4
	-	R	IM	36	-						3	3
	-	IR	IM	37							3	4
SBCX dst, src	$dst \leftarrow dst - src - C$	ER	ER	38	*	*	*	*	1	*	4	3
	-	ER	IM	39	-						4	3
SCF	C ← 1			DF	1	-	-	-	-	-	1	2
SRA dst		R		D0	*	*	*	0	_	-	2	2
	D7D6D5D4D3D2D1D0	IR		D1	-						2	3
SRL dst	0 - ► D7 D6 D5 D4 D3 D2 D1 D0 ► C	R		1F C0	*	*	0	*	_	_	3	2
	dst	IR		1F C1							3	3
SRP src	$RP \leftarrow src$		IM	01	_	_	_	_	_	_	2	2
STOP	STOP Mode			6F	_	-	_	_	_	-	1	2
Note: Flags Nota * = Value is a fund - = Unaffected.	ation: ction of the result of the oper	ation.										

Table 128. eZ8 CPU Instruction Summary (Continued)

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

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		V _{DD} = 2.7 V to 3.6 V				
Symbol	Parameter	Typical ¹	Maximum Std Temp ²	Maximum Ext Temp ³	Units	Conditions
I _{DD} Stop	Supply Current in STOP Mode	0.1			μA	No peripherals enabled. All pins driven to V_{DD} or $V_{SS}.$
I _{DD} Halt	Supply Current in	35	55	65	μA	32kHz.
	HALT Mode (with	520			μA	5.5MHz.
	abled)	2.1	2.85	2.85	mA	20MHz.
I _{DD}	Supply Current in	2.8			mA	32kHz.
	ACTIVE Mode	4.5	5.2	5.2	mA	5.5MHz.
	disabled)	5.5	6.5	6.5	mA	10MHz.
	,	7.9	11.5	11.5	mA	20MHz.
I _{DD} WDT	Watchdog Timer Supply Current	0.9	1.0	1.1	μA	
I _{DD}	Crystal Oscillator	40			μA	32kHz.
XTAL	Supply Current	230			μA	4MHz.
		760			μA	20MHz.
I _{DD} IPO	Internal Precision Oscillator Supply Current	350	500	550	μA	
I _{DD} VBO	Voltage Brown-Out and Low-Voltage	50			μA	For 20-/28-pin devices (VBO only); See Note 4.
	Detect Supply Cur-					For 8-pin devices; See Note 4.
I _{DD}	Analog to Digital	2.8	3.1	3.2	mA	32kHz.
ADC	Converter Supply	3.1	3.6	3.7	mA	5.5MHz.
	External Refer-	3.3	3.7	3.8	mA	10MHz.
	ence)	3.7	4.2	4.3	mA	20MHz.

Table 132. Power Consumption

Notes:

1. Typical conditions are defined as V_{DD} = 3.3 V and +30°C.

2. Standard temperature is defined as $\overline{T}_A = 0^{\circ}C$ to +70°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

3. Extended temperature is defined as $T_A = -40^{\circ}$ C to +105°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.

4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

UART Timing

Figure 37 and Table 146 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the Transmit Data Register has been loaded with data prior to CTS assertion.



Figure 3	37. U	ART	Timing	With	CTS
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		Delay (ns)			
Parameter	Abbreviation	Minimum	Maximum		
UART					
T ₁	CTS Fall to DE output delay	2 * X _{IN} period	2 * X _{IN} period + 1 bit time		
T ₂	DE assertion to TXD falling edge (start bit) delay	± 5			
T ₃	End of Stop Bit(s) to DE deassertion delay	± 5			

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