Zilog - Z8F082AHH020SG2156 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082ahh020sg2156

warning signal. The $\overline{\text{RESET}}$ pin is bidirectional, that is, it functions as reset source and as a reset indicator.

Reset, Stop Mode Recovery and Low Voltage Detection

The Reset Controller within the Z8 Encore! XP F082A Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash option bit to initiate a reset)
- External $\overline{\text{RESET}}$ pin assertion (when the alternate RESET function is enabled by the GPIO Register)
- On-chip debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery is initiated by either of the following occurrences:

- Watchdog Timer time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source

The low voltage detection circuitry on the device (available on the 8-pin product versions only) performs the following functions:

- Generates the VBO reset when the supply voltage drops below a minimum safe level.
- Generates an interrupt when the supply voltage drops below a user-defined level (8-pin devices only).

Reset Types

The Z8 Encore! XP F082A Series provides several different types of Reset operation. Stop Mode Recovery is considered as a form of Reset. Table 8 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

Port A–C Input Data Registers

Reading from the Port A–C Input Data registers, shown in Table 29, return the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Table 29. Port A–C Input Data Registers (PxIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD2H, FD6H, FDAH							

X = Undefined.

Bit	Description
[7:0] PxIN	**Port Input Data** Sampled data from the corresponding port pin input. 0 = Input data is logical 0 (Low). 1 = Input data is logical 1 (High).

Note: x indicates the specific GPIO port pin number (7–0).

Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

Table 30. Port A–D Output Data Register (P*x*OUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H, FD7H, FDBH, FDFH							

Bit	Description
[7:0] PxOUT	**Port Output Data** These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for alternate function operation. 0 = Drive a logical 0 (Low). 1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding Port Output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Table 31. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Bit	Description
[7:0] LEDENx	**LED Drive Enable** These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1 = Enable controlled current sink on the Port C pin. **Note:** *x* indicates the specific GPIO port pin number (7–0).

LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin, as shown in Table 32. These two bits select between four programmable drive levels. Each pin is individually programmable.

Table 32. LED Drive Level High Register (LEDLVLH)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

Bit	Description
[7:0] LEDLVLHx	**LED Level High Bit** {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA 01 = 7mA 10 = 13mA 11 = 20mA

Note: x indicates the specific GPIO port pin number (7–0).

Architecture

Figure 8 displays the interrupt controller block diagram.

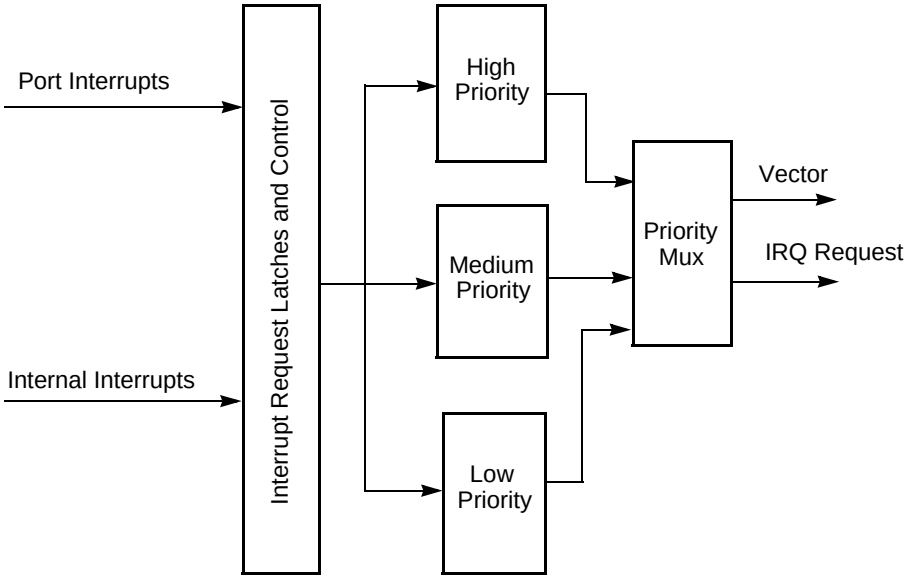

Figure 8. Interrupt Controller Block Diagram

Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 57

Interrupt Vectors and Priority: see page 58

Interrupt Assertion: see page 58

Software Interrupt Assertion: see page 59

Watchdog Timer Interrupt Assertion: see page 59

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables interrupts. Interrupts are globally enabled by any of the following actions:

- Execution of an EI (Enable Interrupt) instruction
- Execution of an IRET (Return from Interrupt) instruction

Table 42. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7VENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Bit	Description
[7] PA7VENH	**Port A Bit[7] or LVD Interrupt Request Enable High Bit**
[6] PA6CENH	**Port A Bit[7] or Comparator Interrupt Request Enable High Bit**
[5:0] PAxENH	**Port A Bit[*x*] Interrupt Request Enable High Bit**

See the Shared Interrupt Select Register (IRQSS) Register on page 68 for selection of either the LVD or the comparator as the interrupt source.

Table 43. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7VENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Bit	Description
[7] PA7VENL	**Port A Bit[7] or LVD Interrupt Request Enable Low Bit**
[6] PA6CENL	**Port A Bit[6] or Comparator Interrupt Request Enable Low Bit**
[5:0] PAxENL	**Port A Bit[*x*] Interrupt Request Enable Low Bit**

IRQ2 Enable High and Low Bit Registers

Table 44 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers, shown in Tables 44 and 45, form a priority-encoded enabling for interrupts in the Interrupt Request 2 Register.

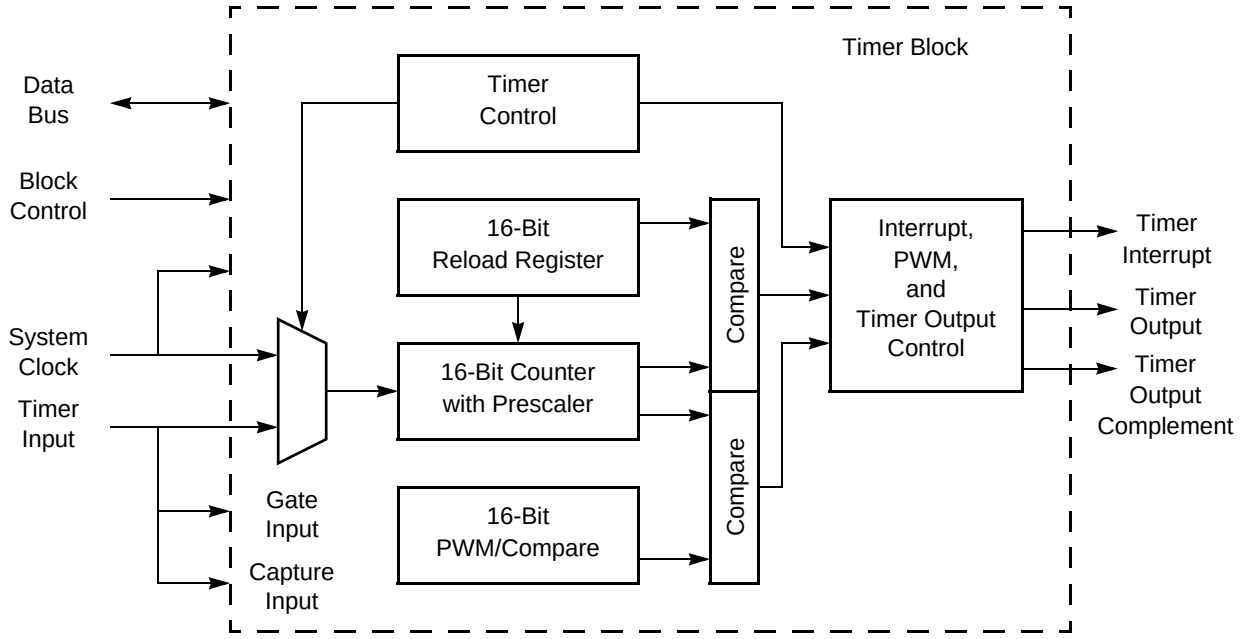

Figure 9. Timer Block Diagram

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer Reload. If

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 56 and 57, control Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 56. Timer 0–1 PWM High Byte Register (TxPWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H, F0CH							

Table 57. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H, F0DH							

Bit	Description
[7:0] PWMH, PWML	**Pulse-Width Modulator High and Low Bytes** These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control Register (TxCTL1) Register.

The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1. For more information about system reset, see the Reset, Stop Mode Recovery and Low Voltage Detection chapter on page 22.

WDT Reset in STOP Mode

If configured to generate a Reset when a time-out occurs and the device is in STOP Mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Reset Status (RSTSTAT) Register are set to 1 following WDT time-out in STOP Mode.

Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the Reload registers. Observe the following steps to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) for write access.

1. Write 55H to the Watchdog Timer Control Register (WDTCTL).
2. Write AAH to the Watchdog Timer Control Register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte Register (WDTU) with the appropriate time-out value.
4. Write the Watchdog Timer Reload High Byte Register (WDTH) with the appropriate time-out value.
5. Write the Watchdog Timer Reload Low Byte Register (WDTL) with the appropriate time-out value.

All three Watchdog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

Watchdog Timer Calibration

Due to its extremely low operating current, the Watchdog Timer oscillator is somewhat inaccurate. This variation can be corrected using the calibration data stored in the Flash Information Page; see Tables 100 and 101 on page 173 for details. Loading these values

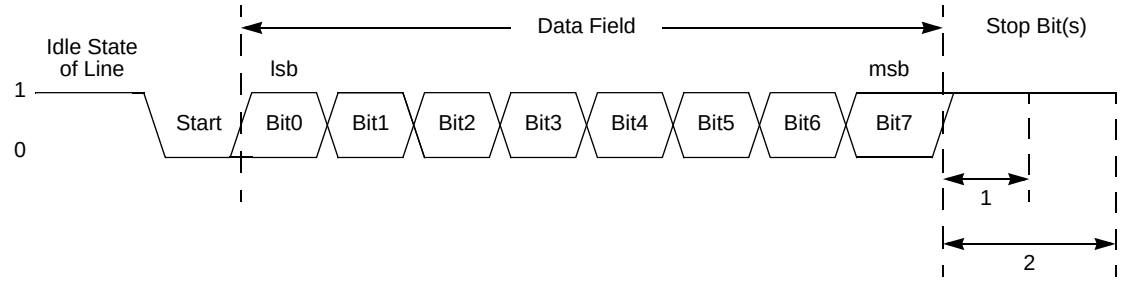

Figure 11. UART Asynchronous Data Format without Parity

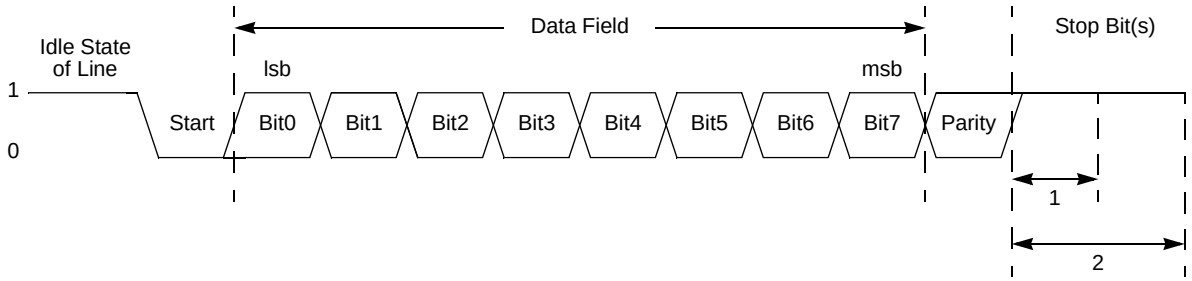

Figure 12. UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Observe the following steps to transmit data using the polled method of operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Write to the UART Control 1 Register, if MULTIPROCESSOR Mode is appropriate, to enable MULTIPROCESSOR (9-bit) Mode functions.
4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR Mode.
5. Write to the UART Control 0 Register to:
   - Set the transmit enable bit (TEN) to enable the UART for data transmission
   - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR Mode is not enabled and select either even or odd parity (PSEL)

6. Read data from the UART Receive Data Register. If operating in MULTIPROCESSOR (9-bit) Mode, further actions may be required depending on the MULTIPROCESSOR Mode bits MPMD[1:0].
7. Return to Step 4 to receive additional data.

Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (and error conditions). Observe the following steps to configure the UART receiver for interrupt-driven operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
5. Clear the UART Receiver interrupt in the applicable Interrupt Request Register.
6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
   - Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR Mode.
   - Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme.
   - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! devices without a DMA block)
7. Write the device address to the Address Compare Register (automatic MULTIPROCESSOR Modes only).
8. Write to the UART Control 0 Register to:
   - Set the receive enable bit (REN) to enable the UART for data reception
   - Enable parity, if appropriate and if multiprocessor mode is not enabled and select either even or odd parity
9. Execute an EI instruction to enable interrupts.

Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. The UART data rate is calculated using the following equation:

$$\text{UART Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

When the UART is disabled, the Baud Rate Generator functions as a basic 16-bit timer with an interrupt upon time-out. Observe the following steps to configure the Baud Rate Generator as a timer with an interrupt upon time-out:

1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 Register to 0.
2. Load the acceptable 16-bit count value into the UART Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 Register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

$$\text{Interrupt Interval(s)} = \text{System Clock Period (s)} \times \text{BRG[15:0]}$$

UART Control Register Definitions

The UART Control registers support the UART and the associated Infrared Encoder/Decoders. For more information about infrared operation, see the Infrared Encoder/Decoder chapter on page 120.

UART Control 0 and Control 1 Registers

The UART Control 0 (UxCTL0) and Control 1 (UxCTL1) registers, shown in Tables 63 and 64, configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

Bit	Description (Continued)
[2] BRGCTL	**Baud Rate Control** This bit causes an alternate UART behavior depending on the value of the REN bit in the UART Control 0 Register. When the UART receiver is not enabled (REN=0), this bit determines whether the Baud Rate Generator issues interrupts. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG reload value. 1 = The Baud Rate Generator generates a receive interrupt when it counts down to 0. Reads from the Baud Rate High and Low Byte registers return the current BRG count value. When the UART receiver is enabled (REN=1), this bit allows reads from the Baud Rate registers to return the BRG count value instead of the reload value. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG reload value. 1 = Reads from the Baud Rate High and Low Byte registers return the current BRG count value. Unlike the Timers, there is no mechanism to latch the Low Byte when the High Byte is read.
[1] RDAIRQ	**Receive Data Interrupt Enable** 0 = Received data and receiver errors generates an interrupt request to the Interrupt Controller. 1 = Received data does not generate an interrupt request to the Interrupt Controller. Only receiver errors generate an interrupt request.
[0] IREN	**Infrared Encoder/Decoder Enable** 0 = Infrared Encoder/Decoder is disabled. UART operates normally. 1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

Trim Bit Data Register

The Trim Bid Data (TRMDR) Register contains the read or write data for access to the trim option bits (Table 87).

Table 87. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR: Trim Bit Data							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H							

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

Flash Program Memory Address 0000H

Table 88. Flash Option Bits at Program Memory Address 0000H

Bit	7	6	5	4	3	2	1	0
Field	WDT_RES	WDT_AO	OSC_SEL[1:0]		VBO_AO	FRP	Reserved	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0000H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7] WDT_RES	**Watchdog Timer Reset** 0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request. 1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.
[6] WDT_AO	**Watchdog Timer Always On** 0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled. 1 = Watchdog Timer is enabled upon execution of the WDT instruction. Once enabled, the Watchdog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Trim Bit Address 0002H

Table 92. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0] IPO_TRIM	**Internal Precision Oscillator Trim Byte** Contains trimming bits for the Internal Precision Oscillator.

Trim Bit Address 0003H

Note: The LVD is available on 8-pin devices only.

Table 93. Trim Option Bits at Address 0003H (TLVD)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			LVD_TRIM				
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0023H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:5]	**Reserved** These bits are reserved and must be programmed to 111.
[4:0] LVD_TRIM	**Low Voltage Detect Trimm** This trimming affects the low voltage detection threshold. Each LSB represents a 50mV change in the threshold level. Alternatively, the low voltage threshold may be computed from the options bit value by the following equation: $LVD\_LVL = 3.6\ V - LVD\_TRIM \times 0.05\ V$ These values are tabulated in Table 94.

enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The On-Chip Debugger contains a 16-bit Runtime Counter. It counts system clock cycles between Breakpoints. The counter starts counting when the On-Chip Debugger leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the on-chip debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of the Z8 Encore! XP F082A Series device. When this option is enabled, several of the OCD commands are disabled. See Table 109.

Table 110 on page 191 is a summary of the on-chip debugger commands. Each OCD command is described in further detail in the bulleted list following this table. Table 110 also indicates those commands that operate when the device is not in DEBUG Mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Table 109. Debug Command Enable/Disable

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	–
Reserved	01H	–	–
Read OCD Status Register	02H	Yes	–
Read Runtime Counter	03H	–	–
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	–

Table 132. Power Consumption (Continued)

		V_{DD} = 2.7 V to 3.6 V				
Symbol	**Parameter**	**Typical[1]**	**Maximum Std Temp[2]**	**Maximum Ext Temp[3]**	**Units**	**Conditions**
I_{DD} ADCRef	ADC Internal Reference Supply Current	0			µA	See Note 4.
I_{DD} CMP	Comparator supply Current	150	180	190	µA	See Note 4.
I_{DD} LPO	Low-Power Operational Amplifier Supply Current	3	5	5	µA	Driving a high-impedance load.
I_{DD} TS	Temperature Sensor Supply Current	60			µA	See Note 4.
I_{DD} BG	Band Gap Supply Current	320	480	500	µA	For 20-/28-pin devices.
						For 8-pin devices.

Notes:
1. Typical conditions are defined as V_{DD} = 3.3V and +30°C.
2. Standard temperature is defined as T_A = 0°C to +70°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as T_A = –40°C to +105°C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

Table 142. Temperature Sensor Electrical Characteristics

		V_{DD} = 2.7 V to 3.6 V				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
T_{AERR}	Temperature Error		±0.5	±2	°C	Over the range +20°C to +30°C (as measured by ADC).[1]
			±1	±5	°C	Over the range +0°C to +70°C (as measured by ADC).
			±2	±7	°C	Over the range +0°C to +105°C (as measured by ADC).
			±7		°C	Over the range –40°C to +105°C (as measured by ADC).
t_{WAKE}	Wakeup Time		80	100	µs	Time required for Temperature Sensor to stabilize after enabling.

Note: Devices are factory calibrated at for maximal accuracy between +20°C and +30°C, so the sensor is maximally accurate in that range. User recalibration for a different temperature range is possible and increases accuracy near the new calibration point.

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 2 KB Flash											
Standard Temperature: 0°C to 70°C											
Z8F021APB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020SG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020SG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020SG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: –40°C to 105°C											
Z8F021APB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020EG	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020EG	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020EG	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package