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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082apj020sg2156

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Table 4. Pin Characteristics (8-Pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
PA1	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
$\overline{\text{RESET}}$ / PA2	I/O	I/O (defaults to $\overline{\text{RESET}}$)	Low (in Reset mode)	Yes	Programma- ble for PA2; always on for $\overline{\text{RESET}}$	Yes	Programma- ble for PA2; always on for $\overline{\text{RESET}}$	Yes, unless pull-ups enabled
PA[5:3]	I/O	I	N/A	Yes	Programma- ble Pull-up	Yes	Yes, Programma- ble	Yes, unless pull-ups enabled
V _{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
V _{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page
F85	Reserved	—	XX	
Oscillator Control				
F86	Oscillator Control	OSCCTL	A0	<u>196</u>
F87–F8F	Reserved	—	XX	
Comparator 0				
F90	Comparator 0 Control	CMP0	14	<u>141</u>
F91–FBF	Reserved	—	XX	
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	<u>60</u>
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	<u>63</u>
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	<u>63</u>
FC3	Interrupt Request 1	IRQ1	00	<u>61</u>
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	<u>65</u>
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	<u>65</u>
FC6	Interrupt Request 2	IRQ2	00	<u>62</u>
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	<u>66</u>
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	<u>67</u>
FC9–FCC	Reserved	—	XX	
FCD	Interrupt Edge Select	IRQES	00	<u>68</u>
FCE	Shared Interrupt Select	IRQSS	00	<u>68</u>
FCF	Interrupt Control	IRQCTL	00	<u>69</u>
GPIO Port A				
FD0	Port A Address	PAADDR	00	<u>44</u>
FD1	Port A Control	PACTL	00	<u>46</u>
FD2	Port A Input Data	PAIN	XX	<u>46</u>
FD3	Port A Output Data	PAOUT	00	<u>46</u>
GPIO Port B				
FD4	Port B Address	PBADDR	00	<u>44</u>
FD5	Port B Control	PBCTL	00	<u>46</u>
FD6	Port B Input Data	PBIN	XX	<u>46</u>
FD7	Port B Output Data	PBOUT	00	<u>46</u>
GPIO Port C				
FD8	Port C Address	PCADDR	00	<u>44</u>

Notes:

1. XX = Undefined.
2. Refer to the [eZ8 CPU Core User Manual \(UM0128\)](#).

Reset Sources

Table 9 lists the possible sources of a system reset.

Table 9. Reset Sources and Resulting Reset Type

Operating Mode	Reset Source	Special Conditions
NORMAL or HALT modes	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	Watchdog Timer time-out when configured for Reset	None.
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugger is unaffected by the reset.
STOP Mode	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.
	DBG pin driven Low	None.

Power-On Reset

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V_{POR}).

and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the $\overline{\text{RESET}}$ input pin is asserted Low, the Z8 Encore! XP F082A Series devices remain in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state on the system clock rising edge following $\overline{\text{RESET}}$ pin deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status (RSTSTAT) Register is set to 1.

External Reset Indicator

During System Reset or when enabled by the GPIO logic (see [Table 20 on page 46](#)), the $\overline{\text{RESET}}$ pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in [Table 8](#) has elapsed.

On-Chip Debugger Initiated Reset

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control Register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) Register is set.

Stop Mode Recovery

STOP Mode is entered by execution of a STOP instruction by the eZ8 CPU. See the [Low-Power Modes](#) chapter on page 32 for detailed STOP Mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (see [Table 135](#) on page 233) T_{SMR} , also includes the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control Register (WDTCTL) and the Oscillator Control Register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vec-

without initiating an interrupt (if enabled for that pin).

Stop Mode Recovery Using the External $\overline{\text{RESET}}$ Pin

When the Z8 Encore! XP F082A Series device is in STOP Mode and the external $\overline{\text{RESET}}$ pin is driven Low, a system reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the Low pulse must be greater than the minimum width specified, or it is ignored. See the [Electrical Characteristics](#) chapter on page 226 for details.

Low Voltage Detection

In addition to the Voltage Brown-Out (VBO) Reset described above, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. For details about configuring the Low Voltage Detection (LVD) and the threshold levels available, see the [Trim Option Bits at Address 0003H \(TLVD\) Register](#) on page 166. The LVD function is available on the 8-pin product versions only.

When the supply voltage drops below the LVD threshold, the LVD bit of the Reset Status (RSTSTAT) Register is set to one. This bit remains one until the low-voltage condition goes away. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when so enabled, see the [GPIO Mode Interrupt Controller](#) chapter on page 55. The LVD bit is not latched; therefore, enabling the interrupt is the only way to guarantee detection of a transient low voltage event.

The LVD functionality depends on circuitry shared with the VBO block; therefore, disabling the VBO also disables the LVD.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The read-only Reset Status (RSTSTAT) Register, shown in Table 11, indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0. This register shares its address with the write-only Watchdog Timer Control Register.

Table 12 lists the bit settings for Reset and Stop Mode Recovery events.

HALT Mode

Executing the eZ8 CPU's HALT instruction places the device into HALT Mode, which powers down the CPU but leaves all other peripherals active. In HALT Mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- If enabled, the Watchdog Timer continues to operate
- All other on-chip peripherals continue to operate, if enabled

The eZ8 CPU can be brought out of HALT Mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out reset
- External $\overline{\text{RESET}}$ pin assertion

To minimize current in HALT Mode, all GPIO pins that are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

Peripheral-Level Power Control

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! XP F082A Series devices. Disabling a given peripheral minimizes its power consumption.

Power Control Register Definitions

The following sections define the Power Control registers.

Power Control Register 0

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block. The default state of the low-power

- Set the prescale value
 - If using the Timer Output alternate function, set the initial output level (High or Low)
2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer Reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.
 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
 4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
 5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
 6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is computed via the following equation:

$$\text{CONTINUOUS Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER Mode, the prescaler is disabled.

! Caution: The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the input signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is

- Set the Capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
 4. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 Register.
 5. Configure the associated GPIO port pin for the Timer Input alternate function.
 6. Write to the Timer Control Register to enable the timer.
 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the Timer Low Byte Register are placed in a holding register. A subsequent read from the Timer Low Byte Register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte Register returns the actual value in the counter.

Timer Pin Signal Operation

The timer output function is a GPIO port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

Bit	Description (Continued)
[6] TPOL	<p>Timer Input/Output Polarity Operation of this bit is a function of the current operating mode of the timer.</p> <p>ONE-SHOT Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>CONTINUOUS Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>COUNTER Mode If the timer is enabled the Timer Output signal is complemented after timer reload. 0 = Count occurs on the rising edge of the Timer Input signal. 1 = Count occurs on the falling edge of the Timer Input signal.</p> <p>PWM SINGLE OUTPUT Mode 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload. 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.</p> <p>CAPTURE Mode 0 = Count is captured on the rising edge of the Timer Input signal. 1 = Count is captured on the falling edge of the Timer Input signal.</p> <p>COMPARE Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p>

Table 52. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H							

Table 53. Timer 0–1 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

Bit	Description
[7:0]	Timer High and Low Bytes
TH, TL	These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Table 62. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	00H							
R/W	R/W*							
Address	FF3H							
Note: A read returns the current WDT count value; a write sets the appropriate reload value.								

Bit	Description
[7:0]	WDT Reload Low
WDTL	Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

Bit	Description (Continued)
[5:2]	Internal Reference Voltage Level
REFLVL	This reference is independent of the ADC voltage reference. Note: 8-pin devices contain two additional LSBs for increased resolution. For 20-/28-pin devices: 0000 = 0.0 V 0001 = 0.2 V 0010 = 0.4 V 0011 = 0.6 V 0100 = 0.8 V 0101 = 1.0 V (Default) 0110 = 1.2 V 0111 = 1.4 V 1000 = 1.6 V 1001 = 1.8 V 1010–1111 = Reserved

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a `CALL` instruction to the address of the byte-read routine (`0x1000`). At the return from the sub-routine, the read byte resides in working register R0 and the read status byte resides in working register R1. The contents of the status byte are undefined for read operations to illegal addresses. Also, the user code must pop the address byte off the stack.

The read routine uses 9 bytes of stack space in addition to the one byte of address pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between 44 μ s and 489 μ s (assuming a 20MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return `0xff`. Illegal read operations have a 2 μ s execution time.

The status byte returned by the NVDS read routine is zero for successful read, as determined by a CRC check. If the status byte is nonzero, there was a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have a CRC error.

Power Failure Protection

The NVDS routines employ error checking mechanisms to ensure a power failure endangers only the most recently written byte. Bytes previously written to the array are not perturbed.

A system reset (such as a pin reset or Watchdog Timer reset) that occurs during a write operation also perturbs the byte currently being written. All other bytes in the array are unperturbed.

Optimizing NVDS Memory Usage for Execution Speed

NVDS read time can vary drastically. This discrepancy is a trade-off for minimizing the frequency of writes that require post-write page erases, as indicated in Table 107. The NVDS read time of address N is a function of the number of writes to addresses other than N since the most recent write to address N, plus the number of writes since the most recent page erase. Neglecting effects caused by page erases and results caused by the initial condition in which the NVDS is blank, a rule of thumb is that every write since the most recent page erase causes read times of unwritten addresses to increase by 1 μ s up to a maximum of $(511 - \text{NVDS_SIZE})\mu$ s.

Table 123. CPU Control Instructions (Continued)

Mnemonic	Operands	Instruction
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 124. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 125. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 126. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 127. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

Figure 33 displays the typical current consumption while operating with all peripherals disabled, at 30 °C, versus the system clock frequency.

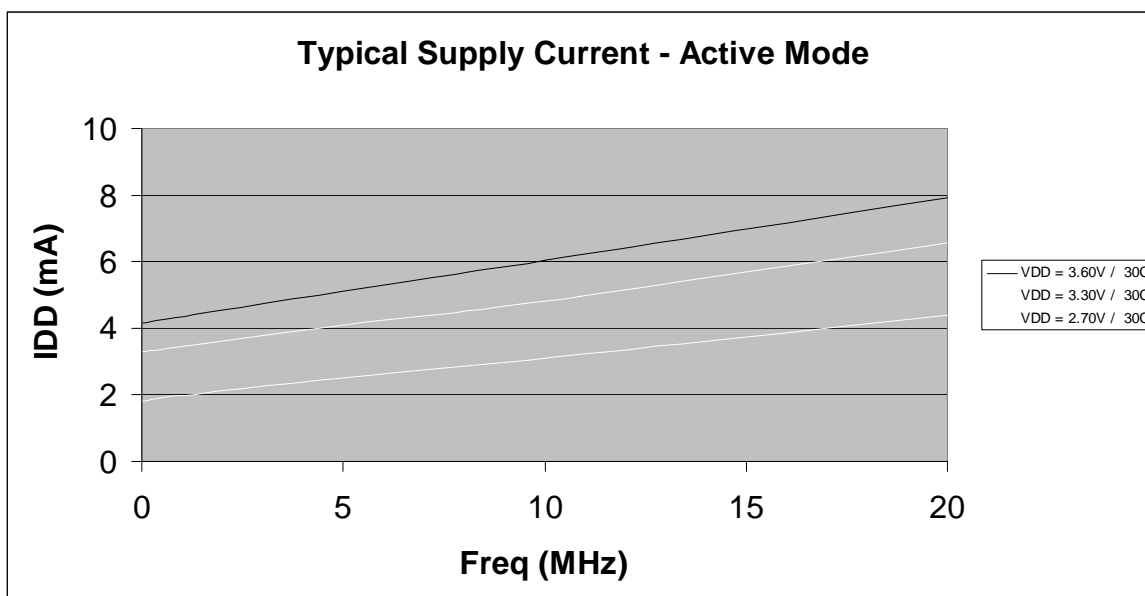


Figure 33. Typical Active Mode I_{DD} Versus System Clock Frequency

Table 148. Z8 Encore! XP F082A Series Ordering Matrix

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP F082A Series with 8KB Flash											
Standard Temperature: 0°C to 70°C											
Z8F081APB020SG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020SG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020SG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020SG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020SG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020SG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40°C to 105°C											
Z8F081APB020EG	8KB	1KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020EG	8KB	1KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020EG	8KB	1KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020EG	8KB	1KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020EG	8KB	1KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020EG	8KB	1KB	0	25	19	2	0	1	1	0	PDIP 28-pin package

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Customer Support

To share comments, get your technical questions answered, or report issues you may be experiencing with our products, please visit Zilog's Technical Support page at <http://support.zilog.com>.

To learn more about this product, find additional documentation, or to discover other facts about Zilog product offerings, please visit the Zilog Knowledge Base at <http://zilog.com/kb> or consider participating in the Zilog Forum at <http://zilog.com/forum>.

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