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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082asj020eg

LED Drive Level Low Register	54
GPIO Mode Interrupt Controller	55
Interrupt Vector Listing	55
Architecture	57
Operation	57
Master Interrupt Enable	57
Interrupt Vectors and Priority	58
Interrupt Assertion	58
Software Interrupt Assertion	59
Watchdog Timer Interrupt Assertion	59
Interrupt Control Register Definitions	60
Interrupt Request 0 Register	60
Interrupt Request 1 Register	61
Interrupt Request 2 Register	62
IRQ0 Enable High and Low Bit Registers	62
IRQ1 Enable High and Low Bit Registers	64
IRQ2 Enable High and Low Bit Registers	65
Interrupt Edge Select Register	67
Shared Interrupt Select Register	68
Interrupt Control Register	69
Timers	70
Architecture	70
Operation	71
Timer Operating Modes	71
Reading the Timer Count Values	84
Timer Pin Signal Operation	84
Timer Control Register Definitions	85
Timer 0–1 Control Registers	85
Timer 0–1 High and Low Byte Registers	89
Timer Reload High and Low Byte Registers	91
Timer 0–1 PWM High and Low Byte Registers	92
Watchdog Timer	93
Operation	93
Watchdog Timer Refresh	94
Watchdog Timer Time-Out Response	94
Watchdog Timer Reload Unlock Sequence	95
Watchdog Timer Calibration	95
Watchdog Timer Control Register Definitions	96
Watchdog Timer Control Register	96
Watchdog Timer Reload Upper, High and Low Byte Registers	97

Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code.

Universal Asynchronous Receiver/Transmitter

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and

PA0 and PA6 contain two different timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the timer mode. See **the Timers chapter on page 70** for more details.

! Caution: For pins with multiple alternate functions, Zilog recommends writing to the AFS1 and AFS2 subregisters before enabling the alternate function via the AF subregister. As a result, spurious transitions through unwanted alternate function modes will be prevented.

Direct LED Drive

The Port C pins provide a current sinked output capable of driving an LED without requiring an external resistor. The output sinks current at programmable levels of 3 mA, 7 mA, 13 mA and 20 mA. This mode is enabled through the LED control registers. The LED Drive Enable (LEDEN) Register turns on the drivers. The LED Drive Level (LEDLVLH and LEDLVLL) registers select the sink current.

For correct function, the LED anode must be connected to V_{DD} and the cathode to the GPIO pin. Using all Port C pins in LED drive mode with maximum current may result in excessive total current. See **the Electrical Characteristics chapter on page 226** for the maximum total current for the applicable package.

Shared Reset Pin

On the 20- and 28-pin devices, the PD0 pin shares function with a bidirectional reset pin. Unlike all other I/O pins, this pin does not default to GPIO function on power-up. This pin acts as a bidirectional input/open-drain output reset until the software reconfigures it. The PD0 pin is an output-only open drain when in GPIO mode. There are no pull-up, High Drive, or Stop Mode Recovery source features associated with the PD0 pin.

On the 8-pin product versions, the reset pin is shared with PA2, but the pin is not limited to output-only when in GPIO mode.

! Caution: If PA2 on the 8-pin product is reconfigured as an input, ensure that no external stimulus drives the pin low during any reset sequence. Since PA2 returns to its RESET alternate function during system resets, driving it Low holds the chip in a reset state until the pin is released.

Table 16. Port Alternate Function Mapping (8-Pin Parts)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Select Register AFS1	Alternate Function Select Register AFS2
Port A	PA0	T0IN	Timer 0 Input	AFS1[0]: 0	AFS2[0]: 0
		Reserved		AFS1[0]: 0	AFS2[0]: 1
		Reserved		AFS1[0]: 1	AFS2[0]: 0
		$\overline{T0OUT}$	Timer 0 Output Complement	AFS1[0]: 1	AFS2[0]: 1
	PA1	T0OUT	Timer 0 Output	AFS1[1]: 0	AFS2[1]: 0
		Reserved		AFS1[1]: 0	AFS2[1]: 1
		CLKIN	External Clock Input	AFS1[1]: 1	AFS2[1]: 0
		Analog Functions ¹	ADC Analog Input/V _{REF}	AFS1[1]: 1	AFS2[1]: 1
	PA2	DE0	UART 0 Driver Enable	AFS1[2]: 0	AFS2[2]: 0
		RESET	External Reset	AFS1[2]: 0	AFS2[2]: 1
		T1OUT	Timer 1 Output	AFS1[2]: 1	AFS2[2]: 0
		Reserved		AFS1[2]: 1	AFS2[2]: 1
	PA3	$\overline{CTS0}$	UART 0 Clear to Send	AFS1[3]: 0	AFS2[3]: 0
		COUT	Comparator Output	AFS1[3]: 0	AFS2[3]: 1
		T1IN	Timer 1 Input	AFS1[3]: 1	AFS2[3]: 0
		Analog Functions ²	ADC Analog Input/LPO Input (P)	AFS1[3]: 1	AFS2[3]: 1
	PA4	RXD0	UART 0 Receive Data	AFS1[4]: 0	AFS2[4]: 0
		Reserved		AFS1[4]: 0	AFS2[4]: 1
		Reserved		AFS1[4]: 1	AFS2[4]: 0
		Analog Functions ²	ADC/Comparator Input (N)/LPO Input (N)	AFS1[4]: 1	AFS2[4]: 1
	PA5	TXD0	UART 0 Transmit Data	AFS1[5]: 0	AFS2[5]: 0
		$\overline{T1OUT}$	Timer 1 Output Complement	AFS1[5]: 0	AFS2[5]: 1
		Reserved		AFS1[5]: 1	AFS2[5]: 0
		Analog Functions ²	ADC/Comparator Input (P) LPO Output	AFS1[5]: 1	AFS2[5]: 1

Notes:

1. Analog functions include ADC inputs, ADC reference, comparator inputs and LPO ports.
2. The alternate function selection must be enabled; see the [Port A–D Alternate Function Subregisters \(PxAF\)](#) section on page 47 for details.

Bit	Description (Continued)
[4] U0REN	UART 0 Receive Interrupt Request Enable Low Bit
[3] U0TEN	UART 0 Transmit Interrupt Request Enable Low Bit
[2:1]	Reserved These bits are reserved and must be programmed to 00.
[0] ADCEN	ADC Interrupt Request Enable Low Bit

IRQ1 Enable High and Low Bit Registers

Table 41 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers, shown in Tables 41 and 42, form a priority-encoded enabling for interrupts in the Interrupt Request 1 Register.

Table 41. IRQ1 Enable and Priority Encoding

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

Note: x indicates register bits 0–7.

Bit	Description (Continued)
[6] TPOL	<p>Timer Input/Output Polarity Operation of this bit is a function of the current operating mode of the timer.</p> <p>ONE-SHOT Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>CONTINUOUS Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p> <p>COUNTER Mode If the timer is enabled the Timer Output signal is complemented after timer reload. 0 = Count occurs on the rising edge of the Timer Input signal. 1 = Count occurs on the falling edge of the Timer Input signal.</p> <p>PWM SINGLE OUTPUT Mode 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon reload. 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon reload.</p> <p>CAPTURE Mode 0 = Count is captured on the rising edge of the Timer Input signal. 1 = Count is captured on the falling edge of the Timer Input signal.</p> <p>COMPARE Mode When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.</p>

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 60 through 62, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate reload value. Reading from these registers returns the current Watchdog Timer count value.

! Caution: The 24-bit WDT reload value must not be set to a value less than 000004H.

Table 60. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	00H							
R/W	R/W*							
Address	FF1H							
Note: A read returns the current WDT count value; a write sets the appropriate reload value.								

Bit	Description
[7:0] WDTU	WDT Reload Upper Byte Most-significant byte (MSB); bits[23:16] of the 24-bit WDT reload value.

Table 61. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	04H							
R/W	R/W*							
Address	FF2H							
Note: A read returns the current WDT count value; a write sets the appropriate reload value.								

Bit	Description
[7:0] WDTH	WDT Reload High Byte Middle byte; bits[15:8] of the 24-bit WDT reload value.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the infrared endec. The infrared endec data rate is calculated using the following equation:

$$\text{Infrared Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16 clocks wide. If the data to be transmitted is 1, the IR_TXD signal remains low for the full 16 clock period. If the data to be transmitted is 0, the transmitter first outputs a 7 clock low period, followed by a 3 clock high pulse. Finally, a 6 clock low pulse is output to complete the full 16 clock data period. Figure 17 displays IrDA data transmission. When the infrared endec is enabled, the UART's TXD signal is internal to the Z8 Encore! XP F082A Series products while the IR_TXD signal is output through the TXD pin.

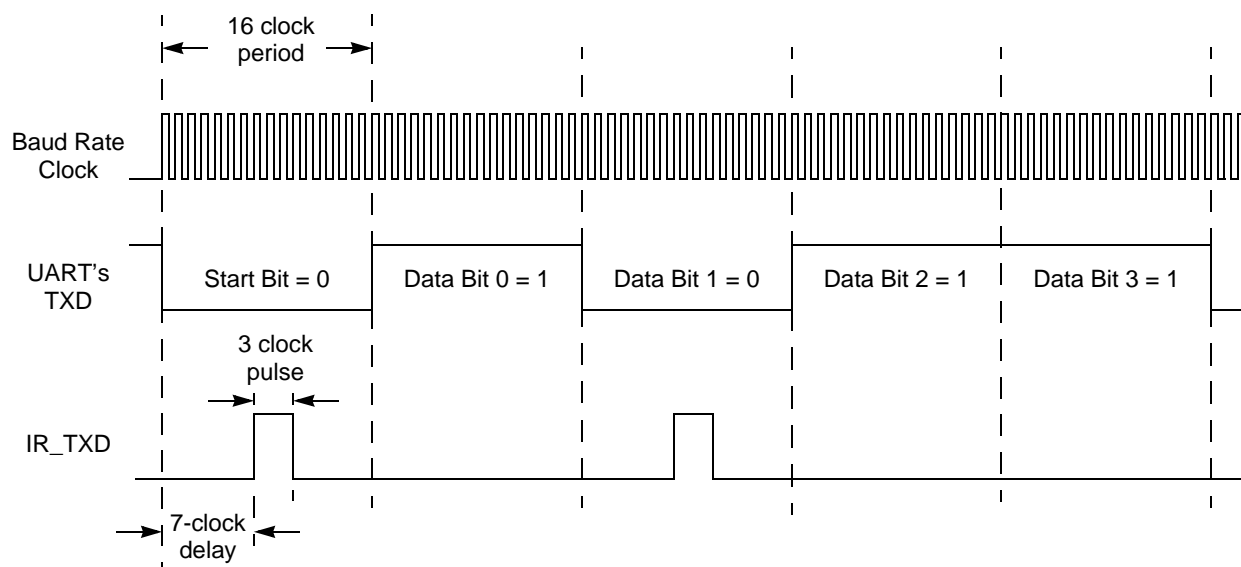


Figure 17. Infrared Data Transmission

- Write to BUFMODE[2:0] to select SINGLE-ENDED or DIFFERENTIAL mode, plus unbuffered or buffered mode.
 - Write the REFSELH bit of the pair {REFSELH, REFSSELL} to select the internal voltage reference level or to disable the internal reference. The REFSSELL bit is contained in the ADC Control Register 0.
3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control Register may be written simultaneously:
 - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
 - Set CONT to 1 to select continuous conversion.
 - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
 - Write the REFSSELL bit of the pair {REFSELH, REFSSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in ADC Control/Status Register 1.
 - Set CEN to 1 to start the conversions.
 4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
 - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation
 - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete
 5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
 - Writes the 13-bit two's complement result to {ADCD_H[7:0], ADCD_L[7:3]}
 - Sends an interrupt request to the Interrupt Controller denoting conversion complete
 6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

► **Note:** The offset compensation is performed first, followed by the gain compensation. One bit of resolution is lost because of rounding on both the offset and gain computations. As a result the ADC registers read back 13 bits: 1 sign bit, two calibration bits lost to rounding and 10 data bits.

Also note that in the second term, the multiplication must be performed before the division by 2^{16} . Otherwise, the second term incorrectly evaluates to zero.

! **Caution:** Although the ADC can be used without the gain and offset compensation, it does exhibit nonunity gain. Designing the ADC with sub-unity gain reduces noise across the ADC range but requires the ADC results to be scaled by a factor of 8/7.

ADC Compensation Details

High-efficiency assembly code that performs ADC compensation is available for download on www.zilog.com. This section offers a bit-specific description of the ADC compensation process used by this code.

The following data bit definitions are used:

0–9, a–f = bit indices in hexadecimal
s = sign bit
v = overflow bit
– = unused

Input Data

MSB	LSB	
s b a 9 8 7 6 5	4 3 2 1 0 – – v	(ADC)
		ADC Output Word; if v = 1, the data is invalid
	s 6 5 4 3 2 1 0	Offset Correction Byte
s s s s s 7 6 5	4 3 2 1 0 0 0 0	(Offset)
		Offset Byte shifted to align with ADC data
s e d c b a 9 8	7 6 5 4 3 2 1 0	(Gain)
		Gain Correction Word

#3	#3	#3	#3
----	----	----	----

4. Round the result and discard the least significant two bytes (equivalent to dividing by 2^{16}).

#3	#3	#3	#3
----	----	----	----

–

0x00	0x00	0x80	0x00
------	------	------	------

=

#4 MSB	#4 LSB
--------	--------

5. Determine the sign of the gain correction factor using the sign bits from Step 2. If the offset-corrected ADC value *and* the gain correction word both have the same sign, then the factor is positive and remains unchanged. If they have differing signs, then the factor is negative and must be multiplied by –1.

#5 MSB	#5 LSB
--------	--------

6. Add the gain correction factor to the original offset corrected value.

#5 MSB	#5 LSB
--------	--------

+

#1 MSB	#1 LSB
--------	--------

=

#6 MSB	#6 LSB
--------	--------

7. Shift the result to the right, using the sign bit determined in Step 1, to allow for the detection of computational overflow.

S →	#6 MSB	#6 LSB
-----	--------	--------

Bit	Description (Continued)
[2:1]	Reserved These bits are reserved and must be undefined.
[0] OVF	Overflow Status 0 = A hardware overflow did not occur in the ADC for the current sample. 1 = A hardware overflow did occur in the ADC for the current sample, therefore the current sample is invalid.

Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

! **Caution:** The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device. Also, Flash programming and erasure is not supported for system clock frequencies below 20kHz or above 20MHz.

Table 84. Flash Frequency High Byte Register (FFREQH)

Bit	7	6	5	4	3	2	1	0
Field	FFREQH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FFAH							

Bit	Description
-----	-------------

[7:0]	Flash Frequency High Byte
-------	----------------------------------

FFREQH	High byte of the 16-bit Flash Frequency value.
--------	--

Table 85. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

Bit	Description
-----	-------------

[7:0]	Flash Frequency Low Byte
-------	---------------------------------

FFREQL	Low byte of the 16-bit Flash Frequency value.
--------	---

These serial numbers are stored in the Flash information page and are unaffected by mass erasure of the device's Flash memory. See the Reading the Flash Information Page section below and the [Serialization Data](#) section on page 173 for more details.

Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

The randomized lot identifier is a 32 byte binary value, stored in the Flash information page and is unaffected by mass erasure of the device's Flash memory. See Reading the Flash Information Page, below, and the [Randomized Lot Identifier](#) section on page 174 for more details.

Reading the Flash Information Page

The following code example shows how to read data from the Flash information area.

```
; get value at info address 60 (FE60h)
ldx FPS, #80 ; enable access to flash info page
ld R0, #FE
ld R1, #60
ldc R2, @RR0 ; R2 now contains the calibration value
```

Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address (TRMADR) Register contains the target address for an access to the trim option bits (Table 86).

Table 86. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Table 101. Watchdog Calibration Low Byte at 007FH (WDTCALL)

Bit	7	6	5	4	3	2	1	0
Field	WDTCALL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 007FH							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] WDTCALL	Watchdog Timer Calibration Low Byte The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second time-out at room temperature and 3.3V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTL with WDT-CALH and WDTL with WDTCALL.

Serialization Data

Table 102. Serial Number at 001C - 001F (S_NUM)

Bit	7	6	5	4	3	2	1	0
Field	S_NUM							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 001C-001F							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] S_NUM	Serial Number Byte The serial number is a unique four-byte binary value. See Table 103.

Table 103. Serialization Data Locations

Info Page Address	Memory Address	Usage
1C	FE1C	Serial Number Byte 3 (most significant).
1D	FE1D	Serial Number Byte 2.
1E	FE1E	Serial Number Byte 1.
1F	FE1F	Serial Number Byte 0 (least significant).

enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

Runtime Counter

The On-Chip Debugger contains a 16-bit Runtime Counter. It counts system clock cycles between Breakpoints. The counter starts counting when the On-Chip Debugger leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the on-chip debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of the Z8 Encore! XP F082A Series device. When this option is enabled, several of the OCD commands are disabled. See Table 109.

Table 110 on page 191 is a summary of the on-chip debugger commands. Each OCD command is described in further detail in the bulleted list following this table. Table 110 also indicates those commands that operate when the device is not in DEBUG Mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Table 109. Debug Command Enable/Disable

Debug Command	Command Byte	Enabled when Not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	–
Reserved	01H	–	–
Read OCD Status Register	02H	Yes	–
Read Runtime Counter	03H	–	–
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit.
Read OCD Control Register	05H	Yes	–

Table 112. Oscillator Configuration and Selection

Clock Source	Characteristics	Required Setup
Internal Precision RC Oscillator	<ul style="list-style-type: none"> • 32.8kHz or 5.53MHz • High accuracy • No external components required 	<ul style="list-style-type: none"> • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator at either 5.53MHz or 32.8kHz
External Crystal/Resonator	<ul style="list-style-type: none"> • 32kHz to 20MHz • Very high accuracy (dependent on crystal or resonator used) • Requires external components 	<ul style="list-style-type: none"> • Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator, wait for it to stabilize and select as system clock (if the XTLDIS option bit has been deasserted, no waiting is required)
External RC Oscillator	<ul style="list-style-type: none"> • 32kHz to 4MHz • Accuracy dependent on external components 	<ul style="list-style-type: none"> • Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator and select as system clock
External Clock Drive	<ul style="list-style-type: none"> • 0 to 20MHz • Accuracy dependent on external clock source 	<ul style="list-style-type: none"> • Write GPIO registers to configure PB3 pin for external clock function • Unlock and write OSCCTL to select external system clock • Apply external clock signal to GPIO
Internal Watchdog Timer Oscillator	<ul style="list-style-type: none"> • 10kHz nominal • Low accuracy; no external components required • Very low power consumption 	<ul style="list-style-type: none"> • Enable WDT if not enabled and wait until WDT Oscillator is operating • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator

! Caution: Unintentional accesses to the Oscillator Control Register can actually stop the chip by switching to a nonfunctioning oscillator. To prevent this condition, the oscillator control block employs a register unlocking/locking scheme.

OSC Control Register Unlocking/Locking

To write the Oscillator Control Register, unlock it by making two writes to the OSCCTL Register with the values `E7H` followed by `18H`. A third write to the OSCCTL Register changes the value of the actual register and returns the register to a locked state. Any other sequence of Oscillator Control Register writes has no effect. The values written to unlock the register must be ordered correctly, but are not necessarily consecutive. It is possible to write to or read from other registers within the unlocking/locking operation.

Table 121. Bit Manipulation Instructions

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
TCM	dst, src	Test Complement Under Mask
TCMX	dst, src	Test Complement Under Mask using Extended Addressing
TM	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

Table 122. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses

Table 123. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	Halt Mode
NOP	—	No Operation

AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

Table 133. AC Characteristics

		$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)			
Symbol	Parameter	Minimum	Maximum	Units	Conditions
F _{SYSCLK}	System Clock Frequency	–	20.0	MHz	Read-only from Flash memory
		0.032768	20.0	MHz	Program or erasure of the Flash memory
F _{XTAL}	Crystal Oscillator Frequency	–	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external clock driver
T _{XIN}	System Clock Period	50	–	ns	T _{CLK} = 1/F _{sysclk}
T _{XINH}	System Clock High Time	20	30	ns	T _{CLK} = 50 ns
T _{XINL}	System Clock Low Time	20	30	ns	T _{CLK} = 50 ns
T _{XINR}	System Clock Rise Time	–	3	ns	T _{CLK} = 50 ns
T _{XINF}	System Clock Fall Time	–	3	ns	T _{CLK} = 50 ns

Table 134. Internal Precision Oscillator Electrical Characteristics

		$V_{DD} = 2.7V \text{ to } 3.6V$ $T_A = -40^{\circ}C \text{ to } +105^{\circ}C$ (unless otherwise stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F _{IPO}	Internal Precision Oscillator Frequency (High Speed)		5.53		MHz	V _{DD} = 3.3V T _A = 30°C
F _{IPO}	Internal Precision Oscillator Frequency (Low Speed)		32.7		kHz	V _{DD} = 3.3V T _A = 30°C
F _{IPO}	Internal Precision Oscillator Error		±1	±4	%	
T _{IPOST}	Internal Precision Oscillator Startup Time		3		μs	