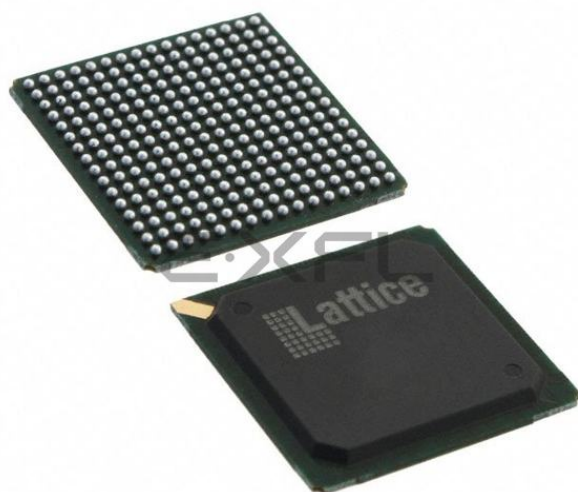




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5f256c

Table 2-12. PIO Signals List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block flip-flops
CLK0, CLK1	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs in left, right and bottom edges contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-29 shows the diagram of the input register block for left, right and bottom edges. The input register block for the top edge contains one memory element to register the input signal as shown in Figure 2-30. The following description applies to the input register block for PIOs in the left, right and bottom edges of the device.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In DDR Mode, two registers are used to sample the data on the positive and negative edges of the DQS signal, creating two data streams, D0 and D1. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-31. Output and Tristate Block for Left, Right and Bottom Edges

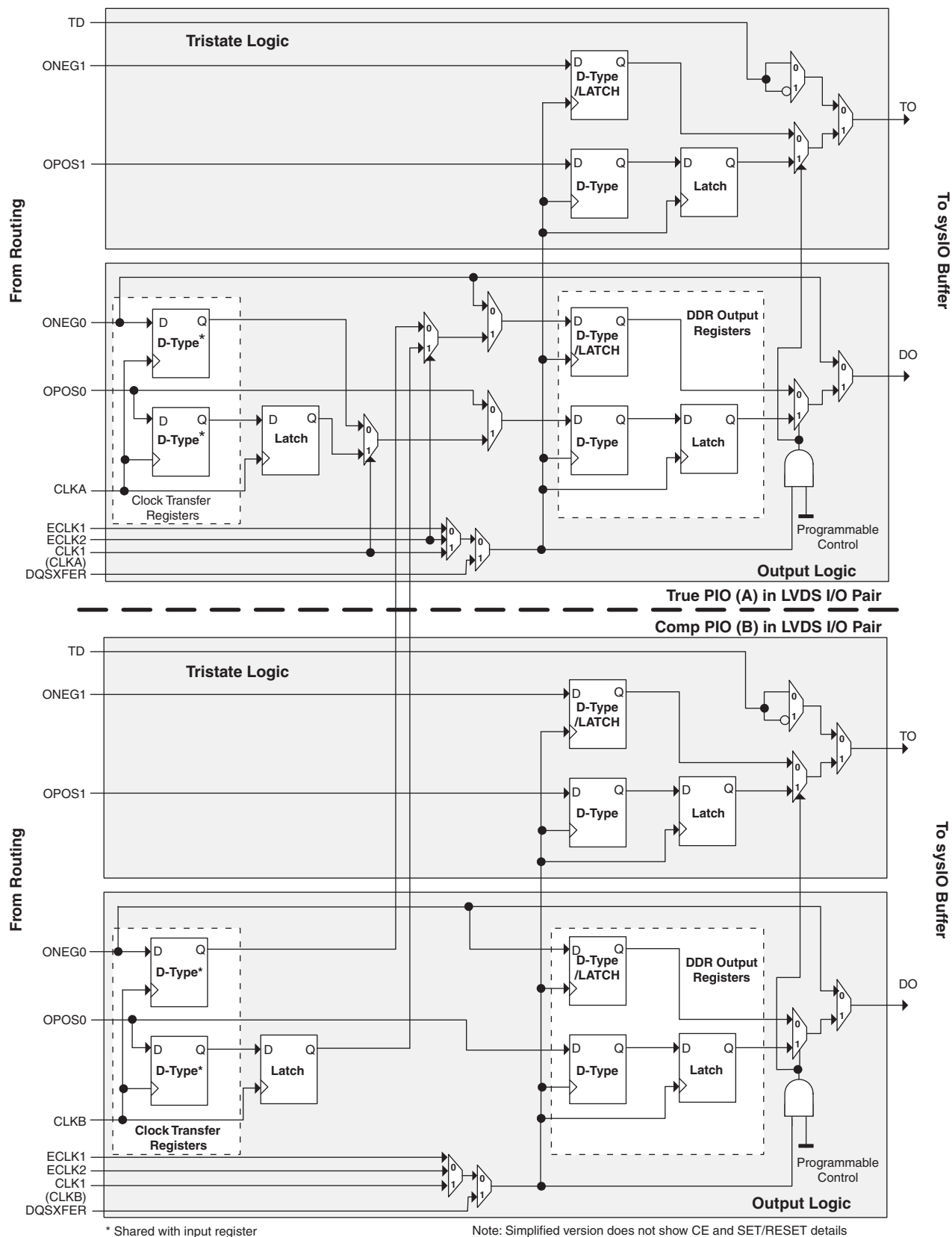
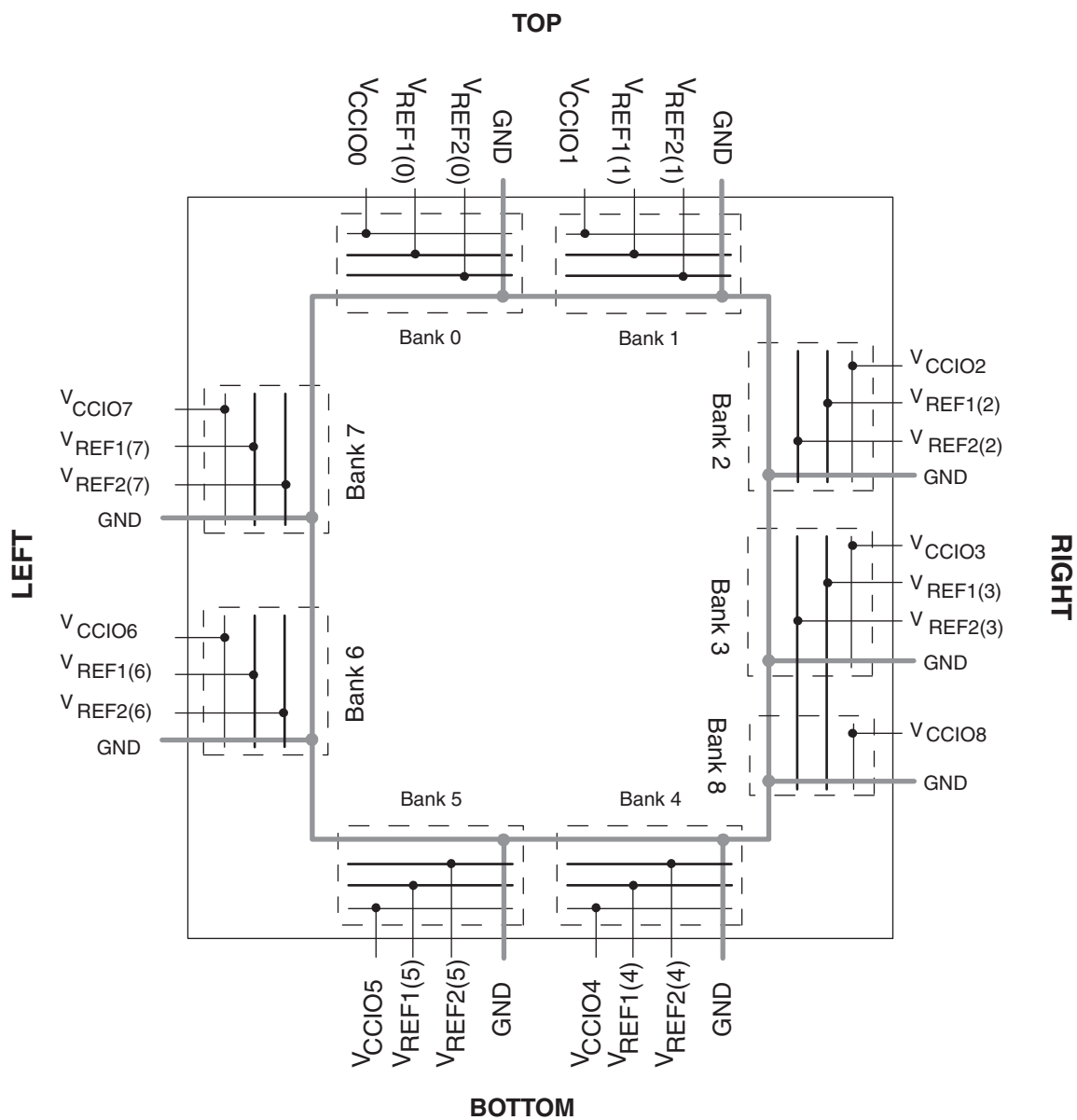


Figure 2-37. LatticeECP2 Banks



SERDES Power Supply Requirements (LatticeECP2M Family Only)¹

Over Recommended Operating Conditions

Symbol	Description	Typ. ²	Units
Standby (Power Down)			
I _{CCTX-SB}	V _{CCTX} current (per channel)	10	μA
I _{CCR_X-SB}	V _{CCR_X} current (per channel)	75	μA
I _{CCIB-SB}	Input buffer current (per channel)	0	μA
I _{CCOB-SB}	Output buffer current (per channel)	0	μA
I _{CCP-SB}	SERDES PLL current (per quad)	30	μA
I _{CCAX33-SB}	SERDES termination current (per quad)	10	μA
Operating (Data Rate = 3.125 Gbps)			
I _{CCTX-OP}	V _{CCTX} current (per channel)	19	mA
I _{CCR_X-OP}	V _{CCR_X} current (per channel)	34	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	mA
I _{CCOB-OP}	Output buffer current (per channel)	13	mA
I _{CCP-OP}	SERDES PLL current (per quad)	26	mA
I _{CCAX33-OP}	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.

2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power¹

Symbol	Description	Typ. ²	Units
P _{S-1CH-31}	SERDES power (one channel @ 3.125 Gbps)	90	mW
P _{S-1CH-25}	SERDES power (one channel @ 2.5 Gbps)	87	mW
P _{S-1CH-12}	SERDES power (one channel @ 1.25 Gbps)	86	mW
P _{S-1CH-02}	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

2. Typical values measured at 25°C and 1.2V.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

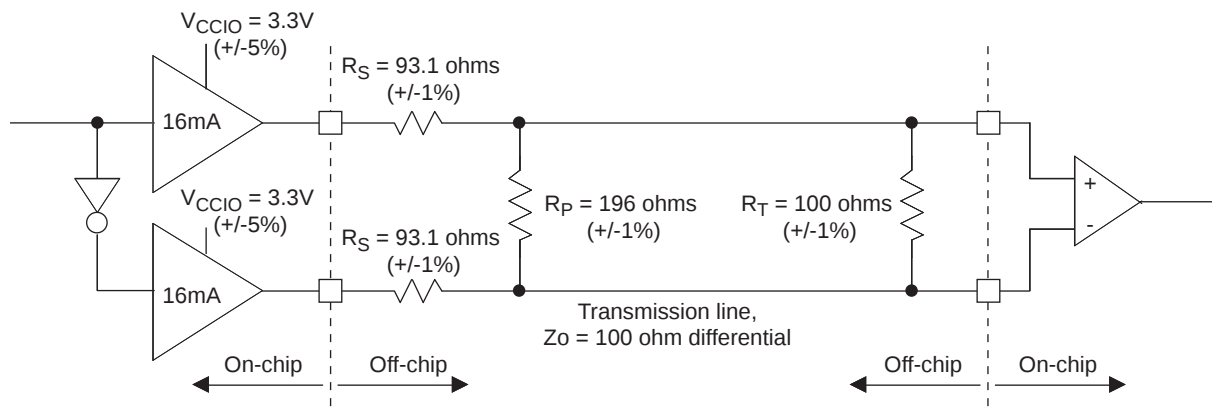


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply ($\pm 5\%$)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor ($\pm 1\%$)	93	Ω
R_P	Driver Parallel Resistor ($\pm 1\%$)	196	Ω
R_T	Receiver Termination ($\pm 1\%$)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F19	PR5A	2		T	PR7A	2	RDQ8	T	
D20	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
F18	PR3B	2		C	PR5B	2	RDQ8	C	
VCCIO	VCCIO2	2			VCCIO2	2			
C21	NC	-			PR4B	2	RDQ8	C (LVDS)*	
F16	PR3A	2		T	PR5A	2	RDQ8	T	
C22	NC	-			PR4A	2	RDQ8	T (LVDS)*	
-	-	-			GNDIO	-			
D19	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
E19	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
B21	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
B22	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
GNDIO	GNDIO1	-			GNDIO1	-			
D18	PT53B	1		C	PT62B	1		C	
C20	PT54B	1		C	PT63B	1		C	
E18	PT53A	1		T	PT62A	1		T	
C19	PT54A	1		T	PT63A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D17	PT51B	1		C	PT60B	1		C	
B20	PT52B	1		C	PT61B	1		C	
C18	PT51A	1		T	PT60A	1		T	
A19	PT52A	1		T	PT61A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
A18	PT49B	1		C	PT58B	1		C	
A21	PT50B	1		C	PT59B	1		C	
B18	PT49A	1		T	PT58A	1		T	
A20	PT50A	1		T	PT59A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D16	PT47B	1		C	PT56B	1		C	
G16	PT48B	1		C	PT57B	1		C	
E16	PT47A	1		T	PT56A	1		T	
G15	PT48A	1		T	PT57A	1		T	
C17	PT46B	1		C	PT55B	1		C	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT46A	1		T	PT55A	1		T	
A17	PT44B	1		C	PT53B	1		C	
B17	PT45B	1		C	PT54B	1		C	
A16	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
B16	PT45A	1		T	PT54A	1		T	
E15	PT42B	1		C	PT51B	1		C	
C15	PT43B	1		C	PT52B	1		C	
F15	PT42A	1		T	PT51A	1		T	
D15	PT43A	1		T	PT52A	1		T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U1	PL53A	6	LDQ50	T	PL66A	6	LDQ63	T	
V1	PL53B	6	LDQ50	C	PL66B	6	LDQ63	C	
GND	GNDIO6	-			GNDIO6	-			
P3	PL54A	6	LDQ58	T (LVDS)*	PL67A	6	LDQ71	T (LVDS)*	
R3	PL54B	6	LDQ58	C (LVDS)*	PL67B	6	LDQ71	C (LVDS)*	
R4	PL55A	6	LDQ58	T	PL68A	6	LDQ71	T	
U2	PL55B	6	LDQ58	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
V2	PL56A	6	LDQ58	T (LVDS)*	PL69A	6	LDQ71	T (LVDS)*	
W2	PL56B	6	LDQ58	C (LVDS)*	PL69B	6	LDQ71	C (LVDS)*	
T6	PL57A	6	LDQ58	T	PL70A	6	LDQ71	T	
R5	PL57B	6	LDQ58	C	PL70B	6	LDQ71	C	
GND	GNDIO6	-			GNDIO6	-			
R6	PL58A	6	LDQS58	T (LVDS)*	PL71A	6	LDQS71	T (LVDS)*	
R7	PL58B	6	LDQ58	C (LVDS)*	PL71B	6	LDQ71	C (LVDS)*	
W1	PL59A	6	LDQ58	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y2	PL59B	6	LDQ58	C	PL72B	6	LDQ71	C	
Y1	PL60A	6	LLM0_GDLLT_IN_A**/LDQ58	T (LVDS)*	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*	
AA2	PL60B	6	LLM0_GDLLC_IN_A**/LDQ58	C (LVDS)*	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*	
T5	PL61A	6	LLM0_GDLLT_FB_A/LDQ58	T	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T	
GND	GNDIO6	-			GNDIO6	-			
T7	PL61B	6	LLM0_GDLLC_FB_D/LDQ58	C	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C	
R8	VCCPLL	6			VCCPLL	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
U3	PL63A	6	LLM0_GPLLT_IN_A**/LDQ67	T (LVDS)*	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*	
U4	PL63B	6	LLM0_GPLLC_IN_A**/LDQ67	C (LVDS)*	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*	
V3	PL64A	6	LLM0_GPLLT_FB_A/LDQ67	T	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T	
U5	PL64B	6	LLM0_GPLLC_FB_A/LDQ67	C	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C	
V4	PL65A	6	LDQ67	T (LVDS)*	PL78A	6	LDQ80	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
V5	PL65B	6	LDQ67	C (LVDS)*	PL78B	6	LDQ80	C (LVDS)*	
Y3	PL66A	6	LDQ67	T	PL79A	6	LDQ80	T	
Y4	PL66B	6	LDQ67	C	PL79B	6	LDQ80	C	
W3	PL67A	6	LDQS67	T (LVDS)*	PL80A	6	LDQS80	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
W4	PL67B	6	LDQ67	C (LVDS)*	PL80B	6	LDQ80	C (LVDS)*	
AA1	PL68A	6	LDQ67	T	PL81A	6	LDQ80	T	
AB1	PL68B	6	LDQ67	C	PL81B	6	LDQ80	C	
VCCIO	VCCIO6	6			VCCIO6	6			
U8	PL69A	6	LDQ67	T (LVDS)*	PL82A	6	LDQ80	T (LVDS)*	
U7	PL69B	6	LDQ67	C (LVDS)*	PL82B	6	LDQ80	C (LVDS)*	
V8	PL70A	6	LDQ67	T	PL83A	6	LDQ80	T	
U6	PL70B	6	LDQ67	C	PL83B	6	LDQ80	C	
GND	GNDIO6	-			GNDIO6	-			
W6	PL71A	6	LDQ75	T (LVDS)*	PL84A	6	LDQ88	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W5	PL71B	6	LDQ75	C (LVDS)*	PL84B	6	LDQ88	C (LVDS)*	
AC1	PL72A	6	LDQ75	T	PL85A	6	LDQ88	T	
AD1	PL72B	6	LDQ75	C	PL85B	6	LDQ88	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y6	PL73A	6	LDQ75	T (LVDS)*	PL86A	6	LDQ88	T (LVDS)*	
Y5	PL73B	6	LDQ75	C (LVDS)*	PL86B	6	LDQ88	C (LVDS)*	
AE2	PL74A	6	LDQ75	T	PL87A	6	LDQ88	T	
AD2	PL74B	6	LDQ75	C	PL87B	6	LDQ88	C	
GND	GNDIO6	-			GNDIO6	-			
AB3	PL75A	6	LDQS75	T (LVDS)*	PL88A	6	LDQS88	T (LVDS)*	
AB2	PL75B	6	LDQ75	C (LVDS)*	PL88B	6	LDQ88	C (LVDS)*	
W7	PL76A	6	LDQ75	T	PL89A	6	LDQ88	T	
VCCIO	VCCIO6	6			VCCIO6	6			
W8	PL76B	6	LDQ75	C	PL89B	6	LDQ88	C	
Y7	PL77A	6	LDQ75	T (LVDS)*	PL90A	6	LDQ88	T (LVDS)*	
Y8	PL77B	6	LDQ75	C (LVDS)*	PL90B	6	LDQ88	C (LVDS)*	
AC2	PL78A	6	LDQ75	T	PL91A	6	LDQ88	T	
GND	GNDIO6	-			GNDIO6	-			
AD3	PL78B	6	LDQ75	C	PL91B	6	LDQ88	C	
AC3	TCK	-			TCK	-			
AA8	TDI	-			TDI	-			
AB4	TMS	-			TMS	-			
AA5	TDO	-			TDO	-			
AB5	VCCJ	-			VCCJ	-			
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
GND	GNDIO5	-			GNDIO5	-			
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G19	GND	-			GND	-			
G4	GND	-			GND	-			
H10	GND	-			GND	-			
H13	GND	-			GND	-			
J14	GND	-			GND	-			
J9	GND	-			GND	-			
K10	GND	-			GND	-			
K11	GND	-			GND	-			
K12	GND	-			GND	-			
K13	GND	-			GND	-			
K15	GND	-			GND	-			
K20	GND	-			GND	-			
K3	GND	-			GND	-			
K8	GND	-			GND	-			
L10	GND	-			GND	-			
L11	GND	-			GND	-			
L12	GND	-			GND	-			
L13	GND	-			GND	-			
M10	GND	-			GND	-			
M11	GND	-			GND	-			
M12	GND	-			GND	-			
M13	GND	-			GND	-			
N10	GND	-			GND	-			
N11	GND	-			GND	-			
N12	GND	-			GND	-			
N13	GND	-			GND	-			
N15	GND	-			GND	-			
N20	GND	-			GND	-			
N3	GND	-			GND	-			
N8	GND	-			GND	-			
P14	GND	-			GND	-			
P9	GND	-			GND	-			
R10	GND	-			GND	-			
R13	GND	-			GND	-			
T19	GND	-			GND	-			
T4	GND	-			GND	-			
W16	GND	-			GND	-			
W2	GND	-			GND	-			
W21	GND	-			GND	-			
W7	GND	-			GND	-			
Y10	GND	-			GND	-			
Y13	GND	-			GND	-			
D15	NC	-			NC	-			
G14	NC	-			NC	-			
G15	NC	-			NC	-			
D14	NC	-			NC	-			
E15	NC	-			NC	-			
E14	NC	-			NC	-			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
P8	PL45A	6	LDQ48	T	PL49A	6	LDQ52	T	
R6	PL45B	6	LDQ48	C	PL49B	6	LDQ52	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T1	PL46A	6	LDQ48	T (LVDS)*	PL50A	6	LDQ52	T*	
U1	PL46B	6	LDQ48	C (LVDS)*	PL50B	6	LDQ52	C*	
R7	PL47A	6	LDQ48	T	PL51A	6	LDQ52	T	
T5	PL47B	6	LDQ48	C	PL51B	6	LDQ52	C	
GNDIO	GNDIO6	-			GNDIO6	-			
U3	PL48A	6	LDQS48	T (LVDS)*	PL52A	6	LDQS52	T*	
U4	PL48B	6	LDQ48	C (LVDS)*	PL52B	6	LDQ52	C*	
U5	PL49A	6	LDQ48	T	PL53A	6	LDQ52	T	
VCCIO	VCCIO6	6			VCCIO6	6			
U6	PL49B	6	LDQ48	C	PL53B	6	LDQ52	C	
U2	PL50A	6	LDQ48	T (LVDS)*	PL54A	6	LDQ52	T*	
V1	PL50B	6	LDQ48	C (LVDS)*	PL54B	6	LDQ52	C*	
W2	PL51A	6	LDQ48	T	PL55A	6	LDQ52	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V2	PL51B	6	LDQ48	C	PL55B	6	LDQ52	C	
V4	PL55A	6	LDQ57	T (LVDS)*	PL59A	6		T*	
VCCIO	VCCIO6	6			VCCIO6	6			
V3	PL55B	6	LDQ57	C (LVDS)*	PL59B	6		C*	
-	-	-			GNDIO6	-			
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	PL62A	6	LLM0_GPLLT_IN_A	T*	
GNDIO	GNDIO6	-			GNDIO6	-			
W3	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	PL62B	6	LLM0_GPLLC_IN_A	C*	
W1	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	PL63A	6	LLM0_GPLLT_FB_A	T	
Y1	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	PL63B	6	LLM0_GPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AA1	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*	PL64A	6	LLM0_GDLLT_IN_A	T*	
AB1	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	PL64B	6	LLM0_GDLLC_IN_A	C*	
U7	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T	PL65A	6	LLM0_GDLLT_FB_A	T	
V6	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	PL65B	6	LLM0_GDLLC_FB_A	C	
GNDIO	GNDIO6	-			GNDIO6	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
W5	PL62A	6	LDQ66	T (LVDS)*	PL67A	6	LDQ71	T*	
Y4	PL62B	6	LDQ66	C (LVDS)*	PL67B	6	LDQ71	C*	
U8	PL63A	6	LDQ66	T	PL68A	6	LDQ71	T	
W6	PL63B	6	LDQ66	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y3	PL64A	6	LDQ66	T (LVDS)*	PL69A	6	LDQ71	T*	
AA3	PL64B	6	LDQ66	C (LVDS)*	PL69B	6	LDQ71	C*	
V7	NC	-			PL70A	6	LDQ71	T	
Y5	PL65B	6	LDQ66	C	PL70B	6	LDQ71	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB2	PL66A	6	LDQS66	T (LVDS)*	PL71A	6	LDQS71	T*	
AA4	PL66B	6	LDQ66	C (LVDS)*	PL71B	6	LDQ71	C*	
Y6	PL67A	6	LDQ66	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
J16	PT51B	1		C	PT60B	1		C	
G15	PT51A	1		T	PT60A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT50B	1		C	PT59B	1		C	
D16	PT50A	1		T	PT59A	1		T	
J15	PT49B	1		C	PT58B	1		C	
H15	PT49A	1		T	PT58A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A15	PT48B	1	VREF2_1	C	PT57B	1	VREF2_1	C	
B15	PT48A	1	VREF1_1	T	PT57A	1	VREF1_1	T	
F15	PT47B	1	PCLKC1_0	C	PT56B	1	PCLKC1_0	C	
E16	PT47A	1	PCLKT1_0	T	PT56A	1	PCLKT1_0	T	
C15	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
D15	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T	
C14	PT45B	0	VREF2_0	C	PT54B	0	VREF2_0	C	
E15	PT45A	0	VREF1_0	T	PT54A	0	VREF1_0	T	
G14	PT44B	0		C	PT53B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J14	PT44A	0		T	PT53A	0		T	
F14	PT43B	0		C	PT52B	0		C	
H14	PT43A	0		T	PT52A	0		T	
A14	PT42B	0		C	PT51B	0		C	
B14	PT42A	0		T	PT51A	0		T	
D13	PT41B	0		C	PT50B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F13	PT41A	0		T	PT50A	0		T	
G13	PT40B	0		C	PT49B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J11	PT40A	0		T	PT49A	0		T	
D4	PT38B	0		C	PT47B	0		C	
D5	PT38A	0		T	PT47A	0		T	
E5	PT37B	0		C	PT46B	0		C	
F6	PT37A	0		T	PT46A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT34B	0		C	PT43B	0		C	
D8	PT34A	0		T	PT43A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
J13	PT32B	0		C	PT41B	0		C	
G11	PT32A	0		T	PT41A	0		T	
H13	PT31B	0		C	PT40B	0		C	
H12	PT31A	0		T	PT40A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
E8	PT30B	0		C	PT39B	0		C	
D9	PT30A	0		T	PT39A	0		T	
D12	PT28B	0		C	PT37B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AF11	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AJ14	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4		
AK14	PB67B	4	PCLKC4_0/BDQ69	C
AK15	PB68A	4	VREF2_4/BDQ69	T
AK16	PB68B	4	VREF1_4/BDQ69	C
AF18	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-		
AD16	PB69B	4	BDQ69	C
AJ15	PB70A	4	BDQ69	T
AG16	PB70B	4	BDQ69	C
AE17	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4		
AC17	PB71B	4	BDQ69	C
AH16	PB72A	4	BDQ69	T
AK17	PB72B	4	BDQ69	C
AG20	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-		
AG21	PB73B	4	BDQ69	C
AG18	PB74A	4	BDQ78	T
AJ16	PB74B	4	BDQ78	C
AF21	PB75A	4	BDQ78	T
AG22	PB75B	4	BDQ78	C
AD17	PB76A	4	BDQ78	T
AF19	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
AH17	PB80A	4	BDQ78	T
AJ17	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4		
AF26	PB82A	4	BDQ78	T
AE25	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-		
AD24	PB92A	4	BDQ96	T
AE24	PB92B	4	BDQ96	C
AD18	PB93A	4	BDQ96	T
AC18	PB93B	4	BDQ96	C
AE18	PB94A	4	BDQ96	T
AG19	PB94B	4	BDQ96	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C29	URC_SQ_VCCR1	12		
B28	URC_SQ_HDINN1	12		C
C28	URC_SQ_VCCIB1	12		
A28	URC_SQ_HDINP1	12		T
B24	URC_SQ_VCCAUX33	12		
E24	URC_SQ_REFCLKN	12		C
D24	URC_SQ_REFCLKP	12		T
C24	URC_SQ_VCCP	12		
A20	URC_SQ_HDINP2	12		T
C20	URC_SQ_VCCIB2	12		
B20	URC_SQ_HDINN2	12		C
C19	URC_SQ_VCCR2	12		
A23	URC_SQ_HDOUTP2	12		T
C23	URC_SQ_VCCOB2	12		
B23	URC_SQ_HDOUTN2	12		C
C22	URC_SQ_VCCTX2	12		
B22	URC_SQ_HDOUTN3	12		C
A21	URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCR3	12		
D23	PT100B	1		C
GNDIO	GNDIO1	-		
E21	PT100A	1		T
D26	PT99B	1		C
E26	PT99A	1		T
E23	PT98B	1		C
VCCIO	VCCIO1	1		
G22	PT98A	1		T
-	-	-		
D22	PT97B	1		C
F21	PT97A	1		T
G18	PT96B	1		C
H18	PT96A	1		T
D20	PT95B	1		C
GNDIO	GNDIO1	-		
D21	PT95A	1		T
E20	PT94B	1		C
VCCIO	VCCIO1	1		
E19	PT94A	1		T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D19	PT93B	1		C
E18	PT93A	1		T
D18	PT92B	1		C
C17	PT92A	1		T
A17	PT91B	1		C
B17	PT91A	1		T
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
J18	PT75B	1		C
J19	PT75A	1		T
H17	PT74B	1		C
J17	PT74A	1		T
F18	PT73B	1		C
F17	PT73A	1		T
GNDIO	GNDIO1	-		
A16	PT72B	1		C
B16	PT72A	1		T
G17	PT71B	1		C
G16	PT71A	1		T
VCCIO	VCCIO1	1		
H16	PT70B	1		C
F16	PT70A	1		T
J16	PT69B	1		C
G15	PT69A	1		T
GNDIO	GNDIO1	-		
C16	PT68B	1		C
D16	PT68A	1		T
J15	PT67B	1		C
H15	PT67A	1		T
VCCIO	VCCIO1	1		
A15	PT66B	1	VREF2_1	C
B15	PT66A	1	VREF1_1	T
F15	PT65B	1	PCLKC1_0	C
E16	PT65A	1	PCLKT1_0	T
C15	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
D15	PT64A	0	PCLKT0_0	T
C14	PT63B	0	VREF2_0	C
E15	PT63A	0	VREF1_0	T
G14	PT62B	0		C
VCCIO	VCCIO0	0		
J14	PT62A	0		T
F14	PT61B	0		C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
H14	PT61A	0		T
A14	PT60B	0		C
B14	PT60A	0		T
D13	PT59B	0		C
GNDIO	GNDIO0	-		
F13	PT59A	0		T
G13	PT58B	0		C
VCCIO	VCCIO0	0		
J11	PT58A	0		T
D4	PT57B	0		
D5	PT56A	0		
E5	PT55B	0		C
F6	PT55A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F7	PT52B	0		C
D8	PT52A	0		T
GNDIO	GNDIO0	-		
J13	PT50B	0		C
G11	PT50A	0		T
H13	PT49B	0		C
H12	PT49A	0		T
VCCIO	VCCIO0	0		
E8	PT48B	0		C
D9	PT48A	0		T
D12	PT46B	0		C
GNDIO	GNDIO0	-		
E13	PT46A	0		T
VCCIO	VCCIO0	0		
GNDIO	GNDIO0	-		
J12	PT31B	0		C
-	-	-		
VCCIO	VCCIO0	0		
H10	PT31A	0		T
E12	PT30B	0		C
D11	PT30A	0		T
H11	PT29B	0		C
F11	PT29A	0		T
C13	ULC_SQ_VCCR0	11		
A12	ULC_SQ_HDINP0	11		T
B13	ULC_SQ_VCCIB0	11		
B12	ULC_SQ_HDINN0	11		C
C10	ULC_SQ_VCCTX0	11		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AN29	LRC_SQ_VCCR2	13			LRC_SQ_VCCR2	13		
AM28	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AL27	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AM29	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AL29	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AL30	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AK30	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AK29	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AM30	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AL31	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AM31	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AN30	LRC_SQ_VCCR1	13			LRC_SQ_VCCR1	13		
AP30	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T
AL32	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AP31	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AN31	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AP32	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AM34	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AP33	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AN32	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AM32	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AN34	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AM33	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AN33	LRC_SQ_VCCR0	13			LRC_SQ_VCCR0	13		
AH28	CFG2	8			CFG2	8		
AD24	CFG1	8			CFG1	8		
AJ29	CFG0	8			CFG0	8		
AF25	PROGRAMN	8			PROGRAMN	8		
AJ28	CCLK	8			CCLK	8		
AE25	INITN	8			INITN	8		
AK31	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE24	WRITEN***	8			WRITEN***	8		
AJ30	CS1N***	8			CS1N***	8		
AD25	CSN***	8			CSN***	8		
AG29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG28	D1***	8			D1***	8		
AG30	D2***	8			D2***	8		
AH29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF26	D4***	8			D4***	8		
AH30	D5***	8			D5***	8		
AE26	D6***	8			D6***	8		
AJ31	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG27	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AK32	DO/CSN/CSPI1N***	8			DO/CSN/CSPI1N***	8		
AK33	BUSY/SISPI***	8			BUSY/SISPI***	8		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK12	NC	-			NC	-		
AK24	NC	-			NC	-		
AK25	NC	-			NC	-		
AK26	NC	-			NC	-		
AK4	NC	-			NC	-		
AK9	NC	-			NC	-		
AL11	NC	-			NC	-		
AL12	NC	-			NC	-		
AL34	NC	-			NC	-		
AM10	NC	-			NC	-		
AM11	NC	-			NC	-		
AM13	NC	-			NC	-		
AM25	NC	-			NC	-		
AN10	NC	-			NC	-		
AN11	NC	-			NC	-		
AN12	NC	-			NC	-		
AN13	NC	-			NC	-		
AN24	NC	-			NC	-		
AN25	NC	-			NC	-		
AP11	NC	-			NC	-		
AP12	NC	-			NC	-		
AP24	NC	-			NC	-		
B10	NC	-			NC	-		
B11	NC	-			NC	-		
B12	NC	-			NC	-		
B13	NC	-			NC	-		
B22	NC	-			NC	-		
B23	NC	-			NC	-		
B24	NC	-			NC	-		
B25	NC	-			NC	-		
C10	NC	-			NC	-		
C11	NC	-			NC	-		
C13	NC	-			NC	-		
C22	NC	-			NC	-		
C24	NC	-			NC	-		
C25	NC	-			NC	-		
D1	NC	-			NC	-		
D15	NC	-			NC	-		
D24	NC	-			NC	-		
D34	NC	-			NC	-		
E10	NC	-			NC	-		
E24	NC	-			NC	-		
E25	NC	-			NC	-		
E26	NC	-			NC	-		
E3	NC	-			NC	-		
E31	NC	-			NC	-		
E32	NC	-			NC	-		
E33	NC	-			NC	-		
E34	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100