Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	297
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5fn484c

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit

- Subtraction 2-bit

- Add/Subtract 2-bit using dynamic control

- Up counter 2-bit

- Down counter 2-bit

- Up/Down counter with Async clear

- Up/Down counter with preload (sync)

- Ripple mode multiplier building block

- Multiplier support

- Comparator functions of A and B inputs
    - A greater-than-or-equal-to B
    - A not-equal-to B
    - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP2/M devices, please see the list of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

SERDES and PCS (Physical Coding Sublayer)

LatticeECP2M devices feature up to 16 channels of embedded SERDES arranged in quads at the corners of the devices. Figure 2-39 shows the position of the quad blocks in relation to the PFU array for LatticeECP2M70 and LatticeECP2M100 devices. Table 2-15 shows the location of Quads for all the devices.

Each quad contains four dedicated SERDES (Ch0 to Ch3) for high-speed, full-duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains digital logic to support an array of popular data protocols. PCS also contains logic to the interface to FPGA core.

Figure 2-39. SERDES Quads (LatticeECP2M70/LatticeECP2M100)

ULC SERDES Quad   **URC SERDES Quad**

| Ch 3 | Ch 2 | | Ch 1 | Ch 0 |

PCS Digital Logic

| Ch 3 | Ch 2 | | Ch 1 | Ch 0 |

PCS Digital Logic

PCS Digital Logic

| Ch 3 | Ch 2 | | Ch 1 | Ch 0 |

PCS Digital Logic

| Ch 3 | Ch 2 | | Ch 1 | Ch 0 |

LLC SERDES Quad   **LRC SERDES Quad**
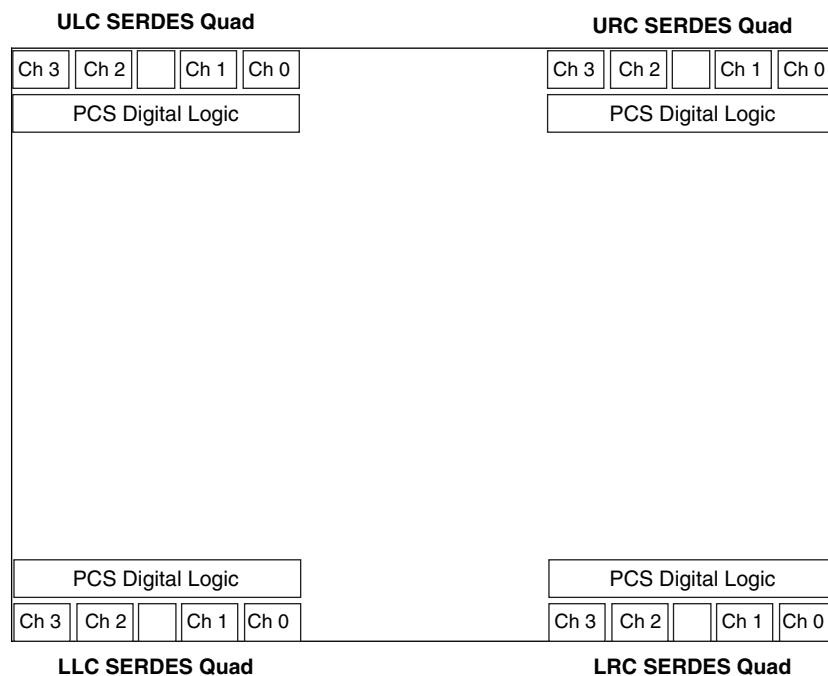
Table 2-15. Available SERDES Quads per LatticeECP2M Devices

Device	URC Quad	ULC Quad	LRC Quad	LLC Quad
ECP2M20	Available	—	—	—
ECP2M35	Available	—	—	—
ECP2M50	Available	—	Available	—
ECP2M70	Available	Available	Available	Available
ECP2M100	Available	Available	Available	Available

SERDES Block

A differential receiver receives the serial encoded data stream, equalizes the signal, extracts the buried clock and de-serializes the data-stream before passing the 8- or 10-bit data to the PCS logic. The transmit channel receives the parallel (8- or 10-bit) encoded data, serializes the data and transmits the serial bit stream through the differential buffers. There is a single transmit clock per quad. Figure 2-40 shows a single channel SERDES and its interface to the PCS logic. Each SERDES receiver channel provides a recovered clock to the PCS block and to the FPGA core logic.

LatticeECP2 Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5, 6, 7]	Units
I_{CC}	Core Power Supply Current	ECP2-6	34	mA
		ECP2-12	54	mA
		ECP2-20	82	mA
		ECP2-35	135	mA
		ECP2-50	187	mA
		ECP2-70	267	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	30	mA
		ECP2-12	30	mA
		ECP2-20	30	mA
		ECP2-35	30	mA
		ECP2-50	30	mA
		ECP2-70	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.
2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. $T_J = 25^{\circ}C$, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Figure 3-6. SPI4.2 Parameters

Transmit Parameters

Receiver Parameters
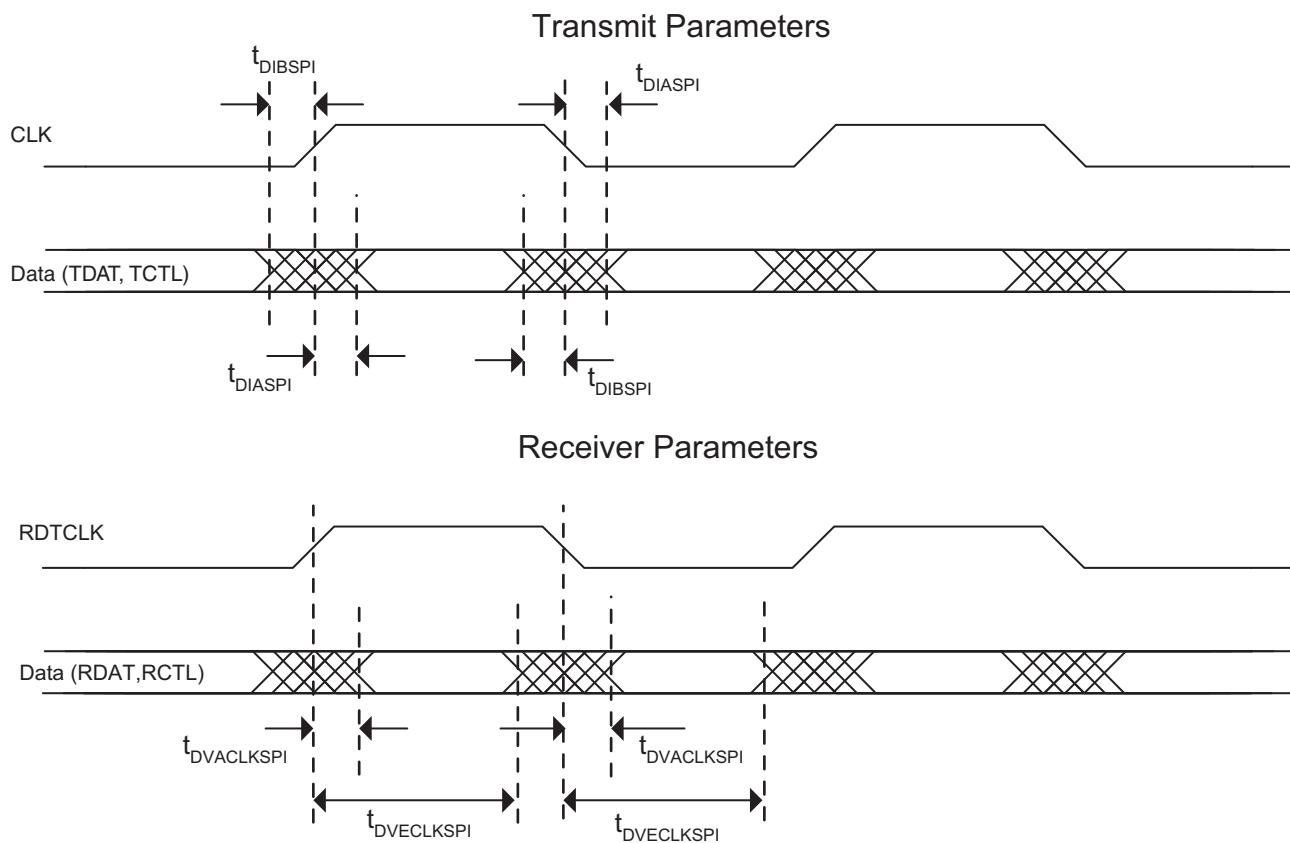
LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTL33_4mA	LVTTL 4mA drive	0.52	0.60	0.68	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.08	0.09	ns
LVTTL33_12mA	LVTTL 12mA drive	0.04	0.04	0.05	ns
LVTTL33_16mA	LVTTL 16mA drive	0.03	0.02	0.02	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100

Pin Type		LFE2M50			LFE2M70		LFE2M100	
		484 fpBGA	672 fpBGA	900 fpBGA	900 fpBGA	1152 fpBGA	900 fpBGA	1152 fpBGA
Single Ended User I/O		270	372	410	416	436	416	520
Differential Pair User I/O		135	185	205	208	218	207	260
Configuration	TAP Pins	5	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7	7
Non Configuration	Muxed Pins	69	72	72	75	76	74	78
	Dedicated Pins	3	3	3	3	3	3	3
VCC		16	20	62	44	44	44	44
VCCAUX		8	26	18	16	12	16	12
VCCPLL		4	8	4	4	4	4	4
VCCIO	Bank0	4	5	6	6	7	6	7
	Bank1	3	4	6	6	7	6	7
	Bank2	4	5	9	9	9	9	9
	Bank3	4	5	9	9	9	9	9
	Bank4	4	4	6	6	7	6	7
	Bank5	4	5	6	6	7	6	7
	Bank6	4	5	9	9	9	9	9
	Bank7	4	5	9	9	9	9	9
	Bank8	2	2	2	2	2	2	2
GND, GND0 to GND7		57	80	122	122	134	122	134
NC		31	35	121	63	283	63	199
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	36/18	63/31	56/28	34/17	46/23	34/17	54/27
	Bank1	18/9	18/9	36/18	42/21	34/17	42/21	44/22
	Bank2	30/15	50/25	54/27	70/35	72/36	70/35	80/40
	Bank3	36/18	43/21	44/22	60/30	64/32	60/30	80/40
	Bank4	42/21	24/12	38/19	38/19	40/20	38/19	44/22
	Bank5	28/14	60/30	58/29	40/20	40/20	40/20	46/23
	Bank6	40/20	54/27	60/30	62/31	66/33	62/31	82/41
	Bank7	40/20	60/30	64/32	70/35	74/37	70/35	90/45
	Bank8	0/0	0/0	0/0	0/0	0/0	0/0	0/0
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0	0
	Bank2 (Right Edge)	7	12	13	17	18	17	20
	Bank3 (Right Edge)	9	11	11	15	16	15	20
	Bank4 (Bottom Edge)	0	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0	0
	Bank6 (Left Edge)	10	14	15	15	16	15	20
	Bank7 (Left Edge)	10	15	17	17	18	17	22
	Bank8 (Right Edge)	0	0	0	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

	LFE2-6E/SE				LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

			LFE2-20E/SE		
Ball Number	**Ball Number**	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
J1	J1	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
K3	K3	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
J2	J2	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
GND	GND	GNDIO6	-		
L2	L2	PL38A	6	LDQ42	T (LVDS)*
K2	K2	PL39A	6	LDQ42	T
L3	L3	PL38B	6	LDQ42	C (LVDS)*
K1	K1	PL39B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
L4	L4	PL40A	6	LDQ42	T (LVDS)*
L1	L1	PL41A	6	LDQ42	T
L5	L5	PL40B	6	LDQ42	C (LVDS)*
M1	M1	PL41B	6	LDQ42	C
GND	GND	GNDIO6	-		
N1	N1	PL43A	6	LDQ42	T
N2	N2	PL42A	6	LDQS42	T (LVDS)*
P1	P1	PL43B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
P2	P2	PL42B	6	LDQ42	C (LVDS)*
R1	R1	PL44A	6	LDQ42	T (LVDS)*
GND	GND	GNDIO6	-		
R2	R2	PL44B	6	LDQ42	C (LVDS)*
N4	N4	TDI	-		
M4	M4	TCK	-		
P3	P3	TDO	-		
N3	N3	TMS	-		
K7	K7	VCCJ	-		
M5	M5	PB2A	5	VREF2_5/BDQ6	T
K6	K6	PB3A	5	BDQ6	
M6	M6	PB2B	5	VREF1_5/BDQ6	C
R3	R3	PB5A	5	BDQ6	T
P4	P4	PB5B	5	BDQ6	C
-	VCC	VCCIO	5		
-	GND	GNDIO5	5		
N5	N5	PB30A	5	BDQ33	T
N6	N6	PB30B	5	BDQ33	C
T2	T2	PB31A	5	BDQ33	T
P6	P6	PB32A	5	BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
T3	T3	PB31B	5	BDQ33	C
R6	R6	PB32B	5	BDQ33	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

	LFE2-12E/12SE				LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C2	PT3A	0		T	PT3A	0		T
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
G10	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
H8	VCCIO0	0			VCCIO0	0		
G11	VCCIO1	1			VCCIO1	1		
G12	VCCIO1	1			VCCIO1	1		
G13	VCCIO1	1			VCCIO1	1		
G14	VCCIO1	1			VCCIO1	1		
H14	VCCIO2	2			VCCIO2	2		
H15	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K16	VCCIO2	2			VCCIO2	2		
L16	VCCIO3	3			VCCIO3	3		
M16	VCCIO3	3			VCCIO3	3		
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

	LFE2-12E/12SE				LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
C5	VCCAUX	-			VCCAUX	-		
D11	VCCAUX	-			VCCAUX	-		
E17	VCCAUX	-			VCCAUX	-		
E6	VCCAUX	-			VCCAUX	-		
F13	VCCAUX	-			VCCAUX	-		
G18	VCCAUX	-			VCCAUX	-		
G5	VCCAUX	-			VCCAUX	-		
K5	VCCAUX	-			VCCAUX	-		
M17	VCCAUX	-			VCCAUX	-		
P17	VCCAUX	-			VCCAUX	-		
R5	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V13	VCCAUX	-			VCCAUX	-		
V15	VCCAUX	-			VCCAUX	-		
V7	VCCAUX	-			VCCAUX	-		
V8	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

	LFE2-35E/SE				LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T
GNDIO	GNDIO4	-			GNDIO4	-		
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO	4		
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

	LFE2-35E/SE				LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K12	GND	-			GND	-		
K13	GND	-			GND	-		
K15	GND	-			GND	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-20E/20SE				LFE2-35E/35SE			
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
G24	PR6B	2	RDQ8	C (LVDS)*	PR12B	2	RDQ14	C (LVDS)*
G23	PR6A	2	RDQ8	T (LVDS)*	PR12A	2	RDQ14	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR5B	2	RDQ8	C	PR11B	2	RDQ14	C
J19	PR5A	2	RDQ8	T	PR11A	2	RDQ14	T
D26	PR4B	2	RDQ8	C (LVDS)*	PR10B	2	RDQ14	C (LVDS)*
C26	PR4A	2	RDQ8	T (LVDS)*	PR10A	2	RDQ14	T (LVDS)*
F22	NC	-			PR9B	2	RDQ6	C
E24	NC	-			PR9A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
D25	NC	-			PR8B	2	RDQ6	C (LVDS)*
C25	NC	-			PR8A	2	RDQ6	T (LVDS)*
D24	NC	-			PR7B	2	RDQ6	C
B25	NC	-			PR7A	2	RDQ6	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	NC	-			PR6B	2	RDQ6	C (LVDS)*
G22	NC	-			PR6A	2	RDQS6	T (LVDS)*
B24	NC	-			PR5B	2	RDQ6	C
GND	GNDIO2	-			GNDIO2	-		
C24	NC	-			PR5A	2	RDQ6	T
D23	NC	-			PR4B	2	RDQ6	C (LVDS)*
C23	NC	-			PR4A	2	RDQ6	T (LVDS)*
G21	PR3B	2		C	PR3B	2	RDQ6	C
VCCIO	VCCIO2	2			VCCIO2	2		
H20	PR3A	2		T	PR3A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2/RDQ6	C (LVDS)*
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2/RDQ6	T (LVDS)*
E23	PT64B	1	VREF2_1	C	PT73B	1	VREF2_1	C
GND	GNDIO1	-			GNDIO1	-		
D22	PT64A	1	VREF1_1	T	PT73A	1	VREF1_1	T
G20	PT63B	1		C	PT72B	1		C
J18	PT63A	1		T	PT72A	1		T
F20	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H19	PT62A	1		T	PT71A	1		T
A24	PT61B	1		C	PT70B	1		C
A23	PT61A	1		T	PT70A	1		T
E21	PT60B	1		C	PT69B	1		C
F19	PT60A	1		T	PT69A	1		T
C22	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
E20	PT59A	1		T	PT68A	1		T
B22	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B23	PT58A	1		T	PT67A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-50E/SE				LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-50E/SE				LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT35B	0		C	PT44B	0		C
B7	PT35A	0		T	PT44A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT34B	0		C	PT43B	0		C
D10	PT34A	0		T	PT43A	0		T
H11	PT33B	0		C	PT42B	0		C
G11	PT33A	0		T	PT42A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT32B	0		C	PT41B	0		C
B6	PT32A	0		T	PT41A	0		T
D8	PT31B	0		C	PT40B	0		C
C8	PT31A	0		T	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT30B	0		C	PT39B	0		C
E10	PT30A	0		T	PT39A	0		T
E9	PT29B	0		C	PT38B	0		C
D9	PT29A	0		T	PT38A	0		T
G10	PT28B	0		C	PT37B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT28A	0		T	PT37A	0		T
A5	PT27B	0		C	PT36B	0		C
B5	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT26A	0		T	PT35A	0		T
E8	PT25B	0		C	PT34B	0		C
F10	PT25A	0		T	PT34A	0		T
F8	PT24B	0		C	PT33B	0		C
H9	PT24A	0		T	PT33A	0		T
C5	PT23B	0		C	PT32B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT23A	0		T	PT32A	0		T
B4	PT22B	0			PT31B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-50E/SE				LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA

	LFE2M50E/SE				LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D2	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7	T
D3	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
J8	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
H7	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
E3	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
E4	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
GNDIO	GNDIO7	-			-	-		
G6	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F5	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
E2	PL14A	7		T	PL14A	7	LDQ15	T
D1	PL14B	7		C	PL14B	7	LDQ15	C
-	-	-			GNDIO7	-		
G5	NC	-			PL15A	7	LDQS15	T (LVDS)*
G4	NC	-			PL15B	7	LDQ15	C (LVDS)*
K7	NC	-			PL16A	7	LDQ15	T
K8	NC	-			PL16B	7	LDQ15	C
E1	NC	-			PL17A	7	LDQ15	T (LVDS)*
F2	NC	-			PL17B	7	LDQ15	C (LVDS)*
F1	NC	-			PL18A	7	LDQ15	T
-	-	-			GNDIO7	-		
G3	NC	-			PL18B	7	LDQ15	C
H5	PL15A	7		T (LVDS)*	PL21A	7		T (LVDS)*
H4	PL15B	7		C (LVDS)*	PL21B	7		C (LVDS)*
J5	PL16A	7		T	PL22A	7		T
J4	PL16B	7		C	PL22B	7		C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	NC	-			PL24A	7	LDQ28	T (LVDS)*
G1	NC	-			PL24B	7	LDQ28	C (LVDS)*
L9	NC	-			PL25A	7	LDQ28	T
L7	NC	-			PL25B	7	LDQ28	C
K6	NC	-			PL26A	7	LDQ28	T (LVDS)*
K5	NC	-			PL26B	7	LDQ28	C (LVDS)*
L8	NC	-			PL27A	7	LDQ28	T
L6	NC	-			PL27B	7	LDQ28	C
-	-	-			GNDIO7	-		
H3	PL18A	7		T (LVDS)*	PL28A	7	LDQS28	T (LVDS)*
H2	PL18B	7		C (LVDS)*	PL28B	7	LDQ28	C (LVDS)*
N8	PL19A	7		T	PL29A	7	LDQ28	T
M9	PL19B	7		C	PL29B	7	LDQ28	C
J3	PL20A	7		T (LVDS)*	PL30A	7	LDQ28	T (LVDS)*
VCCIO	VCCIO7	7			-	-		
J2	PL20B	7		C (LVDS)*	PL30B	7	LDQ28	C (LVDS)*
H1	PL21A	7		T	PL31A	7	LDQ28	T
GNDIO	GNDIO7	-			GNDIO7	-		
J1	PL21B	7		C	PL31B	7	LDQ28	C
-	-	-			-	-		
-	-	-			-	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

	LFE2M70E/SE				LFE2M100E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA8	PL65A	6	LDQ64	T	PL73A	6	LDQ72	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y9	PL65B	6	LDQ64	C	PL73B	6	LDQ72	C
AA6	PL66A	6	LDQ64	T (LVDS)*	PL74A	6	LDQ72	T (LVDS)*
AA7	PL66B	6	LDQ64	C (LVDS)*	PL74B	6	LDQ72	C (LVDS)*
AA4	PL67A	6	LDQ64	T	PL75A	6	LDQ72	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA3	PL67B	6	LDQ64	C	PL75B	6	LDQ72	C
AA9	PL69A	6	LDQ73	T (LVDS)*	PL77A	6	LDQ81	T (LVDS)*
AA10	PL69B	6	LDQ73	C (LVDS)*	PL77B	6	LDQ81	C (LVDS)*
AA5	PL70A	6	LDQ73	T	PL78A	6	LDQ81	T
AB6	PL70B	6	LDQ73	C	PL78B	6	LDQ81	C
AB1	PL71A	6	LDQ73	T (LVDS)*	PL79A	6	LDQ81	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AB2	PL71B	6	LDQ73	C (LVDS)*	PL79B	6	LDQ81	C (LVDS)*
AC8	PL72A	6	LDQ73	T	PL80A	6	LDQ81	T
AB10	PL72B	6	LDQ73	C	PL80B	6	LDQ81	C
AC1	PL73A	6	LDQS73	T (LVDS)*	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AC2	PL73B	6	LDQ73	C (LVDS)*	PL81B	6	LDQ81	C (LVDS)*
AB7	PL74A	6	LDQ73	T	PL82A	6	LDQ81	T
AB5	PL74B	6	LDQ73	C	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6			VCCIO6	6		
AC3	PL75A	6	LDQ73	T (LVDS)*	PL83A	6	LDQ81	T (LVDS)*
AC4	PL75B	6	LDQ73	C (LVDS)*	PL83B	6	LDQ81	C (LVDS)*
AC10	PL76A	6	LDQ73	T	PL84A	6	LDQ81	T
AC9	PL76B	6	LDQ73	C	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-			GNDIO6	-		
AC7	NC	-			PL86A	6	LDQ90	T (LVDS)*
AC5	NC	-			PL86B	6	LDQ90	C (LVDS)*
AC6	NC	-			PL87A	6	LDQ90	T
AD5	NC	-			PL87B	6	LDQ90	C
-	-	-			VCCIO6	6		
AD4	NC	-			PL88A	6	LDQ90	T (LVDS)*
AD3	NC	-			PL88B	6	LDQ90	C (LVDS)*
AD10	NC	-			PL89A	6	LDQ90	T
AD8	NC	-			PL89B	6	LDQ90	C
-	-	-			GNDIO6	-		
AD2	NC	-			PL90A	6	LDQS90	T (LVDS)*
AD1	NC	-			PL90B	6	LDQ90	C (LVDS)*
AD9	NC	-			PL91A	6	LDQ90	T
-	-	-			VCCIO6	6		
AC11	NC	-			PL91B	6	LDQ90	C
AD6	NC	-			PL92A	6	LDQ90	T (LVDS)*
AD7	NC	-			PL92B	6	LDQ90	C (LVDS)*
AE1	NC	-			PL93A	6	LDQ90	T
-	-	-			GNDIO6	-		
AE2	NC	-			PL93B	6	LDQ90	C
AF2	PL78A	6	LDQ82	T (LVDS)*	PL95A	6	LDQ99	T (LVDS)*