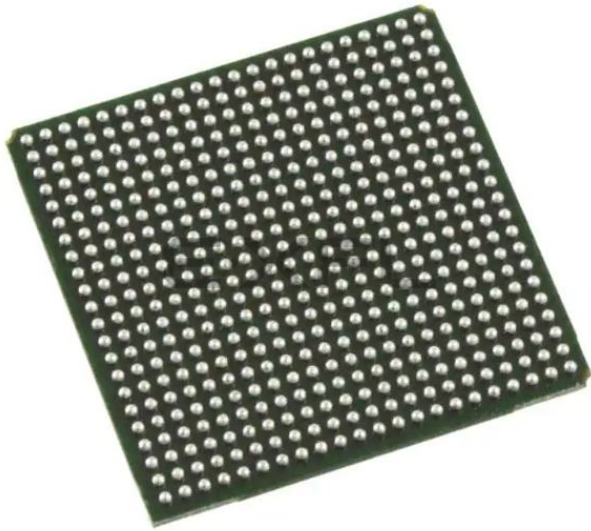




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	297
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5fn484i

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeECP2/M devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, allowing the routing of both short and long connections between PFUs.

The LatticeECP2/M family has an enhanced routing architecture that produces a compact design. The Diamond design software takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (GPLL/SPLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP2/M family support two General Purpose PLLs (GPLLs) which are full-featured PLLs. In addition, some of the larger devices have two to six Standard PLLs (SPLLs) that have a subset of GPLL functionality.

General Purpose PLL (GPLL)

The architecture of the GPLL is shown in Figure 2-5. A description of the GPLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP or from a user clock PIN/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

The Delay Adjust Block adjusts either the delays of the reference or feedback signals. The Delay Adjust Block can either be programmed during configuration or can be adjusted dynamically. The setup, hold or clock-to-out times of the device can be improved by programming a delay in the feedback or input path of the PLL, which will advance or delay the output clock with reference to the input clock.

Following the Delay Adjust Block, both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied. LatticeECP2/M devices have two dedicated pins on the left and right edges of the device for connecting optional external capacitors to the VCO. This allows the PLLs to operate at a lower frequency. This is a shared resource that can only be used by one PLL (GPLL or SPLL) per side.

The output of the VCO then enters the post-scalar divider. The post-scalar divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. A secondary divider takes the CLKOP signal and uses it to derive lower frequency outputs (CLKOK). The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOP signal and generates the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The primary output from the post scalar divider CLKOP along with the outputs from the secondary divider (CLKOK) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

Figure 2-25. MULTADDSUB

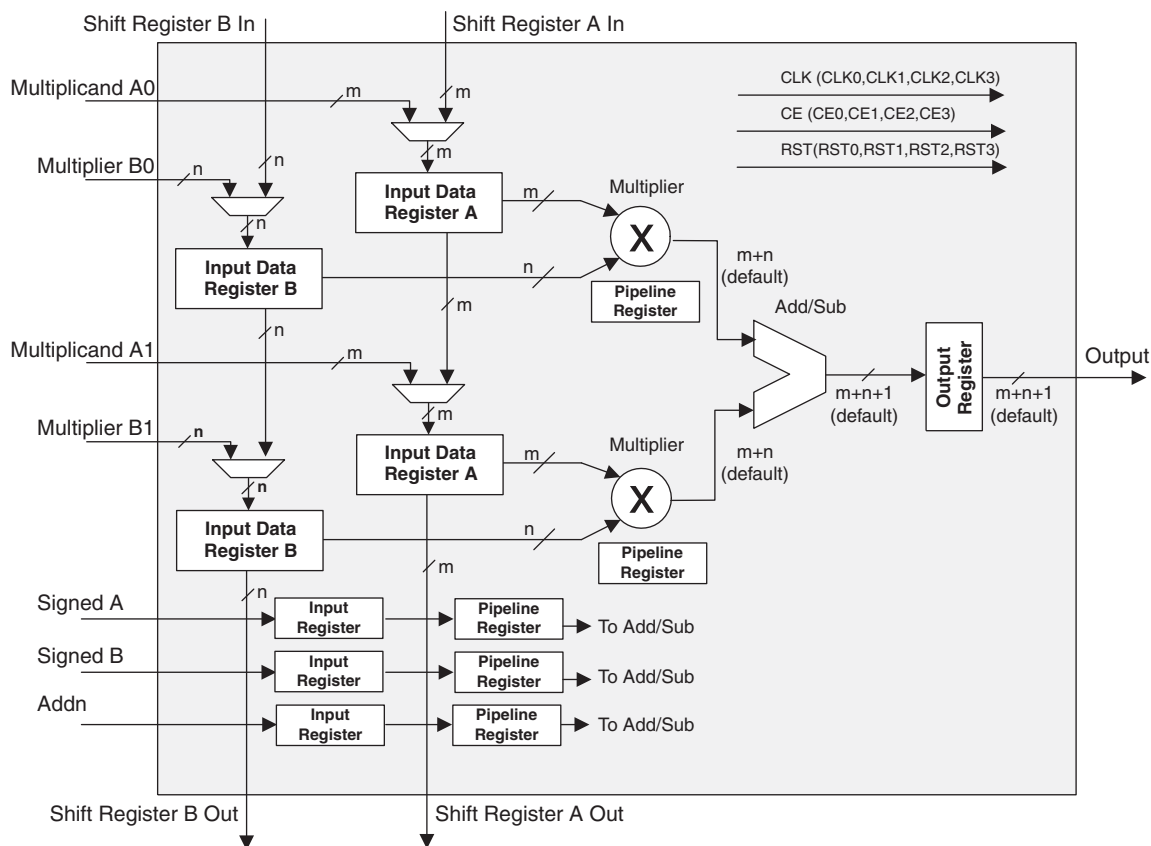
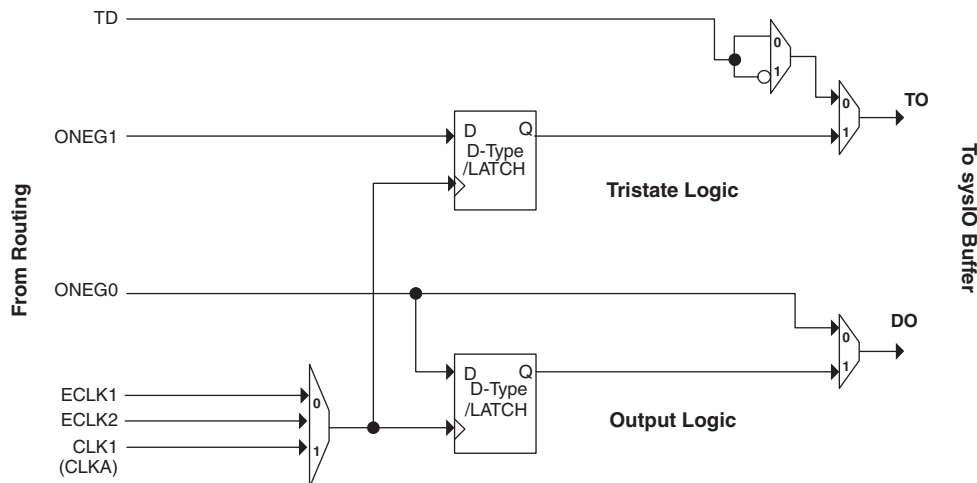


Figure 2-32. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (DO).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

Bottom Edge

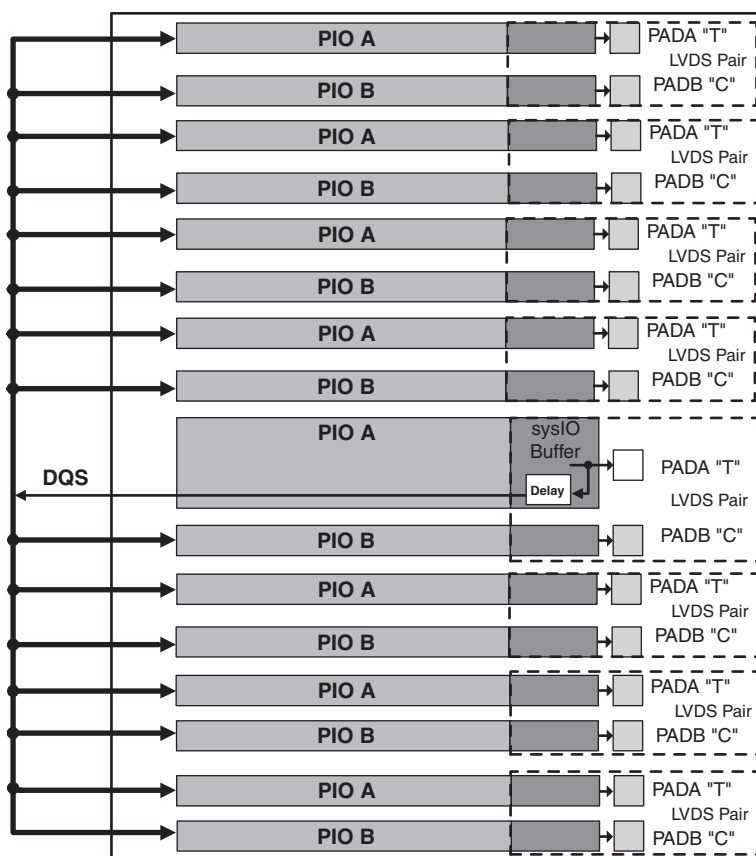
PICs on the bottom edge have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device



Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	3.8	ns
32-bit Decoder	4.5	ns
64-bit Decoder	5.0	ns
4:1 MUX	3.2	ns
8:1 MUX	3.4	ns
16:1 MUX	3.5	ns
32:1 MUX	4.0	ns

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	599	MHz
32-bit Decoder	542	MHz
64-bit Decoder	417	MHz
4:1 MUX	847	MHz
8:1 MUX	803	MHz
16:1 MUX	660	MHz
32:1 MUX	577	MHz
8-bit Adder	591	MHz
16-bit Adder	500	MHz
64-bit Adder	306	MHz
16-bit Counter	488	MHz
32-bit Counter	378	MHz
64-bit Counter	260	MHz
64-bit Accumulator	253	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	280	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	819	MHz
32x4 Pseudo-Dual Port RAM	521	MHz
64x8 Pseudo-Dual Port RAM	435	MHz
DSP Functions		
18x18 Multiplier (All Registers)	420	MHz
9x9 Multiplier (All Registers)	420	MHz

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M8	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
P7	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
R8	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
VCCIO	VCCIO4	4			VCCIO4	4		
T5	PB14A	4	BDQ15	T	PB32A	4	BDQ33	T
T6	PB14B	4	BDQ15	C	PB32B	4	BDQ33	C
T8	PB15A	4	BDQS15	T	PB33A	4	BDQS33	T
GND	GNDIO4	-			GNDIO4	-		
R7	PB16A	4	BDQ15	T	PB34A	4	BDQ33	T
T9	PB15B	4	BDQ15	C	PB33B	4	BDQ33	C
T7	PB16B	4	BDQ15	C	PB34B	4	BDQ33	C
L8	PB17A	4	BDQ15	T	PB35A	4	BDQ33	T
VCCIO	VCCIO4	4			VCCIO4	4		
P8	PB18A	4	BDQ15	T	PB36A	4	BDQ33	T
L9	PB17B	4	BDQ15	C	PB35B	4	BDQ33	C
N8	PB18B	4	BDQ15	C	PB36B	4	BDQ33	C
R9	PB19A	4	BDQ15	T	PB37A	4	BDQ33	T
GND	GNDIO4	-			GNDIO4	-		
R10	PB19B	4	BDQ15	C	PB37B	4	BDQ33	C
-	-	-			VCCIO	4		
-	-	-			GNDIO4	4		
N9	PB20A	4	BDQ24	T	PB47A	4	BDQ51	T
T10	PB21A	4	BDQ24	T	PB48A	4	BDQ51	T
M9	PB20B	4	BDQ24	C	PB47B	4	BDQ51	C
R11	PB21B	4	BDQ24	C	PB48B	4	BDQ51	C
P10	PB22A	4	BDQ24	T	PB49A	4	BDQ51	T
N11	PB23A	4	BDQ24	T	PB50A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
N10	PB22B	4	BDQ24	C	PB49B	4	BDQ51	C
P11	PB23B	4	BDQ24	C	PB50B	4	BDQ51	C
T11	PB24A	4	BDQS24	T	PB51A	4	BDQS51	T
GND	GNDIO4	-			GNDIO4	-		
M11	PB25A	4	BDQ24	T	PB52A	4	BDQ51	T
T12	PB24B	4	BDQ24	C	PB51B	4	BDQ51	C
L11	PB25B	4	BDQ24	C	PB52B	4	BDQ51	C
T13	PB26A	4	BDQ24	T	PB53A	4	BDQ51	T
R13	PB27A	4	BDQ24	T	PB54A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
T14	PB26B	4	BDQ24	C	PB53B	4	BDQ51	C
P13	PB27B	4	BDQ24	C	PB54B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
N12	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
M12	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
R15	CFG2	8			CFG2	8		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
GND	GND	GNDIO5	-		
R4	R4	PB33A	5	BDQS33	T
L6	L6	PB34A	5	BDQ33	T
T4	T4	PB33B	5	BDQ33	C
L7	L7	PB34B	5	BDQ33	C
N7	N7	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
M8	M8	PB35B	5	PCLKC5_0/BDQ33	C
GND	GND	GNDIO5	-		
P7	P7	PB40A	4	PCLKT4_0/BDQ42	T
R8	R8	PB40B	4	PCLKC4_0/BDQ42	C
VCCIO	VCCIO	VCCIO4	4		
T5	T5	PB41A	4	BDQ42	T
T6	T6	PB41B	4	BDQ42	C
T8	T8	PB42A	4	BDQS42	T
GND	GND	GNDIO4	-		
R7	R7	PB43A	4	BDQ42	T
T9	T9	PB42B	4	BDQ42	C
T7	T7	PB43B	4	BDQ42	C
L8	L8	PB44A	4	BDQ42	T
VCCIO	VCCIO	VCCIO4	4		
P8	P8	PB45A	4	BDQ42	T
L9	L9	PB44B	4	BDQ42	C
N8	N8	PB45B	4	BDQ42	C
R9	R9	PB46A	4	BDQ42	T
GND	GND	GNDIO4	-		
R10	R10	PB46B	4	BDQ42	C
-	VCC	VCCIO	4		
-	GND	GNDIO4	4		
N9	N9	PB56A	4	BDQ60	T
T10	T10	PB57A	4	BDQ60	T
M9	M9	PB56B	4	BDQ60	C
R11	R11	PB57B	4	BDQ60	C
P10	P10	PB58A	4	BDQ60	T
N11	N11	PB59A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
N10	N10	PB58B	4	BDQ60	C
P11	P11	PB59B	4	BDQ60	C
T11	T11	PB60A	4	BDQS60	T
GND	GND	GNDIO4	-		
M11	M11	PB61A	4	BDQ60	T
T12	T12	PB60B	4	BDQ60	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C2	PT3A	0		T	PT3A	0		T	
J10	VCC	-			VCC	-			
J11	VCC	-			VCC	-			
J12	VCC	-			VCC	-			
J13	VCC	-			VCC	-			
K14	VCC	-			VCC	-			
K9	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L9	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M9	VCC	-			VCC	-			
N14	VCC	-			VCC	-			
N9	VCC	-			VCC	-			
P10	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P13	VCC	-			VCC	-			
G10	VCCIO0	0			VCCIO0	0			
G9	VCCIO0	0			VCCIO0	0			
H9	VCCIO0	0			VCCIO0	0			
H8	VCCIO0	0			VCCIO0	0			
G11	VCCIO1	1			VCCIO1	1			
G12	VCCIO1	1			VCCIO1	1			
G13	VCCIO1	1			VCCIO1	1			
G14	VCCIO1	1			VCCIO1	1			
H14	VCCIO2	2			VCCIO2	2			
H15	VCCIO2	2			VCCIO2	2			
J15	VCCIO2	2			VCCIO2	2			
K16	VCCIO2	2			VCCIO2	2			
L16	VCCIO3	3			VCCIO3	3			
M16	VCCIO3	3			VCCIO3	3			
N16	VCCIO3	3			VCCIO3	3			
P16	VCCIO3	3			VCCIO3	3			
R14	VCCIO4	4			VCCIO4	4			
T12	VCCIO4	4			VCCIO4	4			
T13	VCCIO4	4			VCCIO4	4			
T14	VCCIO4	4			VCCIO4	4			
R9	VCCIO5	5			VCCIO5	5			
T10	VCCIO5	5			VCCIO5	5			
T11	VCCIO5	5			VCCIO5	5			
T9	VCCIO5	5			VCCIO5	5			
N7	VCCIO6	6			VCCIO6	6			
P7	VCCIO6	6			VCCIO6	6			
P8	VCCIO6	6			VCCIO6	6			

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*	
U25	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLL_T_IN_A**/RDQ80	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCCPLL	3			VCCPLL	-			
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C	
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*	
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*	
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C	
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*	
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*	
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C	
GND	GNDIO3	-			GNDIO3	-			
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T	
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*	
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*	
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T	
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*	
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*	
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C	
GND	GNDIO3	-			GNDIO3	-			
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T	
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*	
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*	
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T	
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*	
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C	
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T	
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*	
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C	
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T	
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*	
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*	
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C	
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7		
F4	PL2A	7	VREF2_7	T (LVDS)*
F3	PL2B	7	VREF1_7	C (LVDS)*
H4	PL3A	7		T
G5	PL3B	7		C
GND	GNDIO7	-		
D2	PL4A	7		T (LVDS)*
D1	PL4B	7		C (LVDS)*
E2	PL5A	7		T
VCCIO	VCCIO7	7		
E1	PL5B	7		C
GND	GNDIO7	-		
VCCIO	VCCIO7	7		
F1	PL14A	7	LUM1_SPLLT_IN_A/LDQ12	T (LVDS)*
F2	PL14B	7	LUM1_SPLLC_IN_A/LDQ12	C (LVDS)*
G1	PL15A	7	LUM1_SPLLT_FB_A/LDQ12	T
G2	PL15B	7	LUM1_SPLLC_FB_A/LDQ12	C
GND	GNDIO7	-		
H8	PL18A	7	LDQ21	T
H6	PL18B	7	LDQ21	C
VCCIO	VCCIO7	7		
G4	PL19A	7	LDQ21	T (LVDS)*
G3	PL19B	7	LDQ21	C (LVDS)*
H7	PL20A	7	LDQ21	T
H5	PL20B	7	LDQ21	C
GND	GNDIO7	-		
H2	PL21A	7	LDQS21	T (LVDS)*
H1	PL21B	7	LDQ21	C (LVDS)*
J6	PL22A	7	LDQ21	T
VCCIO	VCCIO7	7		
J8	PL22B	7	LDQ21	C
J2	PL23A	7	LDQ21	T (LVDS)*
J1	PL23B	7	LDQ21	C (LVDS)*
J5	PL24A	7	LDQ21	T
GND	GNDIO7	-		
J7	PL24B	7	LDQ21	C
J4	PL25A	7	LDQ29	T (LVDS)*
J3	PL25B	7	LDQ29	C (LVDS)*
K6	PL26A	7	LDQ29	T
K8	PL26B	7	LDQ29	C
VCCIO	VCCIO7	7		
K2	PL27A	7	LDQ29	T (LVDS)*

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L5	PL23A	7	LDQ27	T (LVDS)*	PL33A	7	LDQ37	T (LVDS)*	
L4	PL23B	7	LDQ27	C (LVDS)*	PL33B	7	LDQ37	C (LVDS)*	
N9	PL24A	7	LDQ27	T	PL34A	7	LDQ37	T	
N7	PL24B	7	LDQ27	C	PL34B	7	LDQ37	C	
K2	PL25A	7	LDQ27	T (LVDS)*	PL35A	7	LDQ37	T (LVDS)*	
K1	PL25B	7	LDQ27	C (LVDS)*	PL35B	7	LDQ37	C (LVDS)*	
P9	PL26A	7	LDQ27	T	PL36A	7	LDQ37	T	
P7	PL26B	7	LDQ27	C	PL36B	7	LDQ37	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M6	PL27A	7	LDQS27	T (LVDS)*	PL37A	7	LDQS37	T (LVDS)*	
M5	PL27B	7	LDQ27	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
N5	PL28A	7	LDQ27	T	PL38A	7	LDQ37	T	
N6	PL28B	7	LDQ27	C	PL38B	7	LDQ37	C	
M4	PL29A	7	LDQ27	T (LVDS)*	PL39A	7	LDQ37	T (LVDS)*	
M3	PL29B	7	LDQ27	C (LVDS)*	PL39B	7	LDQ37	C (LVDS)*	
P6	PL30A	7	LDQ27	T	PL40A	7	LDQ37	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P8	PL30B	7	LDQ27	C	PL40B	7	LDQ37	C	
L3	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	
L2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	
P5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	
P4	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	
L1	PL34A	7	LDQ36	T (LVDS)*	PL44A	7	LDQ46	T (LVDS)*	
M2	PL34B	7	LDQ36	C (LVDS)*	PL44B	7	LDQ46	C (LVDS)*	
R5	PL35A	7	LDQ36	T	PL45A	7	LDQ46	T	
R4	PL35B	7	LDQ36	C	PL45B	7	LDQ46	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M1	PL36A	7	LDQS36	T (LVDS)*	PL46A	7	LDQS46	T (LVDS)*	
N2	PL36B	7	LDQ36	C (LVDS)*	PL46B	7	LDQ46	C (LVDS)*	
R8	PL37A	7	LDQ36	T	PL47A	7	LDQ46	T	
T9	PL37B	7	LDQ36	C	PL47B	7	LDQ46	C	
P3	PL38A	7	LDQ36	T (LVDS)*	PL48A	7	LDQ46	T (LVDS)*	
P2	PL38B	7	LDQ36	C (LVDS)*	PL48B	7	LDQ46	C (LVDS)*	
N1	PL39A	7	PCLKT7_0/LDQ36	T	PL49A	7	PCLKT7_0/LDQ46	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P1	PL39B	7	PCLKC7_0/LDQ36	C	PL49B	7	PCLKC7_0/LDQ46	C	
T5	PL41A	6	PCLKT6_0	T (LVDS)*	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	
T4	PL41B	6	PCLKC6_0	C (LVDS)*	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	
U7	PL42A	6	VREF2_6	T	PL52A	6	VREF2_6/LDQ55	T	
T8	PL42B	6	VREF1_6	C	PL52B	6	VREF1_6/LDQ55	C	
R3	PL43A	6		T (LVDS)*	PL53A	6	LDQ55	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
R2	PL43B	6		C (LVDS)*	PL53B	6	LDQ55	C (LVDS)*	
R1	PL44A	6		T	PL54A	6	LDQ55	T	
T1	PL44B	6		C	PL54B	6	LDQ55	C	
GNDIO	GNDIO6	-			GNDIO6	-			
-	-	-			VCCIO6	6			
T3	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			VCCIO2	2			
H23	NC	-			PR15B	2	RDQ15	C (LVDS)*	
H24	NC	-			PR15A	2	RDQS15	T (LVDS)*	
D28	NC	-			PR14B	2	RDQ15	C	
-	-	-			GNDIO2	-			
E28	NC	-			PR14A	2	RDQ15	T	
G24	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
H25	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
D27	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
GNDIO	GNDIO2	-			VCCIO2	2			
E27	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	
G25	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
F24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
VCCIO	VCCIO2	-			-	-			
GNDIO	GNDIO2	-			GNDIO2	-			
F25	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G23	XRES	-			XRES	1			
C30	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A29	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B30	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B29	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C27	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A26	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A27	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B26	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C26	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B25	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C25	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A25	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C29	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B28	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C28	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A28	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B24	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E24	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D24	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C24	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A20	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	
C20	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B20	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C19	URC_SQ_VCCR_X2	12			URC_SQ_VCCR_X2	12			
A23	URC_SQ_HDOUT_P2	12		T	URC_SQ_HDOUT_P2	12		T	
C23	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B23	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C22	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B22	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
J16	PT51B	1		C	PT60B	1		C	
G15	PT51A	1		T	PT60A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT50B	1		C	PT59B	1		C	
D16	PT50A	1		T	PT59A	1		T	
J15	PT49B	1		C	PT58B	1		C	
H15	PT49A	1		T	PT58A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A15	PT48B	1	VREF2_1	C	PT57B	1	VREF2_1	C	
B15	PT48A	1	VREF1_1	T	PT57A	1	VREF1_1	T	
F15	PT47B	1	PCLKC1_0	C	PT56B	1	PCLKC1_0	C	
E16	PT47A	1	PCLKT1_0	T	PT56A	1	PCLKT1_0	T	
C15	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
D15	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T	
C14	PT45B	0	VREF2_0	C	PT54B	0	VREF2_0	C	
E15	PT45A	0	VREF1_0	T	PT54A	0	VREF1_0	T	
G14	PT44B	0		C	PT53B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J14	PT44A	0		T	PT53A	0		T	
F14	PT43B	0		C	PT52B	0		C	
H14	PT43A	0		T	PT52A	0		T	
A14	PT42B	0		C	PT51B	0		C	
B14	PT42A	0		T	PT51A	0		T	
D13	PT41B	0		C	PT50B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F13	PT41A	0		T	PT50A	0		T	
G13	PT40B	0		C	PT49B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J11	PT40A	0		T	PT49A	0		T	
D4	PT38B	0		C	PT47B	0		C	
D5	PT38A	0		T	PT47A	0		T	
E5	PT37B	0		C	PT46B	0		C	
F6	PT37A	0		T	PT46A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT34B	0		C	PT43B	0		C	
D8	PT34A	0		T	PT43A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
J13	PT32B	0		C	PT41B	0		C	
G11	PT32A	0		T	PT41A	0		T	
H13	PT31B	0		C	PT40B	0		C	
H12	PT31A	0		T	PT40A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
E8	PT30B	0		C	PT39B	0		C	
D9	PT30A	0		T	PT39A	0		T	
D12	PT28B	0		C	PT37B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J2	PL34B	7	LDQ32	C (LVDS)*
H1	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-		
J1	PL35B	7	LDQ32	C
GNDIO	GNDIO7	-		
L5	PL41A	7	LDQ45	T (LVDS)*
L4	PL41B	7	LDQ45	C (LVDS)*
N9	PL42A	7	LDQ45	T
N7	PL42B	7	LDQ45	C
K2	PL43A	7	LDQ45	T (LVDS)*
K1	PL43B	7	LDQ45	C (LVDS)*
P9	PL44A	7	LDQ45	T
P7	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-		
M6	PL45A	7	LDQS45	T (LVDS)*
M5	PL45B	7	LDQ45	C (LVDS)*
N5	PL46A	7	LDQ45	T
N6	PL46B	7	LDQ45	C
M4	PL47A	7	LDQ45	T (LVDS)*
M3	PL47B	7	LDQ45	C (LVDS)*
P6	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-		
P8	PL48B	7	LDQ45	C
L3	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
L2	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
P5	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T
P4	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
L1	PL52A	7	LDQ54	T (LVDS)*
M2	PL52B	7	LDQ54	C (LVDS)*
R5	PL53A	7	LDQ54	T
R4	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-		
M1	PL54A	7	LDQS54	T (LVDS)*
N2	PL54B	7	LDQ54	C (LVDS)*
R8	PL55A	7	LDQ54	T
T9	PL55B	7	LDQ54	C
P3	PL56A	7	LDQ54	T (LVDS)*
P2	PL56B	7	LDQ54	C (LVDS)*
N1	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-		
P1	PL57B	7	PCLKC7_0/LDQ54	C
T5	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
T4	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AJ30	LRC_SQ_VCCIB0	13		
AK29	LRC_SQ_HDINP0	13		T
AH30	LRC_SQ_VCCRX0	13		
AG27	CFG2	8		
AD25	CFG1	8		
AG28	CFG0	8		
AG30	PROGRAMN	8		
AG29	CCLK	8		
AC24	INITN	8		
AF27	DONE	8		
GNDIO	GNDIO8	-		
AF28	WRITEN***	8		
AE26	CS1N***	8		
AB23	CSN***	8		
AF29	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8		
AF30	D1***	8		
AD26	D2***	8		
AE29	D3***	8		
GNDIO	GNDIO8	-		
AE30	D4***	8		
AD29	D5***	8		
AC25	D6***	8		
AD30	D7/SPID0***	8		
VCCIO	VCCIO8	8		
AA22	DI/CSSPI0N***	8		
AC26	DOUT/CSON/CSSPI1N***	8		
AA23	BUSY/SISPI***	8		
AB22	RLM0_PLLCAP	3		
AC27	PR102B	3	RLM0_GDLLC_FB_A/RDQ99	C
GNDIO	GNDIO3	-		
AC28	PR102A	3	RLM0_GDLLT_FB_A/RDQ99	T
AC29	PR101B	3	RLM0_GDLLC_IN_A**/RDQ99	C (LVDS)*
AC30	PR101A	3	RLM0_GDLLT_IN_A**/RDQ99	T (LVDS)*
AB30	PR100B	3	RLM0_GPLLC_IN_A**/RDQ99	C
VCCIO	VCCIO3	3		
AA30	PR100A	3	RLM0_GPLLT_IN_A**/RDQ99	T
AB29	PR99B	3	RLM0_GPLLC_FB_A/RDQ99	C (LVDS)*
AB28	PR99A	3	RLM0_GPLLT_FB_A/RDQS99	T (LVDS)*
GNDIO	GNDIO3	-		
Y22	PR98B	3	RDQ99	C
Y23	PR98A	3	RDQ99	T
AB26	PR97B	3	RDQ99	C (LVDS)*

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO2	-		
M27	PR47B	2	RDQ45	C (LVDS)*
M28	PR47A	2	RDQ45	T (LVDS)*
H30	PR46B	2	RDQ45	C
G30	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2		
M25	PR45B	2	RDQ45	C (LVDS)*
M26	PR45A	2	RDQS45	T (LVDS)*
L30	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-		
L29	PR44A	2	RDQ45	T
L28	PR43B	2	RDQ45	C (LVDS)*
L27	PR43A	2	RDQ45	T (LVDS)*
H29	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2		
G29	PR42A	2	RDQ45	T
L22	PR41B	2	RDQ45	C (LVDS)*
M22	PR41A	2	RDQ45	T (LVDS)*
F30	PR40B	2		C
GNDIO	GNDIO2	-		
F29	PR40A	2		T
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E30	PR34B	2	RDQ32	C (LVDS)*
E29	PR34A	2	RDQ32	T (LVDS)*
-	-	-		
L25	PR33B	2	RDQ32	C
L26	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2		
H28	PR32B	2	RDQ32	C (LVDS)*
J28	PR32A	2	RDQS32	T (LVDS)*
G28	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-		
G27	PR31A	2	RDQ32	T
L24	PR30B	2	RDQ32	C (LVDS)*
L23	PR30A	2	RDQ32	T (LVDS)*
D30	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2		
D29	PR29A	2	RDQ32	T
K24	PR28B	2	RDQ32	C (LVDS)*
K25	PR28A	2	RDQ32	T (LVDS)*
J27	PR26B	2	RDQ23	C
GNDIO	GNDIO2	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO0	-			GNDIO0	-		
G15	PT41A	0		T	PT46A	0		T
J14	NC	-			PT45B	0		C
L15	NC	-			PT45A	0		T
H14	NC	-			PT44B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
K14	NC	-			PT44A	0		T
F15	PT38B	0		C	PT42B	0		C
G14	PT38A	0		T	PT42A	0		T
C15	PT37B	0		C	PT41B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		
D14	PT37A	0		T	PT41A	0		T
G13	PT36B	0		C	PT40B	0		C
-	-	-			VCCIO0	0		
J13	PT36A	0		T	PT40A	0		T
B14	PT35B	0		C	PT39B	0		C
VCCIO	VCCIO0	0			-	-		
A14	PT35A	0		T	PT39A	0		T
F13	PT34B	0		C	PT38B	0		C
H13	PT34A	0		T	PT38A	0		T
D13	PT33B	0		C	PT37B	0		C
C14	PT33A	0		T	PT37A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
E13	PT32B	0		C	PT32B	0		C
D12	PT32A	0		T	PT32A	0		T
G12	PT31B	0		C	PT31B	0		C
E12	PT31A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	NC	-			PT30B	0		C
D11	NC	-			PT30A	0		T
F11	NC	-			PT29B	0		C
E11	NC	-			PT29A	0		T
D7	ULC_SQ_VCCRX0	11			ULC_SQ_VCCRX0	11		
C9	ULC_SQ_HDINP0	11		T	ULC_SQ_HDINP0	11		T
B9	ULC_SQ_VCCIB0	11			ULC_SQ_VCCIB0	11		
C8	ULC_SQ_HDINN0	11		C	ULC_SQ_HDINN0	11		C
B8	ULC_SQ_VCCTX0	11			ULC_SQ_VCCTX0	11		
A9	ULC_SQ_HDOUTP0	11		T	ULC_SQ_HDOUTP0	11		T
D9	ULC_SQ_VCCOB0	11			ULC_SQ_VCCOB0	11		
A8	ULC_SQ_HDOUTN0	11		C	ULC_SQ_HDOUTN0	11		C
B7	ULC_SQ_VCCTX1	11			ULC_SQ_VCCTX1	11		
A7	ULC_SQ_HDOUTN1	11		C	ULC_SQ_HDOUTN1	11		C
E7	ULC_SQ_VCCOB1	11			ULC_SQ_VCCOB1	11		
A6	ULC_SQ_HDOUTP1	11		T	ULC_SQ_HDOUTP1	11		T
B6	ULC_SQ_VCCRX1	11			ULC_SQ_VCCRX1	11		
C7	ULC_SQ_HDINN1	11		C	ULC_SQ_HDINN1	11		C
D8	ULC_SQ_VCCIB1	11			ULC_SQ_VCCIB1	11		
C6	ULC_SQ_HDINP1	11		T	ULC_SQ_HDINP1	11		T
E6	ULC_SQ_VCCAUX33	11			ULC_SQ_VCCAUX33	11		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table.
		Ordering Information	Updated ordering part number table to include ECP2-12.
			Updated topside mark drawing.
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions.
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
			Updated timing numbers to include LFE2-12E (rev A 0.08).
		Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.
		Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added "Security Series" to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	"Security Series" ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.
August 2007	02.8	Introduction	1156-fpBGA package option has been removed from the LatticeECP2M family.
		Architecture	Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated.
		DC and Switching	Supply Current (Standby) table has been updated.
			DSP Function timing has been updated.