Lattice Semiconductor Corporation - LFE2-12E-5QN208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

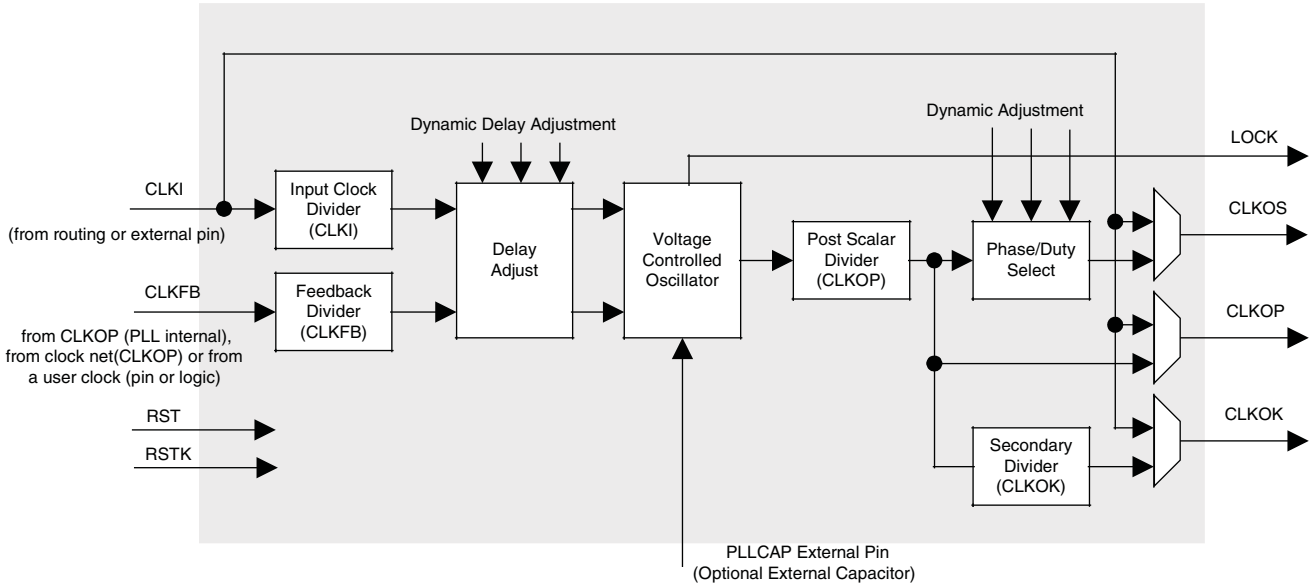
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5qn208c

Figure 2-5. General Purpose PLL (GPLL) Diagram



Standard PLL (SPLL)

Some of the larger devices have two to six Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see the list of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

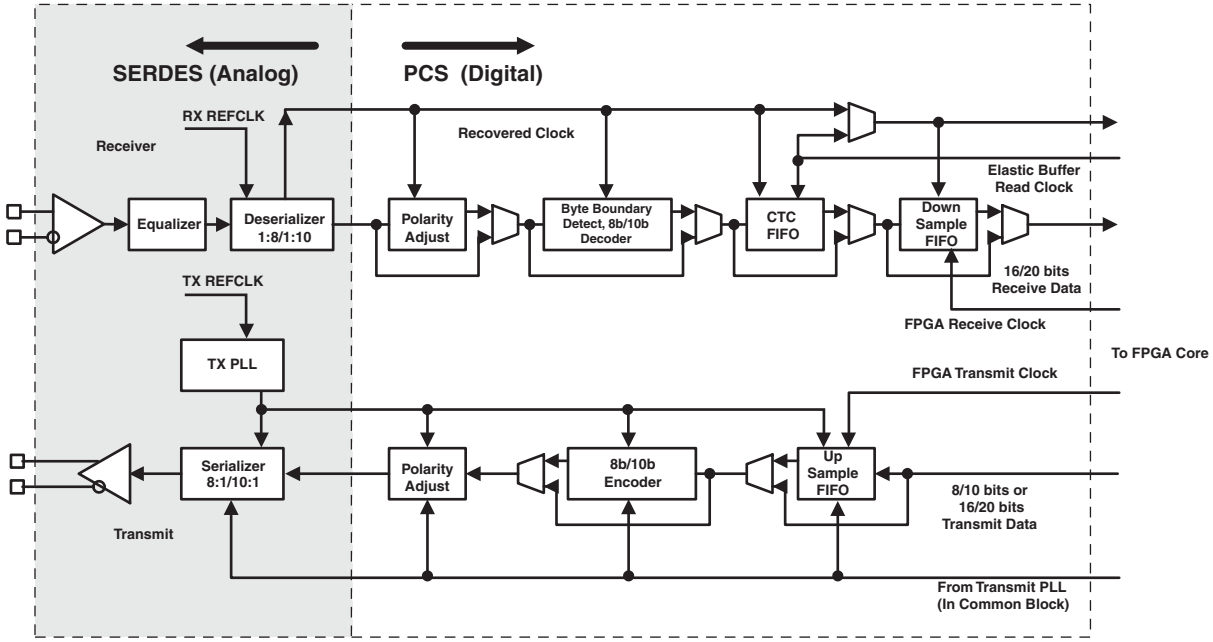
Table 2-4. GPLL and SPLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE[1]	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR[1]	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG[1]	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0][1]	I	Dynamic Delay Input
DPA MODES	I	DPA (Dynamic Phase Adjust/Duty Cycle Select) mode
DPHASE [3:0]	I	DPA Phase Adjust inputs
DDDUTY [3:0]	—	DPA Duty Cycle Select inputs

1. These signals are not available in SPLL.

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel also have their own independent power supplies. In addition, there are separate power supplies for PLL, terminating resistor per quad.

Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS



PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With Diamond, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information about SERDES, please see the list of additional technical documentation at the end of this data sheet.

MLVDS

The LatticeECP2/M devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Multipoint Low Voltage Differential Signaling)

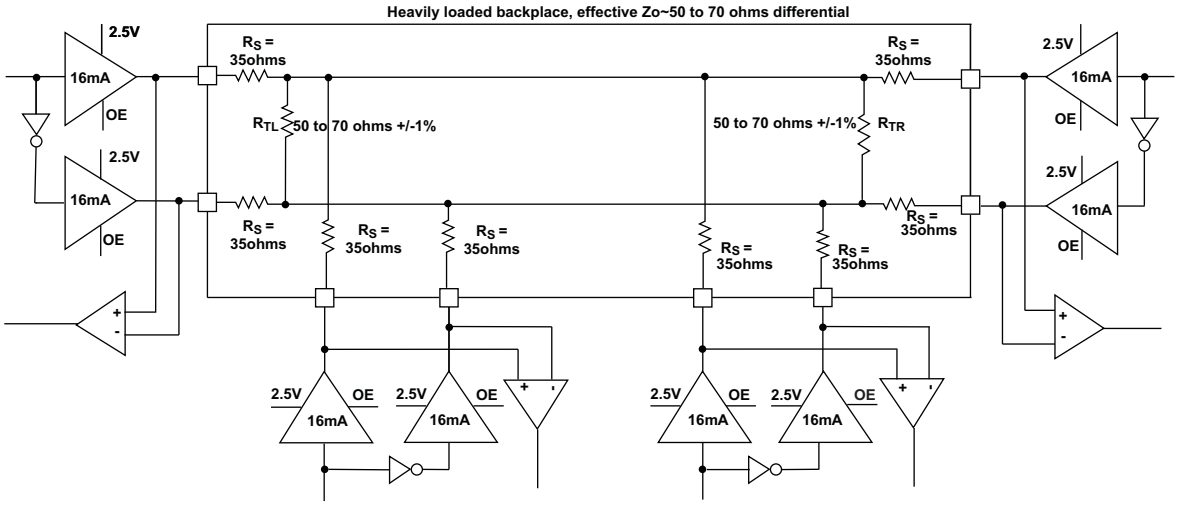


Table 3-6. MLVDS DC Conditions[1]

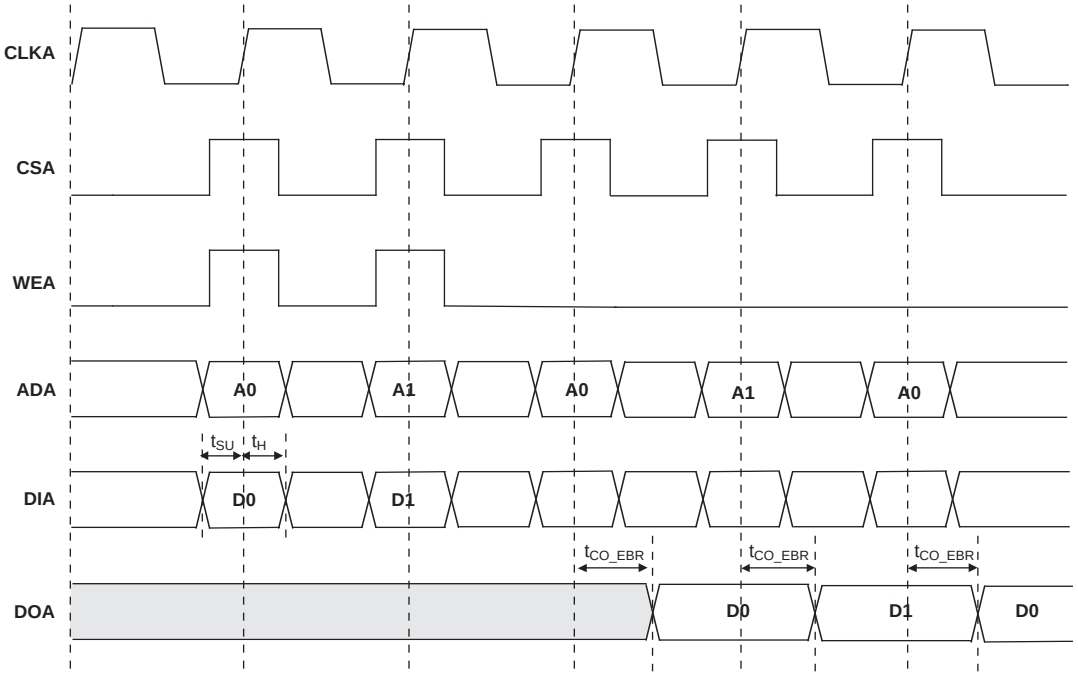
Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

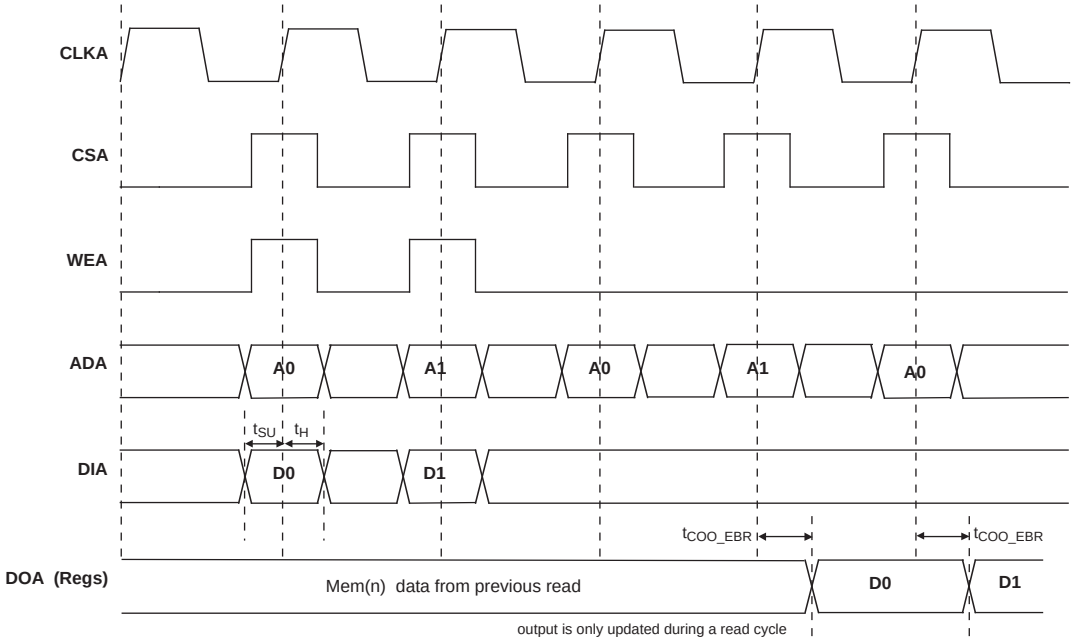
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB7	PB13B	5	BDQ15	C	PB22B	5	BDQ24	C
Y8	PB16A	5	BDQ15	T	PB25A	5	BDQ24	T
GNDIO	GNDIO5	-			GNDIO	-		
W9	PB15A	5	BDQS15	T	PB24A	5	BDQS24	T
AA8	PB16B	5	BDQ15	C	PB25B	5	BDQ24	C
V9	PB15B	5	BDQ15	C	PB24B	5	BDQ24	C
AB8	PB18A	5	BDQ15	T	PB27A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
W10	PB17A	5	BDQ15	T	PB26A	5	BDQ24	T
AA9	PB18B	5	BDQ15	C	PB27B	5	BDQ24	C
V10	PB17B	5	BDQ15	C	PB26B	5	BDQ24	C
GNDIO	GNDIO5	-			GNDIO	-		
Y10	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AB9	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AB10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
AB11	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U10	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA11	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
U11	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB12	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
Y11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AA12	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W11	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AB13	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AB14	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y12	PB32A	4	BDQ33	T	PB41A	4	BDQ42	T
W12	PB32B	4	BDQ33	C	PB41B	4	BDQ42	C
VCCIO	VCCIO4	4			VCCIO4	4		
U12	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
V12	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
U13	PB34A	4	BDQ33	T	PB43A	4	BDQ42	T
GNDIO	GNDIO4	-			GNDIO4	-		
AA13	PB33A	4	BDQS33	T	PB42A	4	BDQS42	T
U14	PB34B	4	BDQ33	C	PB43B	4	BDQ42	C
Y13	PB33B	4	BDQ33	C	PB42B	4	BDQ42	C
AB16	PB36A	4	BDQ33	T	PB45A	4	BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB15	PB35A	4	BDQ33	T	PB44A	4	BDQ42	T
AB17	PB36B	4	BDQ33	C	PB45B	4	BDQ42	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C2	PT3A	0		T	PT3A	0		T
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
G10	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
H8	VCCIO0	0			VCCIO0	0		
G11	VCCIO1	1			VCCIO1	1		
G12	VCCIO1	1			VCCIO1	1		
G13	VCCIO1	1			VCCIO1	1		
G14	VCCIO1	1			VCCIO1	1		
H14	VCCIO2	2			VCCIO2	2		
H15	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K16	VCCIO2	2			VCCIO2	2		
L16	VCCIO3	3			VCCIO3	3		
M16	VCCIO3	3			VCCIO3	3		
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
H16	NC	-			NC	-		
H20	NC	-			NC	-		
H18	NC	-			NC	-		
K6	NC	-			NC	-		
J16	NC	-			NC	-		
N18	VCC	-			VCC	-		
N6	VCC	-			VCC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U3	PL55A	6	LDQ56	T	PL74A	6	LDQ75	T
U4	PL55B	6	LDQ56	C	PL74B	6	LDQ75	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL56A	6	LDQS56	T (LVDS)*	PL75A	6	LDQS75	T (LVDS)*
W1	PL56B	6	LDQ56	C (LVDS)*	PL75B	6	LDQ75	C (LVDS)*
R7	PL57A	6	LDQ56	T	PL76A	6	LDQ75	T
VCCIO	VCCIO6	6			VCCIO	6		
T7	PL57B	6	LDQ56	C	PL76B	6	LDQ75	C
V4	PL58A	6	LDQ56	T (LVDS)*	PL77A	6	LDQ75	T (LVDS)*
V3	PL58B	6	LDQ56	C (LVDS)*	PL77B	6	LDQ75	C (LVDS)*
AA2	PL59A	6	LDQ56	T	PL78A	6	LDQ75	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL59B	6	LDQ56	C	PL78B	6	LDQ75	C
U7	TCK	-			TCK	-		
U5	TDI	-			TDI	-		
V5	TMS	-			TMS	-		
V6	TDO	-			TDO	-		
T8	VCCJ	-			VCCJ	-		
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO	5		
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO	5		
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
GNDIO	GNDIO5	-			GNDIO5	-		
VCCIO	VCCIO5	5			VCCIO	5		
W7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
W8	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
Y6	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
Y7	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AA7	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
AB7	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K8	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L12	GND	-			GND	-		
L13	GND	-			GND	-		
L15	GND	-			GND	-		
L8	GND	-			GND	-		
M10	GND	-			GND	-		
M11	GND	-			GND	-		
M12	GND	-			GND	-		
M13	GND	-			GND	-		
M15	GND	-			GND	-		
M8	GND	-			GND	-		
N10	GND	-			GND	-		
N11	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N15	GND	-			GND	-		
N8	GND	-			GND	-		
P14	GND	-			GND	-		
P20	GND	-			GND	-		
P3	GND	-			GND	-		
P9	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R12	GND	-			GND	-		
R13	GND	-			GND	-		
U17	GND	-			GND	-		
U6	GND	-			GND	-		
W2	GND	-			GND	-		
W21	GND	-			GND	-		
Y14	GND	-			GND	-		
Y9	GND	-			GND	-		
A1	GND	-			GND	-		
N18	VCCPLL	-			VCCPLL	-		
K6	NC	-			VCCPLL	-		
N6	VCCPLL	-			VCCPLL	-		
J16	NC	-			VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
P25	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2		
P23	PR51A	2	RDQ54	T
P27	PR50B	2	RDQ54	C (LVDS)*
P28	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-		
VCCIO	VCCIO2	2		
N24	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
N26	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
N23	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
N25	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2		
P29	PR37B	2	RDQ37	C (LVDS)*
P30	PR37A	2	RDQS37	T (LVDS)*
M26	PR36B	2	RDQ37	C
GND	GNDIO2	-		
M24	PR36A	2	RDQ37	T
N29	PR35B	2	RDQ37	C (LVDS)*
N30	PR35A	2	RDQ37	T (LVDS)*
M25	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2		
M23	PR34A	2	RDQ37	T
M27	PR33B	2	RDQ37	C (LVDS)*
M28	PR33A	2	RDQ37	T (LVDS)*
L26	PR32B	2	RDQ29	C
GND	GNDIO2	-		
L24	PR32A	2	RDQ29	T
M29	PR31B	2	RDQ29	C (LVDS)*
M30	PR31A	2	RDQ29	T (LVDS)*
L25	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2		
L23	PR30A	2	RDQ29	T
L27	PR29B	2	RDQ29	C (LVDS)*
L28	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-		
K24	PR28B	2	RDQ29	C
K26	PR28A	2	RDQ29	T
L29	PR27B	2	RDQ29	C (LVDS)*
L30	PR27A	2	RDQ29	T (LVDS)*
VCCIO	VCCIO2	2		
K23	PR26B	2	RDQ29	C
K25	PR26A	2	RDQ29	T
K27	PR25B	2	RDQ29	C (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R19	GND	-		
R20	GND	-		
T11	GND	-		
T12	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T19	GND	-		
T20	GND	-		
U11	GND	-		
U12	GND	-		
U13	GND	-		
U14	GND	-		
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U19	GND	-		
U20	GND	-		
V12	GND	-		
V13	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V18	GND	-		
V19	GND	-		
V28	GND	-		
V3	GND	-		
W12	GND	-		
W13	GND	-		
W14	GND	-		
W15	GND	-		
W16	GND	-		
W17	GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
C12	URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
E13	PT55B	1		C
D12	PT55A	1		T
GNDIO	GNDIO1	-		
A9	PT54B	1		C
A8	PT54A	1		T
A7	PT53B	1		C
A6	PT53A	1		T
VCCIO	VCCIO1	1		
E12	PT52B	1		C
F12	PT52A	1		T
A5	PT51B	1		C
A4	PT51A	1		T
GNDIO	GNDIO1	-		
B7	PT50B	1		C
B8	PT50A	1		T
G11	PT49B	1		C
E11	PT49A	1		T
VCCIO	VCCIO1	1		
D11	PT48B	1	VREF2_1	C
D10	PT48A	1	VREF1_1	T
G10	PT47B	1	PCLKC1_0	C
F11	PT47A	1	PCLKT1_0	T
G9	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
F9	PT46A	0	PCLKT0_0	T
C9	PT45B	0	VREF2_0	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P8	PL45A	6	LDQ48	T	PL49A	6	LDQ52	T
R6	PL45B	6	LDQ48	C	PL49B	6	LDQ52	C
VCCIO	VCCIO6	6			VCCIO6	6		
T1	PL46A	6	LDQ48	T (LVDS)*	PL50A	6	LDQ52	T*
U1	PL46B	6	LDQ48	C (LVDS)*	PL50B	6	LDQ52	C*
R7	PL47A	6	LDQ48	T	PL51A	6	LDQ52	T
T5	PL47B	6	LDQ48	C	PL51B	6	LDQ52	C
GNDIO	GNDIO6	-			GNDIO6	-		
U3	PL48A	6	LDQS48	T (LVDS)*	PL52A	6	LDQS52	T*
U4	PL48B	6	LDQ48	C (LVDS)*	PL52B	6	LDQ52	C*
U5	PL49A	6	LDQ48	T	PL53A	6	LDQ52	T
VCCIO	VCCIO6	6			VCCIO6	6		
U6	PL49B	6	LDQ48	C	PL53B	6	LDQ52	C
U2	PL50A	6	LDQ48	T (LVDS)*	PL54A	6	LDQ52	T*
V1	PL50B	6	LDQ48	C (LVDS)*	PL54B	6	LDQ52	C*
W2	PL51A	6	LDQ48	T	PL55A	6	LDQ52	T
GNDIO	GNDIO6	-			GNDIO6	-		
V2	PL51B	6	LDQ48	C	PL55B	6	LDQ52	C
V4	PL55A	6	LDQ57	T (LVDS)*	PL59A	6		T*
VCCIO	VCCIO6	6			VCCIO6	6		
V3	PL55B	6	LDQ57	C (LVDS)*	PL59B	6		C*
-	-	-			GNDIO6	-		
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	PL62A	6	LLM0_GPLLT_IN_A	T*
GNDIO	GNDIO6	-			GNDIO6	-		
W3	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	PL62B	6	LLM0_GPLLC_IN_A	C*
W1	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	PL63A	6	LLM0_GPLLT_FB_A	T
Y1	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	PL63B	6	LLM0_GPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
AA1	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*	PL64A	6	LLM0_GDLLT_IN_A	T*
AB1	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	PL64B	6	LLM0_GDLLC_IN_A	C*
U7	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T	PL65A	6	LLM0_GDLLT_FB_A	T
V6	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	PL65B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	-			GNDIO6	-		
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
W5	PL62A	6	LDQ66	T (LVDS)*	PL67A	6	LDQ71	T*
Y4	PL62B	6	LDQ66	C (LVDS)*	PL67B	6	LDQ71	C*
U8	PL63A	6	LDQ66	T	PL68A	6	LDQ71	T
W6	PL63B	6	LDQ66	C	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6			VCCIO6	6		
Y3	PL64A	6	LDQ66	T (LVDS)*	PL69A	6	LDQ71	T*
AA3	PL64B	6	LDQ66	C (LVDS)*	PL69B	6	LDQ71	C*
V7	NC	-			PL70A	6	LDQ71	T
Y5	PL65B	6	LDQ66	C	PL70B	6	LDQ71	C
GNDIO	GNDIO6	-			GNDIO6	-		
AB2	PL66A	6	LDQS66	T (LVDS)*	PL71A	6	LDQS71	T*
AA4	PL66B	6	LDQ66	C (LVDS)*	PL71B	6	LDQ71	C*
Y6	PL67A	6	LDQ66	T	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6			VCCIO6	6		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J16	PT51B	1		C	PT60B	1		C
G15	PT51A	1		T	PT60A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
C16	PT50B	1		C	PT59B	1		C
D16	PT50A	1		T	PT59A	1		T
J15	PT49B	1		C	PT58B	1		C
H15	PT49A	1		T	PT58A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A15	PT48B	1	VREF2_1	C	PT57B	1	VREF2_1	C
B15	PT48A	1	VREF1_1	T	PT57A	1	VREF1_1	T
F15	PT47B	1	PCLKC1_0	C	PT56B	1	PCLKC1_0	C
E16	PT47A	1	PCLKT1_0	T	PT56A	1	PCLKT1_0	T
C15	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
D15	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T
C14	PT45B	0	VREF2_0	C	PT54B	0	VREF2_0	C
E15	PT45A	0	VREF1_0	T	PT54A	0	VREF1_0	T
G14	PT44B	0		C	PT53B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
J14	PT44A	0		T	PT53A	0		T
F14	PT43B	0		C	PT52B	0		C
H14	PT43A	0		T	PT52A	0		T
A14	PT42B	0		C	PT51B	0		C
B14	PT42A	0		T	PT51A	0		T
D13	PT41B	0		C	PT50B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		
F13	PT41A	0		T	PT50A	0		T
G13	PT40B	0		C	PT49B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
J11	PT40A	0		T	PT49A	0		T
D4	PT38B	0		C	PT47B	0		C
D5	PT38A	0		T	PT47A	0		T
E5	PT37B	0		C	PT46B	0		C
F6	PT37A	0		T	PT46A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT34B	0		C	PT43B	0		C
D8	PT34A	0		T	PT43A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
J13	PT32B	0		C	PT41B	0		C
G11	PT32A	0		T	PT41A	0		T
H13	PT31B	0		C	PT40B	0		C
H12	PT31A	0		T	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
E8	PT30B	0		C	PT39B	0		C
D9	PT30A	0		T	PT39A	0		T
D12	PT28B	0		C	PT37B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K3	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
N10	VCCIO7	7			VCCIO7	7		
N3	VCCIO7	7			VCCIO7	7		
P10	VCCIO7	7			VCCIO7	7		
R6	VCCIO7	7			VCCIO7	7		
AA25	VCCIO8	8			VCCIO8	8		
AD28	VCCIO8	8			VCCIO8	8		
AA10	VCCAUX	-			VCCAUX	-		
AA11	VCCAUX	-			VCCAUX	-		
AA20	VCCAUX	-			VCCAUX	-		
AA21	VCCAUX	-			VCCAUX	-		
K10	VCCAUX	-			VCCAUX	-		
K11	VCCAUX	-			VCCAUX	-		
K20	VCCAUX	-			VCCAUX	-		
K21	VCCAUX	-			VCCAUX	-		
L10	VCCAUX	-			VCCAUX	-		
L11	VCCAUX	-			VCCAUX	-		
L20	VCCAUX	-			VCCAUX	-		
L21	VCCAUX	-			VCCAUX	-		
Y10	VCCAUX	-			VCCAUX	-		
Y11	VCCAUX	-			VCCAUX	-		
Y20	VCCAUX	-			VCCAUX	-		
Y21	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A13	GND	-			GND	-		
A18	GND	-			GND	-		
A24	GND	-			GND	-		
A30	GND	-			GND	-		
A7	GND	-			GND	-		
AA14	GND	-			GND	-		
AA15	GND	-			GND	-		
AA16	GND	-			GND	-		
AA17	GND	-			GND	-		
AA24	GND	-			GND	-		
AA27	GND	-			GND	-		
AA4	GND	-			GND	-		
AB24	GND	-			GND	-		
AB7	GND	-			GND	-		
AD12	GND	-			GND	-		
AD19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE22	GND	-			GND	-		
AE27	GND	-			GND	-		
AE4	GND	-			GND	-		
AE9	GND	-			GND	-		
AF14	GND	-			GND	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
U7	PL60A	6	VREF2_6/LDQ63	T
T8	PL60B	6	VREF1_6/LDQ63	C
R3	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6		
R2	PL61B	6	LDQ63	C (LVDS)*
R1	PL62A	6	LDQ63	T
T1	PL62B	6	LDQ63	C
GNDIO	GNDIO6	-		
VCCIO	VCCIO6	6		
T3	PL65A	6	LLM4_SPLLT_IN_A/LDQ63	T (LVDS)*
T2	PL65B	6	LLM4_SPLLC_IN_A/LDQ63	C (LVDS)*
U9	PL66A	6	LLM4_SPLLT_FB_A/LDQ63	T
U8	PL66B	6	LLM4_SPLLC_FB_A/LDQ63	C
GNDIO	GNDIO6	-		
U5	PL68A	6	LDQ72	T (LVDS)*
U4	PL68B	6	LDQ72	C (LVDS)*
V9	PL69A	6	LDQ72	T
V7	PL69B	6	LDQ72	C
VCCIO	VCCIO6	6		
U3	PL70A	6	LDQ72	T (LVDS)*
U2	PL70B	6	LDQ72	C (LVDS)*
V8	PL71A	6	LDQ72	T
U6	PL71B	6	LDQ72	C
GNDIO	GNDIO6	-		
U1	PL72A	6	LDQS72	T (LVDS)*
V2	PL72B	6	LDQ72	C (LVDS)*
V5	PL73A	6	LDQ72	T
VCCIO	VCCIO6	6		
V6	PL73B	6	LDQ72	C
V1	PL74A	6	LDQ72	T (LVDS)*
W1	PL74B	6	LDQ72	C (LVDS)*
W5	PL75A	6	LDQ72	T
GNDIO	GNDIO6	-		
W6	PL75B	6	LDQ72	C
W3	PL77A	6	LDQ81	T (LVDS)*
W4	PL77B	6	LDQ81	C (LVDS)*
W2	PL78A	6	LDQ81	T
Y4	PL78B	6	LDQ81	C
Y1	PL79A	6	LDQ81	T (LVDS)*
VCCIO	VCCIO6	6		
Y2	PL79B	6	LDQ81	C (LVDS)*
Y5	PL80A	6	LDQ81	T
Y6	PL80B	6	LDQ81	C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AF11	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AJ14	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4		
AK14	PB67B	4	PCLKC4_0/BDQ69	C
AK15	PB68A	4	VREF2_4/BDQ69	T
AK16	PB68B	4	VREF1_4/BDQ69	C
AF18	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-		
AD16	PB69B	4	BDQ69	C
AJ15	PB70A	4	BDQ69	T
AG16	PB70B	4	BDQ69	C
AE17	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4		
AC17	PB71B	4	BDQ69	C
AH16	PB72A	4	BDQ69	T
AK17	PB72B	4	BDQ69	C
AG20	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-		
AG21	PB73B	4	BDQ69	C
AG18	PB74A	4	BDQ78	T
AJ16	PB74B	4	BDQ78	C
AF21	PB75A	4	BDQ78	T
AG22	PB75B	4	BDQ78	C
AD17	PB76A	4	BDQ78	T
AF19	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
AH17	PB80A	4	BDQ78	T
AJ17	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4		
AF26	PB82A	4	BDQ78	T
AE25	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-		
AD24	PB92A	4	BDQ96	T
AE24	PB92B	4	BDQ96	C
AD18	PB93A	4	BDQ96	T
AC18	PB93B	4	BDQ96	C
AE18	PB94A	4	BDQ96	T
AG19	PB94B	4	BDQ96	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U20	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V27	GND	-		
V4	GND	-		
W23	GND	-		
W8	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
AA26	NC	-		
AB10	NC	-		
AB11	NC	-		
AB12	NC	-		
AB13	NC	-		
AB14	NC	-		
AB15	NC	-		
AB16	NC	-		
AB17	NC	-		
AB19	NC	-		
AB20	NC	-		
AB21	NC	-		
AB9	NC	-		
AC10	NC	-		
AC11	NC	-		
AC21	NC	-		
AC22	NC	-		
AC8	NC	-		
AC9	NC	-		
AD21	NC	-		
AD22	NC	-		
AD4	NC	-		
AD5	NC	-		
AD6	NC	-		
AD7	NC	-		
AD8	NC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R21	VCC	-			VCC	-		
R22	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T21	VCC	-			VCC	-		
U14	VCC	-			VCC	-		
U21	VCC	-			VCC	-		
V14	VCC	-			VCC	-		
V21	VCC	-			VCC	-		
W14	VCC	-			VCC	-		
W21	VCC	-			VCC	-		
Y13	VCC	-			VCC	-		
Y14	VCC	-			VCC	-		
Y21	VCC	-			VCC	-		
Y22	VCC	-			VCC	-		
C12	VCCIO0	0			VCCIO0	0		
C16	VCCIO0	0			VCCIO0	0		
E14	VCCIO0	0			VCCIO0	0		
H12	VCCIO0	0			VCCIO0	0		
H16	VCCIO0	0			VCCIO0	0		
M14	VCCIO0	0			VCCIO0	0		
M15	VCCIO0	0			VCCIO0	0		
C19	VCCIO1	1			VCCIO1	1		
C23	VCCIO1	1			VCCIO1	1		
E21	VCCIO1	1			VCCIO1	1		
H19	VCCIO1	1			VCCIO1	1		
H23	VCCIO1	1			VCCIO1	1		
M20	VCCIO1	1			VCCIO1	1		
M21	VCCIO1	1			VCCIO1	1		
G32	VCCIO2	2			VCCIO2	2		
K28	VCCIO2	2			VCCIO2	2		
K32	VCCIO2	2			VCCIO2	2		
N27	VCCIO2	2			VCCIO2	2		
N32	VCCIO2	2			VCCIO2	2		
P23	VCCIO2	2			VCCIO2	2		
R23	VCCIO2	2			VCCIO2	2		
T27	VCCIO2	2			VCCIO2	2		
T32	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
AB27	VCCIO3	3			VCCIO3	3		
AB32	VCCIO3	3			VCCIO3	3		
AE28	VCCIO3	3			VCCIO3	3		
AE32	VCCIO3	3			VCCIO3	3		
AH32	VCCIO3	3			VCCIO3	3		
W27	VCCIO3	3			VCCIO3	3		
W32	VCCIO3	3			VCCIO3	3		
Y23	VCCIO3	3			VCCIO3	3		
AC20	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
AG19	VCCIO4	4			VCCIO4	4		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F21	GND	-			GND	-		
G31	GND	-			GND	-		
G4	GND	-			GND	-		
J12	GND	-			GND	-		
J16	GND	-			GND	-		
J19	GND	-			GND	-		
J23	GND	-			GND	-		
K27	GND	-			GND	-		
K31	GND	-			GND	-		
K4	GND	-			GND	-		
K8	GND	-			GND	-		
M16	GND	-			GND	-		
M17	GND	-			GND	-		
M18	GND	-			GND	-		
M19	GND	-			GND	-		
N16	GND	-			GND	-		
N17	GND	-			GND	-		
N18	GND	-			GND	-		
N19	GND	-			GND	-		
N26	GND	-			GND	-		
N31	GND	-			GND	-		
N4	GND	-			GND	-		
N9	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R19	GND	-			GND	-		
T12	GND	-			GND	-		
T13	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T19	GND	-			GND	-		
T20	GND	-			GND	-		
T22	GND	-			GND	-		
T23	GND	-			GND	-		
T26	GND	-			GND	-		
T31	GND	-			GND	-		
T4	GND	-			GND	-		
T9	GND	-			GND	-		
U12	GND	-			GND	-		
U13	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U19	GND	-			GND	-		
U20	GND	-			GND	-		