



Welcome to [E·XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5qn208i

Features

■ High Logic Density for System Integration

- 6K to 95K LUTs
- 90 to 583 I/Os

■ Embedded SERDES (LatticeECP2M Only)

- Data Rates 250 Mbps to 3.125 Gbps
- Up to 16 channels per device
PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.

■ sysDSP™ Block

- 3 to 42 blocks for high performance multiply and accumulate
- Each block supports
 - One 36x36, four 18x18 or eight 9x9 multipliers

■ Flexible Memory Resources

- 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
 - 18Kbit block
 - Single, pseudo dual and true dual port
 - Byte Enable Mode support
- 12K to 202Kbits distributed RAM
 - Single port and pseudo dual port

■ sysCLOCK Analog PLLs and DLLs

- Two GPLLs and up to six SPLLS per device
 - Clock multiply, divide, phase & delay adjust
 - Dynamic PLL adjustment
- Two general purpose DLLs per device

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- Source synchronous standards support
 - SPI4.2, SFI4 (DDR Mode), XGMII
 - High Speed ADC/DAC devices
- Dedicated DDR and DDR2 memory support
 - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
- Dedicated DQS support

■ Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces

- LVTTTL and LVCMOS 33/25/18/15/12
- SSTL 3/2/18 I, II
- HSTL15 I and HSTL18 I, II
- PCI and Differential HSTL, SSTL
- LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL

■ Flexible Device Configuration

- 1149.1 Boundary Scan compliant
- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual boot images supported
- TransFR™ I/O for simple field updates
- Soft Error Detect macro embedded

■ Optional Bitstream Encryption (LatticeECP2/M “S” Versions Only)

■ System Level Support

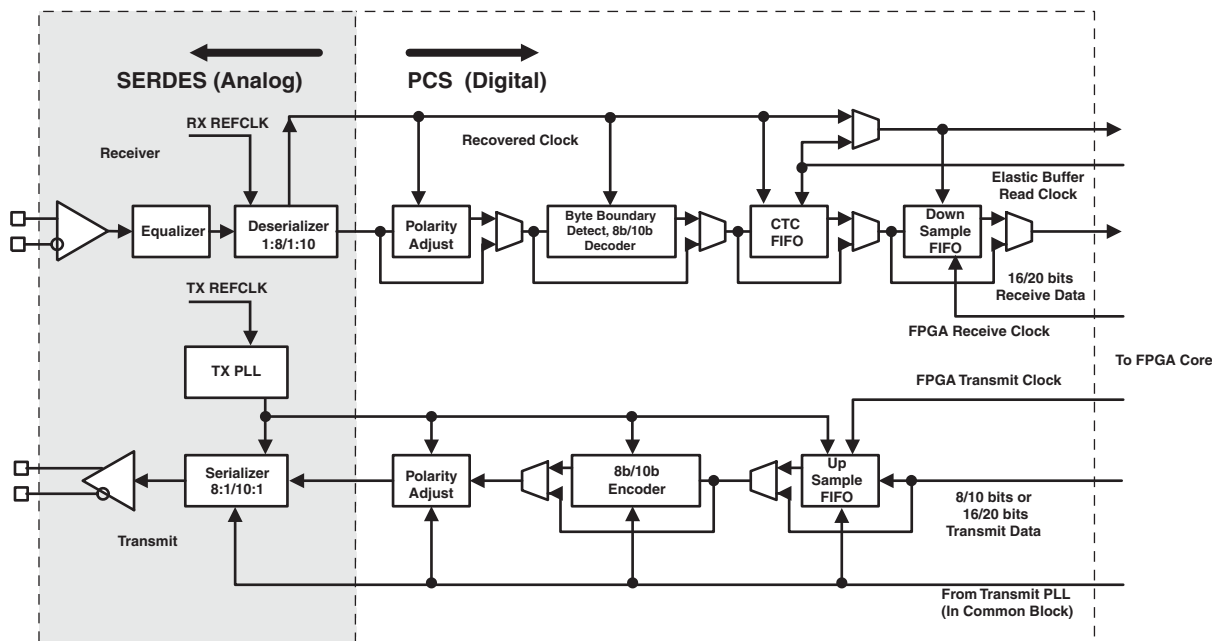
- ispTRACY™ internal logic analyzer capability
- On-chip oscillator for initialization & general use
- 1.2V power supply

Table 1-1. LatticeECP2 (Including “S-Series”) Family Selection

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel also have their own independent power supplies. In addition, there are separate power supplies for PLL, terminating resistor per quad.

Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS



PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With Diamond, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information about SERDES, please see the list of additional technical documentation at the end of this data sheet.

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	420	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	20	—	420	MHz
		With external capacitor ⁵	5	—	50	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.156	—	210	MHz
		With external capacitor ⁵	0.039	—	25	MHz
f _{VCO}	PLL VCO Frequency		640	—	1280	MHz
f _{PFD}	Phase Detector Input Frequency	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	50	MHz
AC Characteristics						
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{PH} ⁴	Output Phase Accuracy		—	—	±0.05	UI
t _{OPJIT} ¹	Output Clock Period Jitter	f _{OUT} ≥ 100 MHz	—	—	±125	ps
		50 ≤ f _{OUT} < 100 MHz	—	—	0.025	UIPP
		f _{OUT} < 50 MHz	—	—	0.04	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t _W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t _{LOCK} ²	PLL Lock-in Time	Without external capacitor	—	—	150	μs
		With external capacitor ⁵	—	—	500	μs
t _{PA}	Programmable Delay Unit		85	130	360	ps
t _{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t _{FBKDLY}	External Feedback Delay		—	—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t _{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor ⁵	20	—	—	μs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

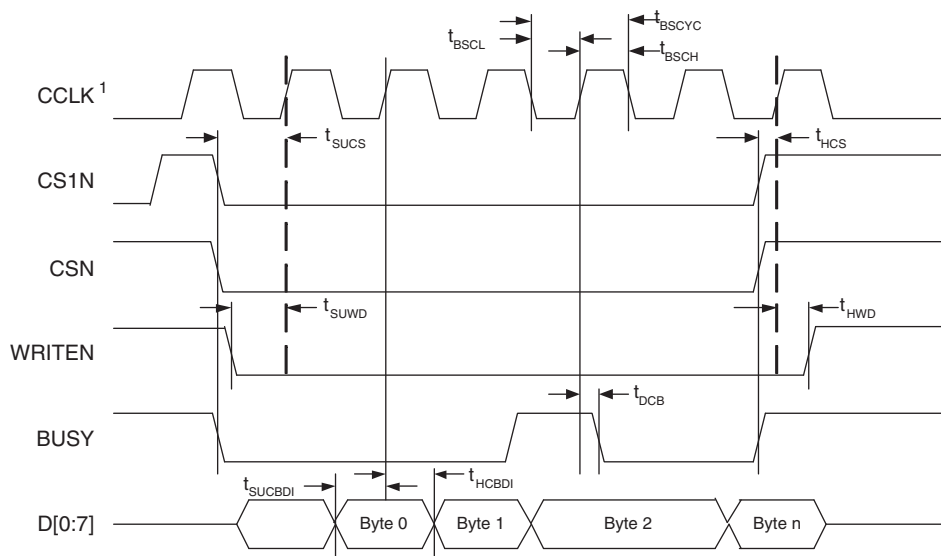
3. Using LVDS output buffers.

4. Relative to CLKOP.

5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.

6. $f_{OUT} (max) = f_{IN} * 10$ for $f_{IN} < 5$ MHz.

Figure 3-15. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-16. sysCONFIG Slave Serial Port Timing

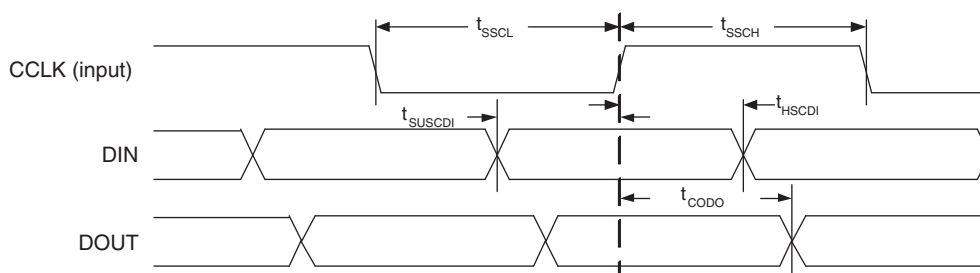
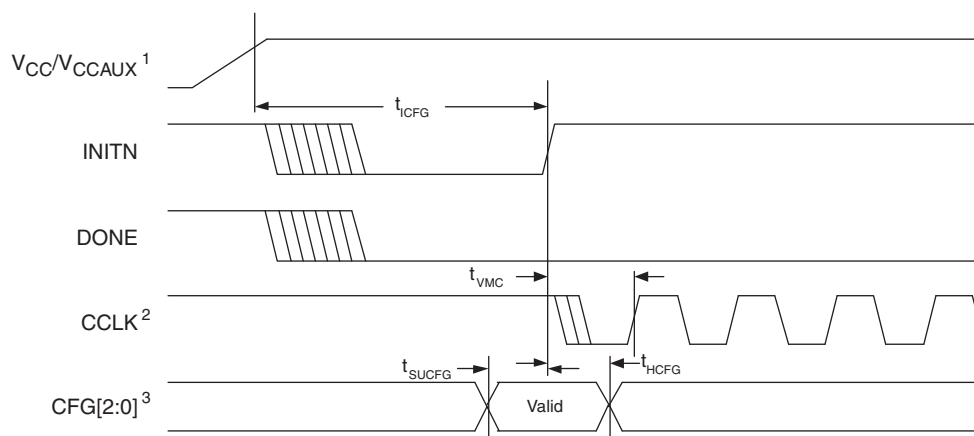


Figure 3-17. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX} , whichever is the last to reach its V_{MIN} .
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See “Typical sysI/O I/O Behavior During Power-up” for more information about I/O behavior during power-up.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V _{CCPLL}	—	PLL supply pins. Should be tied to V _{CC} even when the corresponding PLL is unused.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES ⁴	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP ⁴	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V _{CCPLL}	—	Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A ⁵	I	Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A ⁵	I	Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.

LatticeECP2M Power Supply and NC (Cont.)

Signal	1152 fpBGA
V _{CC}	AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22
V _{CCIO0}	C12, C16, E14, H12, H16, M14, M15
V _{CCIO1}	C19, C23, E21, H19, H23, M20, M21
V _{CCIO2}	G32, K28, K32, N27, N32, P23, R23, T27, T32
V _{CCIO3}	AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23
V _{CCIO4}	AC20, AC21, AG19, AG23, AK21, AM19, AM23
V _{CCIO5}	AC14, AC15, AG12, AG16, AK14, AM12, AM16
V _{CCIO6}	AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12
V _{CCIO7}	G3, K3, K7, N3, N8, P12, R12, T3, T8
V _{CCIO8}	AD28, AG32
V _{CCJ}	AK3
V _{CCAUX}	AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23
V _{CCPLL}	R15, R20, Y15, Y20
SERDES Power ³	D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7
GND ¹	A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19
NC ²	LFE2M70: H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 LFE2M100: A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2M Density Migration](#) for more details.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
5	GND	-			GND	-			
6	PL6A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ16	T (LVDS)*	
7	VCCAUX	-			VCCAUX	-			
8	PL6B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ16	C (LVDS)*	
9	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
10	VCCIO7	7			VCCIO7	7			
11	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
12	VCC	-			VCC	-			
13	GND	-			GND	-			
14	VCCIO7	7			VCCIO7	7			
15	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
16	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
17	GND	-			GND	-			
18	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
19	VCC	-			VCC	-			
20	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
21	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
22	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*	
23	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T	
24	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C	
25	GND	-			GND	-			
26	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*	
27	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*	
28	VCC	-			VCC	-			
29	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
30	VCCAUX	-			VCCAUX	-			
31	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*	
32	GND	-			GND	-			
33	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T	
34	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*	
35	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C	
36	PL23A	6			PL33A	6	LDQ34		
37	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*	
38	VCCIO6	6			VCCIO6	6			
39	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*	
40	VCC	-			VCC	-			
41	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*	
42	GND	-			GND	-			
43	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
44	VCCIO6	6			VCCIO6	6			
45	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
184	GND	-			GND	-			
185	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T	
186	PT26B	0		C	PT36B	0		C	
187	PT26A	0		T	PT36A	0		T	
188	VCC	-			VCC	-			
189	PT20B	0		C	PT30B	0		C	
190	VCCAUX	-			VCCAUX	-			
191	PT20A	0		T	PT30A	0		T	
192	GND	-			GND	-			
193	PT18B	0		C	PT26B	0		C	
194	PT18A	0		T	PT26A	0		T	
195	VCCIO0	0			VCCIO0	0			
196	PT16B	0		C	PT20B	0		C	
197	PT16A	0		T	PT20A	0		T	
198	VCC	-			VCC	-			
199	PT12B	0		C	PT12B	0		C	
200	PT12A	0		T	PT12A	0		T	
201	GND	-			GND	-			
202	PT8B	0		C	PT8B	0		C	
203	PT8A	0		T	PT8A	0		T	
204	PT6B	0		C	PT6B	0		C	
205	PT6A	0		T	PT6A	0		T	
206	VCCIO0	0			VCCIO0	0			
207	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
208	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
R8	VCCIO6	6			VCCIO6	6			
J8	VCCIO7	7			VCCIO7	7			
K7	VCCIO7	7			VCCIO7	7			
L7	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
P15	VCCIO8	8			VCCIO8	8			
R15	VCCIO8	8			VCCIO8	8			
C5	VCCAUX	-			VCCAUX	-			
D11	VCCAUX	-			VCCAUX	-			
E17	VCCAUX	-			VCCAUX	-			
E6	VCCAUX	-			VCCAUX	-			
F13	VCCAUX	-			VCCAUX	-			
G18	VCCAUX	-			VCCAUX	-			
G5	VCCAUX	-			VCCAUX	-			
K5	VCCAUX	-			VCCAUX	-			
M17	VCCAUX	-			VCCAUX	-			
P17	VCCAUX	-			VCCAUX	-			
R5	VCCAUX	-			VCCAUX	-			
V11	VCCAUX	-			VCCAUX	-			
V13	VCCAUX	-			VCCAUX	-			
V15	VCCAUX	-			VCCAUX	-			
V7	VCCAUX	-			VCCAUX	-			
V8	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A22	GND	-			GND	-			
AA19	GND	-			GND	-			
AA4	GND	-			GND	-			
AB1	GND	-			GND	-			
AB22	GND	-			GND	-			
B19	GND	-			GND	-			
B4	GND	-			GND	-			
C14	GND	-			GND	-			
C9	GND	-			GND	-			
D2	GND	-			GND	-			
D21	GND	-			GND	-			
F17	GND	-			GND	-			
F6	GND	-			GND	-			
H10	GND	-			GND	-			
H11	GND	-			GND	-			
H12	GND	-			GND	-			
H13	GND	-			GND	-			
J14	GND	-			GND	-			
J20	GND	-			GND	-			
J3	GND	-			GND	-			

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
J9	GND	-			GND	-			
K10	GND	-			GND	-			
K11	GND	-			GND	-			
K12	GND	-			GND	-			
K13	GND	-			GND	-			
K15	GND	-			GND	-			
K8	GND	-			GND	-			
L10	GND	-			GND	-			
L11	GND	-			GND	-			
L12	GND	-			GND	-			
L13	GND	-			GND	-			
L15	GND	-			GND	-			
L8	GND	-			GND	-			
M10	GND	-			GND	-			
M11	GND	-			GND	-			
M12	GND	-			GND	-			
M13	GND	-			GND	-			
M15	GND	-			GND	-			
M8	GND	-			GND	-			
N10	GND	-			GND	-			
N11	GND	-			GND	-			
N12	GND	-			GND	-			
N13	GND	-			GND	-			
N15	GND	-			GND	-			
N8	GND	-			GND	-			
P14	GND	-			GND	-			
P20	GND	-			GND	-			
P3	GND	-			GND	-			
P9	GND	-			GND	-			
R10	GND	-			GND	-			
R11	GND	-			GND	-			
R12	GND	-			GND	-			
R13	GND	-			GND	-			
U17	GND	-			GND	-			
U6	GND	-			GND	-			
W2	GND	-			GND	-			
W21	GND	-			GND	-			
Y14	GND	-			GND	-			
Y9	GND	-			GND	-			
H6	NC	-			NC	-			
J6	NC	-			NC	-			
H3	NC	-			NC	-			
H2	NC	-			NC	-			
H17	NC	-			NC	-			

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
Y10	VCC	-		
Y11	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
Y20	VCC	-		
J13	VCCIO0	0		
J14	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
K14	VCCIO0	0		
K15	VCCIO0	0		
J17	VCCIO1	1		
J18	VCCIO1	1		
J20	VCCIO1	1		
K17	VCCIO1	1		
K18	VCCIO1	1		
K20	VCCIO1	1		
L21	VCCIO2	2		
M21	VCCIO2	2		
M22	VCCIO2	2		
N21	VCCIO2	2		
N22	VCCIO2	2		
R21	VCCIO2	2		
U21	VCCIO3	3		
U22	VCCIO3	3		
V21	VCCIO3	3		
V22	VCCIO3	3		
W21	VCCIO3	3		
Y22	VCCIO3	3		
AA16	VCCIO4	4		
AA17	VCCIO4	4		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AB17	VCCIO4	4		
AB18	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AA14	VCCIO5	5		
AB12	VCCIO5	5		
AB13	VCCIO5	5		
AB14	VCCIO5	5		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F14	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C(LVDS)*	
F13	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
GNDIO	GNDIO2	-			GNDIO2	-			
H11	PR14B	2		C	PR14B	2	RDQ15	C	
G11	PR14A	2		T	PR14A	2	RDQ15	T	
E13	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C(LVDS)*	
F12	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C(LVDS)*	
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
GNDIO	GNDIO2	-			GNDIO2	-			
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
F4	XRES	-			XRES	-			
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12			
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T	
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T	
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T	
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12			
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T	
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C	
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T	
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T	
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AB6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T	
AB7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA8	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AB8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C	
AA9	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T	
Y9	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C	
AB9	PB24A	4	BDQS24****	T	PB42A	4	BDQS42****	T	
GNDIO	GNDIO4	-			GNDIO4	-			
AB10	PB24B	4	BDQ24	C	PB42B	4	BDQ42	C	
AA10	PB25A	4	BDQ24	T	PB43A	4	BDQ42	T	
Y11	PB25B	4	BDQ24	C	PB43B	4	BDQ42	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
V10	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T	
U11	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C	
V11	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T	
W11	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C	
AA11	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T	
AB11	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T11	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T	
U12	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA12	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T	
Y12	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C	
V12	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T	
W12	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C	
AB12	PB35A	4	BDQ33	T	PB53A	4	BDQ51	T	
AA13	PB35B	4	BDQ33	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T12	PB36A	4	BDQ33	T	PB54A	4	BDQ51	T	
U13	PB36B	4	BDQ33	C	PB54B	4	BDQ51	C	
V13	PB37A	4	BDQ33	T	PB55A	4	BDQ51	T	
T13	PB37B	4	BDQ33	C	PB55B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AB13	PB38A	4	BDQ42	T	PB56A	4	BDQ60	T	
AB14	PB38B	4	BDQ42	C	PB56B	4	BDQ60	C	
U14	PB39A	4	BDQ42	T	PB57A	4	BDQ60	T	
T14	PB39B	4	BDQ42	C	PB57B	4	BDQ60	C	
AA14	PB40A	4	BDQ42	T	PB58A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	BDQ42	C	PB58B	4	BDQ60	C	
W14	PB41A	4	BDQ42	T	PB59A	4	BDQ60	T	
V14	PB41B	4	BDQ42	C	PB59B	4	BDQ60	C	
AB15	PB42A	4	BDQS42	T	PB60A	4	BDQS60	T	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
GNDIO	GNDIO2	-			GNDIO2	-			
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			-	-			
F16	XRES	-			XRES	-			
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12			
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T	
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A18	URC_SQ_HDOUTP ₀	12		T	URC_SQ_HDOUTP ₀	12		T	
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B18	URC_SQ_HDOUTN ₀	12		C	URC_SQ_HDOUTN ₀	12		C	
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B17	URC_SQ_HDOUTN ₁	12		C	URC_SQ_HDOUTN ₁	12		C	
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A17	URC_SQ_HDOUTP ₁	12		T	URC_SQ_HDOUTP ₁	12		T	
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12			
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T	
B16	URC_SQ_VCCAUX ₃₃	12			URC_SQ_VCCAUX ₃₃	12			
E17	URC_SQ_REFCLK _N	12		C	URC_SQ_REFCLK _N	12		C	
D17	URC_SQ_REFCLK _P	12		T	URC_SQ_REFCLK _P	12		T	
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T	
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A15	URC_SQ_HDOUTP ₂	12		T	URC_SQ_HDOUTP ₂	12		T	
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B15	URC_SQ_HDOUTN ₂	12		C	URC_SQ_HDOUTN ₂	12		C	
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B14	URC_SQ_HDOUTN ₃	12		C	URC_SQ_HDOUTN ₃	12		C	
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A14	URC_SQ_HDOUTP ₃	12		T	URC_SQ_HDOUTP ₃	12		T	
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K3	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
N10	VCCIO7	7			VCCIO7	7			
N3	VCCIO7	7			VCCIO7	7			
P10	VCCIO7	7			VCCIO7	7			
R6	VCCIO7	7			VCCIO7	7			
AA25	VCCIO8	8			VCCIO8	8			
AD28	VCCIO8	8			VCCIO8	8			
AA10	VCCAUX	-			VCCAUX	-			
AA11	VCCAUX	-			VCCAUX	-			
AA20	VCCAUX	-			VCCAUX	-			
AA21	VCCAUX	-			VCCAUX	-			
K10	VCCAUX	-			VCCAUX	-			
K11	VCCAUX	-			VCCAUX	-			
K20	VCCAUX	-			VCCAUX	-			
K21	VCCAUX	-			VCCAUX	-			
L10	VCCAUX	-			VCCAUX	-			
L11	VCCAUX	-			VCCAUX	-			
L20	VCCAUX	-			VCCAUX	-			
L21	VCCAUX	-			VCCAUX	-			
Y10	VCCAUX	-			VCCAUX	-			
Y11	VCCAUX	-			VCCAUX	-			
Y20	VCCAUX	-			VCCAUX	-			
Y21	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A13	GND	-			GND	-			
A18	GND	-			GND	-			
A24	GND	-			GND	-			
A30	GND	-			GND	-			
A7	GND	-			GND	-			
AA14	GND	-			GND	-			
AA15	GND	-			GND	-			
AA16	GND	-			GND	-			
AA17	GND	-			GND	-			
AA24	GND	-			GND	-			
AA27	GND	-			GND	-			
AA4	GND	-			GND	-			
AB24	GND	-			GND	-			
AB7	GND	-			GND	-			
AD12	GND	-			GND	-			
AD19	GND	-			GND	-			
AD27	GND	-			GND	-			
AE22	GND	-			GND	-			
AE27	GND	-			GND	-			
AE4	GND	-			GND	-			
AE9	GND	-			GND	-			
AF14	GND	-			GND	-			

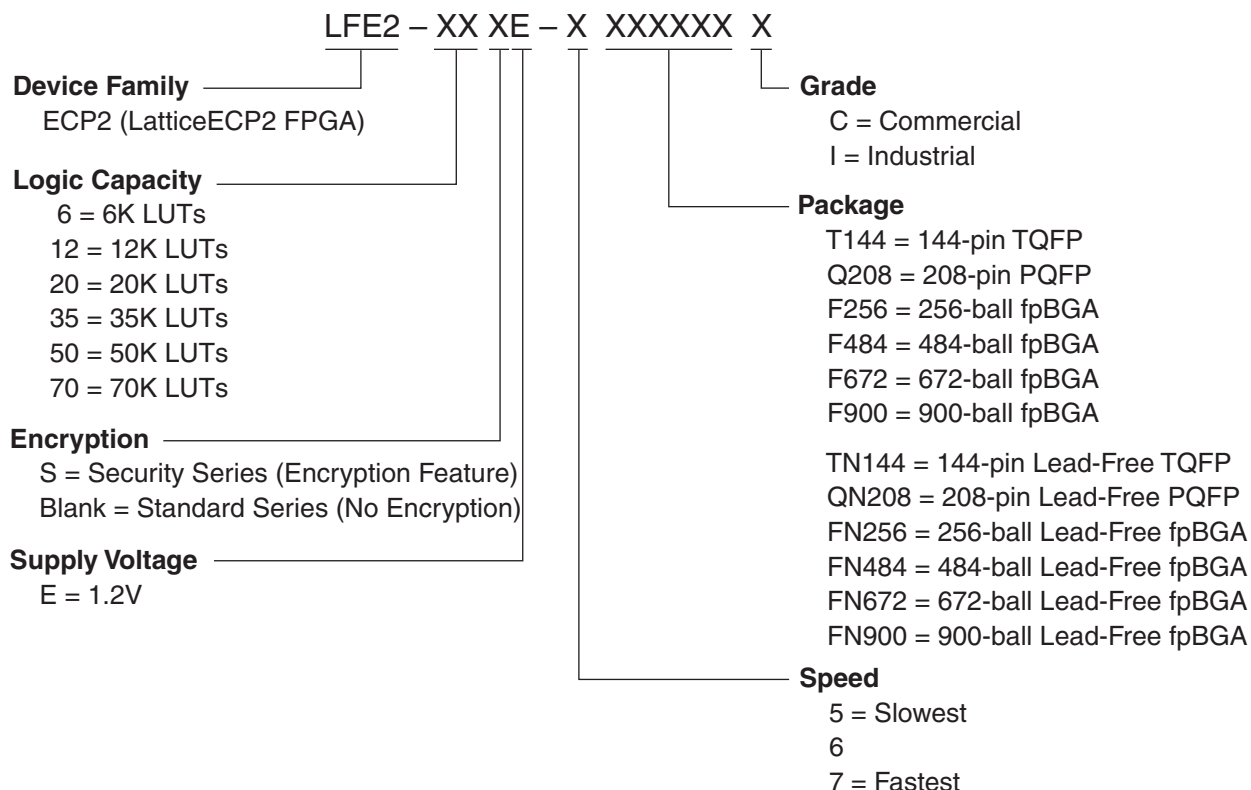
LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AN29	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AM28	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AL27	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AM29	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AL29	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AL30	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AK30	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AK29	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AM30	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AL31	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AM31	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AN30	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AP30	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T
AL32	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AP31	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AN31	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AP32	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AM34	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AP33	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AN32	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AM32	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AN34	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AM33	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AN33	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AH28	CFG2	8			CFG2	8		
AD24	CFG1	8			CFG1	8		
AJ29	CFG0	8			CFG0	8		
AF25	PROGRAMN	8			PROGRAMN	8		
AJ28	CCLK	8			CCLK	8		
AE25	INITN	8			INITN	8		
AK31	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE24	WRITEN***	8			WRITEN***	8		
AJ30	CS1N***	8			CS1N***	8		
AD25	CSN***	8			CSN***	8		
AG29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG28	D1***	8			D1***	8		
AG30	D2***	8			D2***	8		
AH29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF26	D4***	8			D4***	8		
AH30	D5***	8			D5***	8		
AE26	D6***	8			D6***	8		
AJ31	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG27	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AK32	DOUT/CSN/ CSSPI1N***	8			DOUT/CSN/ CSSPI1N***	8		
AK33	BUSY/SISPI***	8			BUSY/SISPI***	8		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

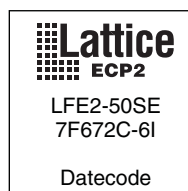
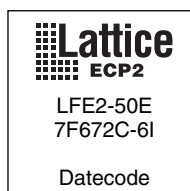
LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB16	GND	-			GND	-		
AB17	GND	-			GND	-		
AB18	GND	-			GND	-		
AB19	GND	-			GND	-		
AB26	GND	-			GND	-		
AB31	GND	-			GND	-		
AB4	GND	-			GND	-		
AB9	GND	-			GND	-		
AC16	GND	-			GND	-		
AC17	GND	-			GND	-		
AC18	GND	-			GND	-		
AC19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE27	GND	-			GND	-		
AE31	GND	-			GND	-		
AE4	GND	-			GND	-		
AE8	GND	-			GND	-		
AF12	GND	-			GND	-		
AF16	GND	-			GND	-		
AF19	GND	-			GND	-		
AF23	GND	-			GND	-		
AG31	GND	-			GND	-		
AH31	GND	-			GND	-		
AH4	GND	-			GND	-		
AJ14	GND	-			GND	-		
AJ21	GND	-			GND	-		
AK27	GND	-			GND	-		
AK8	GND	-			GND	-		
AL10	GND	-			GND	-		
AL16	GND	-			GND	-		
AL19	GND	-			GND	-		
AL2	GND	-			GND	-		
AL25	GND	-			GND	-		
AL33	GND	-			GND	-		
AP1	GND	-			GND	-		
AP10	GND	-			GND	-		
AP13	GND	-			GND	-		
AP22	GND	-			GND	-		
AP25	GND	-			GND	-		
AP34	GND	-			GND	-		
D10	GND	-			GND	-		
D16	GND	-			GND	-		
D19	GND	-			GND	-		
D2	GND	-			GND	-		
D25	GND	-			GND	-		
D33	GND	-			GND	-		
E27	GND	-			GND	-		
E8	GND	-			GND	-		
F14	GND	-			GND	-		

LatticeECP2 Part Number Description



Ordering Information

Note: LatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Date	Version	Section	Change Summary
August 2007 (cont.)	02.8 (cont.)	DC and Switching (cont.)	sysCLOCK GPLL timing has been updated.
		Pinout Information	Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information.
		Ordering Information	1156-fpBGA package option has been removed from the LatticeECP2M family.
September 2007	02.9	Pinout Information	Added Thermal Management text section.
February 2008	03.0	Architecture	Added LVC MOS33D description.
		DC and Switching	LatticeECP2M Supply Current has been updated.
			Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11).
			Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated.
			Table 3-8. Channel output Jitter (Max) has been updated.
		Pinout Information	Signal description has been updated.
April 2008	03.1	Pinout Information	Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100.
June 2008	03.2	Pinout Information	Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated.
		Introduction	Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
August 2008	03.3	DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
		Pinout Information	Added information for [LOC]DQ[num] to Signal Descriptions table.
January 2009	03.4	DC and Switching Characteristics	Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode.
			Added Channel Output Jitter table for x20 mode.
November 2009	03.5	DC and Switching Characteristics	Updated SPI/SPI _m Configuration Waveforms diagram.
			Updated footnotes in LatticeECP2 Initialization Supply Current table.
			Updated footnotes in LatticeECP2M Initialization Supply Current table.
			Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table.
			Updated max. value for t _{DINIT} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.
			Updated Serial Output Timing and Levels table.
			Updated Figure 3-5 MLVDS
			Updated Table 3-7 Serial Output Timing and Levels
			Updated Table 3-15 Power Down/Power Up Specification
		Pinout Information	Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5.