Lattice Semiconductor Corporation - LFE2-12E-5TN144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

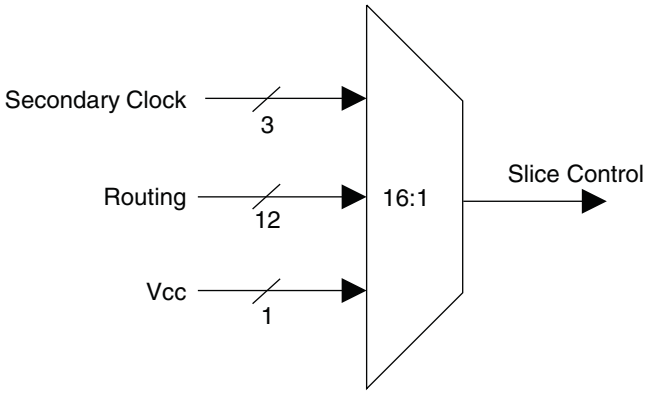
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-5tn144c

Figure 2-18. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeECP2/M devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per device: two edge clocks per edge. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKO signal (generated from the DLLDELA block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-19 shows the selection muxes for these clocks.

Figure 2-19. Edge Clock Mux Connections

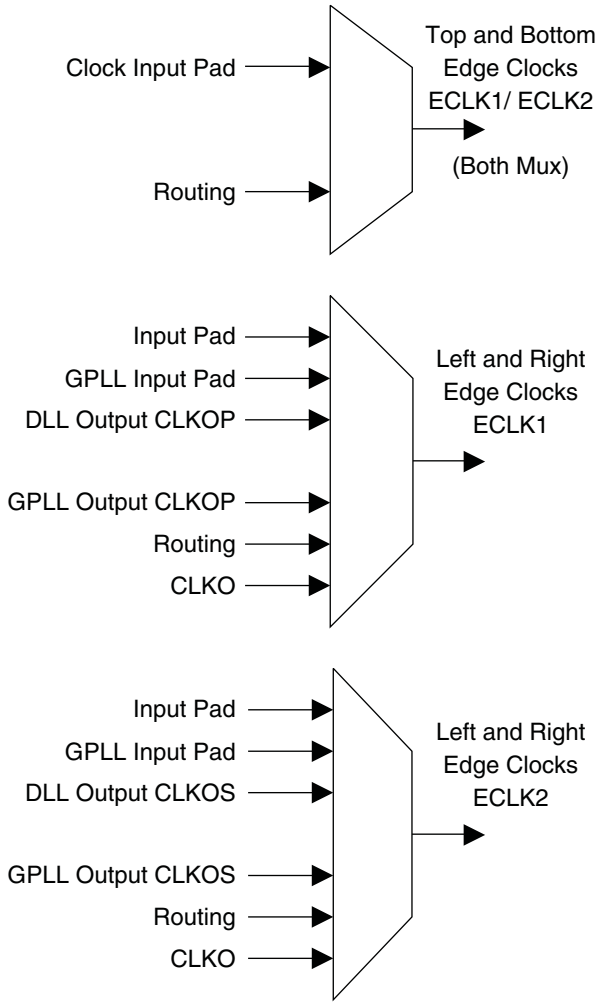
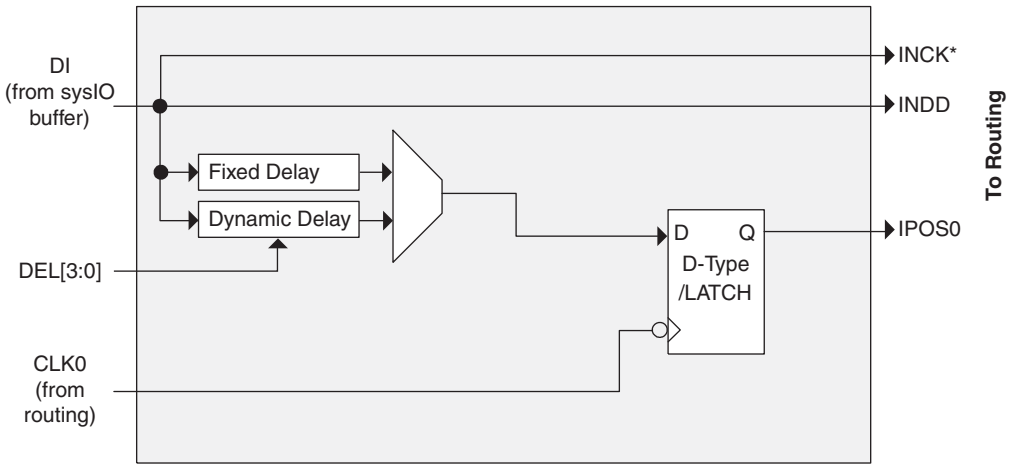


Figure 2-30. Input Register Block Top Edge



Note: Simplified version does not show CE and SET/RESET details.
*On selected blocks.

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the PIOs on the left, right and bottom contain a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-31 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-32 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining the output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams: ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-32 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

MLVDS

The LatticeECP2/M devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Multipoint Low Voltage Differential Signaling)

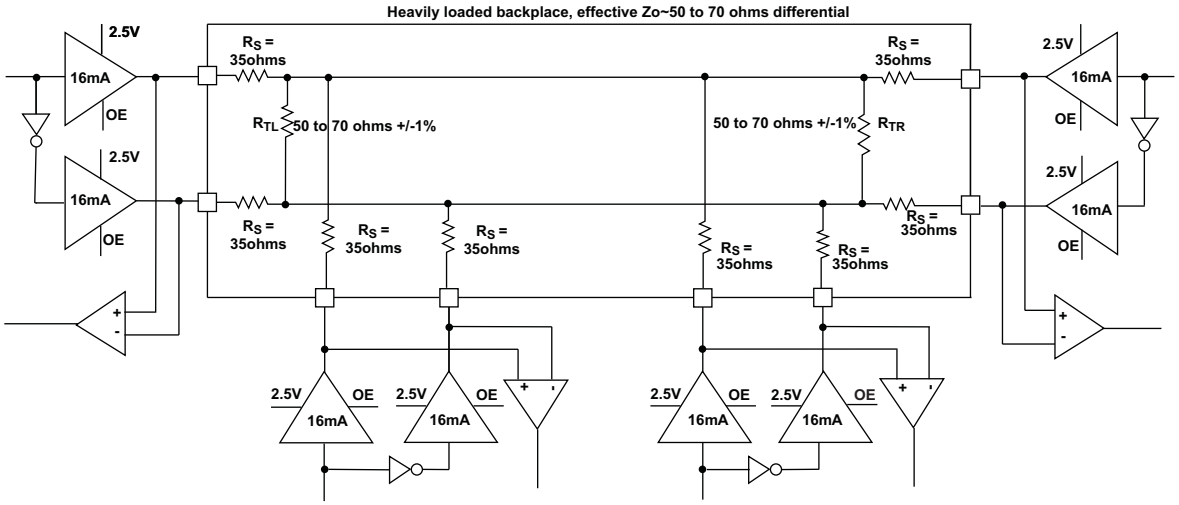


Table 3-6. MLVDS DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUE}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	LFE2-6	0.90	—	1.10	—	1.30	—	ns
		LFE2-12	0.90	—	1.10	—	1.30	—	ns
		LFE2-20	0.90	—	1.10	—	1.30	—	ns
		LFE2-35	0.90	—	1.10	—	1.30	—	ns
		LFE2-50	0.90	—	1.10	—	1.30	—	ns
		LFE2-70	0.90	—	1.10	—	1.30	—	ns
		LFE2M20	0.90	—	1.10	—	1.30	—	ns
		LFE2M35	0.90	—	1.10	—	1.30	—	ns
		LFE2M50	1.20	—	1.40	—	1.60	—	ns
		LFE2M70	1.20	—	1.40	—	1.60	—	ns
		LFE2M100	1.20	—	1.40	—	1.60	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.00	—	1.30	—	1.60	—	ns
		LFE2-12	1.00	—	1.30	—	1.60	—	ns
		LFE2-20	1.00	—	1.30	—	1.60	—	ns
		LFE2-35	1.00	—	1.30	—	1.60	—	ns
		LFE2-50	1.00	—	1.30	—	1.60	—	ns
		LFE2-70	1.00	—	1.30	—	1.60	—	ns
		LFE2M20	1.20	—	1.60	—	1.90	—	ns
		LFE2M35	1.20	—	1.60	—	1.90	—	ns
		LFE2M50	1.20	—	1.60	—	1.90	—	ns
		LFE2M70	1.20	—	1.60	—	1.90	—	ns
		LFE2M100	1.20	—	1.60	—	1.90	—	ns

LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTL33_4mA	LVTTL 4mA drive	0.52	0.60	0.68	ns
LVTTL33_8mA	LVTTL 8mA drive	0.06	0.08	0.09	ns
LVTTL33_12mA	LVTTL 12mA drive	0.04	0.04	0.05	ns
LVTTL33_16mA	LVTTL 16mA drive	0.03	0.02	0.02	ns
LVTTL33_20mA	LVTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

Table 3-13. Periodic Receiver Jitter Tolerance Specification[1]

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	3.125 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
	1.25 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	250 Mbps[2]	600 mV differential eye	—	—	0.08	UI, p-p

1. Values are measured with PRBS 2^7-1, all channels operating.
2. Jitter specification is limited by measurement equipment capability.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO6	-			GNDIO6	-		
L2	PL24A	6	LDQ28	T (LVDS)*	PL24A	6	LDQ28	T (LVDS)*
K2	PL25A	6	LDQ28	T	PL25A	6	LDQ28	T
L3	PL24B	6	LDQ28	C (LVDS)*	PL24B	6	LDQ28	C (LVDS)*
K1	PL25B	6	LDQ28	C	PL25B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
L4	PL26A	6	LDQ28	T (LVDS)*	PL26A	6	LDQ28	T (LVDS)*
L1	PL27A	6	LDQ28	T	PL27A	6	LDQ28	T
L5	PL26B	6	LDQ28	C (LVDS)*	PL26B	6	LDQ28	C (LVDS)*
M1	PL27B	6	LDQ28	C	PL27B	6	LDQ28	C
GND	GNDIO6	-			GNDIO6	-		
N1	PL29A	6	LDQ28	T	PL29A	6	LDQ28	T
N2	PL28A	6	LDQS28	T (LVDS)*	PL28A	6	LDQS28	T (LVDS)*
P1	PL29B	6	LDQ28	C	PL29B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL28B	6	LDQ28	C (LVDS)*	PL28B	6	LDQ28	C (LVDS)*
R1	PL30A	6	LDQ28	T (LVDS)*	PL30A	6	LDQ28	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
R2	PL30B	6	LDQ28	C (LVDS)*	PL30B	6	LDQ28	C (LVDS)*
N4	TDI	-			TDI	-		
M4	TCK	-			TCK	-		
P3	TDO	-			TDO	-		
N3	TMS	-			TMS	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
K6	NC	-			PB3A	5	BDQ6	
M6	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
R3	NC	-			PB5A	5	BDQ6	T
P4	NC	-			PB5B	5	BDQ6	C
-	-	-			VCCIO	5		
-	-	-			GNDIO5	5		
N5	PB3A	5	BDQ6	T	PB21A	5	BDQ24	T
N6	PB3B	5	BDQ6	C	PB21B	5	BDQ24	C
T2	PB4A	5	BDQ6	T	PB22A	5	BDQ24	T
P6	PB5A	5	BDQ6	T	PB23A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB4B	5	BDQ6	C	PB22B	5	BDQ24	C
R6	PB5B	5	BDQ6	C	PB23B	5	BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
R4	PB6A	5	BDQS6	T	PB24A	5	BDQS24	T
L6	PB7A	5	BDQ6	T	PB25A	5	BDQ24	T
T4	PB6B	5	BDQ6	C	PB24B	5	BDQ24	C
L7	PB7B	5	BDQ6	C	PB25B	5	BDQ24	C
N7	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
GND	GND	GNDIO5	-		
R4	R4	PB33A	5	BDQS33	T
L6	L6	PB34A	5	BDQ33	T
T4	T4	PB33B	5	BDQ33	C
L7	L7	PB34B	5	BDQ33	C
N7	N7	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
M8	M8	PB35B	5	PCLKC5_0/BDQ33	C
GND	GND	GNDIO5	-		
P7	P7	PB40A	4	PCLKT4_0/BDQ42	T
R8	R8	PB40B	4	PCLKC4_0/BDQ42	C
VCCIO	VCCIO	VCCIO4	4		
T5	T5	PB41A	4	BDQ42	T
T6	T6	PB41B	4	BDQ42	C
T8	T8	PB42A	4	BDQS42	T
GND	GND	GNDIO4	-		
R7	R7	PB43A	4	BDQ42	T
T9	T9	PB42B	4	BDQ42	C
T7	T7	PB43B	4	BDQ42	C
L8	L8	PB44A	4	BDQ42	T
VCCIO	VCCIO	VCCIO4	4		
P8	P8	PB45A	4	BDQ42	T
L9	L9	PB44B	4	BDQ42	C
N8	N8	PB45B	4	BDQ42	C
R9	R9	PB46A	4	BDQ42	T
GND	GND	GNDIO4	-		
R10	R10	PB46B	4	BDQ42	C
-	VCC	VCCIO	4		
-	GND	GNDIO4	4		
N9	N9	PB56A	4	BDQ60	T
T10	T10	PB57A	4	BDQ60	T
M9	M9	PB56B	4	BDQ60	C
R11	R11	PB57B	4	BDQ60	C
P10	P10	PB58A	4	BDQ60	T
N11	N11	PB59A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
N10	N10	PB58B	4	BDQ60	C
P11	P11	PB59B	4	BDQ60	C
T11	T11	PB60A	4	BDQS60	T
GND	GND	GNDIO4	-		
M11	M11	PB61A	4	BDQ60	T
T12	T12	PB60B	4	BDQ60	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		
V20	PROGRAMN	8			PROGRAMN	8		
W20	CFG0	8			CFG0	8		
U22	PR28B	8	D1	C	PR42B	8	D1	C
V22	INITN	8			INITN	8		
R16	PR30B	8	WRITEN	C	PR44B	8	WRITEN	C
GNDIO	GNDIO8	-			GNDIO8	-		
W22	CCLK	8			CCLK	8		
R17	PR30A	8	CS1N	T	PR44A	8	CS1N	T
V21	DONE	8			DONE	8		
VCCIO	VCCIO8	8			VCCIO8	8		
U19	PR29B	8	CSN	C	PR43B	8	CSN	C
T17	PR26B	8	D5	C	PR40B	8	D5	C
U20	PR29A	8	D0/SPIFASTN	T	PR43A	8	D0/SPIFASTN	T
U21	PR28A	8	D2	T	PR42A	8	D2	T
GNDIO	GNDIO8	-			GNDIO8	-		
T18	PR26A	8	D6	T	PR40A	8	D6	T
T20	PR27B	8	D3	C	PR41B	8	D3	C
T21	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
T19	PR27A	8	D4	T	PR41A	8	D4	T
VCCIO	VCCIO8	8			VCCIO8	8		
T22	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
R18	PR24B	8	DOUT/CSON	C	PR38B	8	DOUT/CSON	C
R19	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
-	-	-			VCCIO3	3		
GNDIO	GNDIO3	-			GNDIO3	-		
P18	PR22B	3		C (LVDS)*	PR32B	3	RDQ34	C (LVDS)*
R22	PR23B	3		C	PR33B	3	RDQ34	C
P19	PR22A	3		T (LVDS)*	PR32A	3	RDQ34	T (LVDS)*
R21	PR23A	3		T	PR33A	3	RDQ34	T
VCCIO	VCCIO3	3			VCCIO3	3		
R20	PR21B	3	RLM0_GPLLC_FB_A	C	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
P21	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR18B	3	RLM0_GDLLC_FB_A	C	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
M22	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
N19	NC	-			PR26B	3	RDQ25	C
-	-	-			VCCIO3	3		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
C5	VCCAUX	-			VCCAUX	-		
D11	VCCAUX	-			VCCAUX	-		
E17	VCCAUX	-			VCCAUX	-		
E6	VCCAUX	-			VCCAUX	-		
F13	VCCAUX	-			VCCAUX	-		
G18	VCCAUX	-			VCCAUX	-		
G5	VCCAUX	-			VCCAUX	-		
K5	VCCAUX	-			VCCAUX	-		
M17	VCCAUX	-			VCCAUX	-		
P17	VCCAUX	-			VCCAUX	-		
R5	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V13	VCCAUX	-			VCCAUX	-		
V15	VCCAUX	-			VCCAUX	-		
V7	VCCAUX	-			VCCAUX	-		
V8	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W20	CFG0	8			CFG0	8		
V20	PROGRAMN	8			PROGRAMN	8		
W22	CCLK	8			CCLK	8		
V22	INITN	8			INITN	8		
V21	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
R16	PR58B	8	WRITEN	C	PR77B	8	WRITEN	C
R17	PR58A	8	CS1N	T	PR77A	8	CS1N	T
U19	PR57B	8	CSN	C	PR76B	8	CSN	C
U20	PR57A	8	D0/SPIFASTN	T	PR76A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO	8		
U22	PR56B	8	D1	C	PR75B	8	D1	C
U21	PR56A	8	D2	T	PR75A	8	D2	T
T20	PR55B	8	D3	C	PR74B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
T19	PR55A	8	D4	T	PR74A	8	D4	T
T17	PR54B	8	D5	C	PR73B	8	D5	C
T18	PR54A	8	D6	T	PR73A	8	D6	T
T21	PR53B	8	D7/SPID0	C	PR72B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO	8		
T22	PR53A	8	DI/CSSPI0N	T	PR72A	8	DI/CSSPI0N	T
R18	PR52B	8	DOUT/CSON	C	PR71B	8	DOUT/CSON	C
R19	PR52A	8	BUSY/SISPI	T	PR71A	8	BUSY/SISPI	T
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO	3		
R22	PR47B	3	RDQ48	C	PR66B	3	RDQ67	C
R21	PR47A	3	RDQ48	T	PR66A	3	RDQ67	T
P18	PR46B	3	RDQ48	C (LVDS)*	PR65B	3	RDQ67	C (LVDS)*
P19	PR46A	3	RDQ48	T (LVDS)*	PR65A	3	RDQ67	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
R20	PR45B	3	RLM0_GPLLC_FB_A/RDQ48	C	PR64B	3	RLM0_GPLLC_FB_A/RDQ67	C
P22	PR45A	3	RLM0_GPLLT_FB_A/RDQ48	T	PR64A	3	RLM0_GPLLT_FB_A/RDQ67	T
P21	PR44B	3	RLM0_GPLLC_IN_A**/RDQ48	C (LVDS)*	PR63B	3	RLM0_GPLLC_IN_A**/RDQ67	C (LVDS)*
N21	PR44A	3	RLM0_GPLLT_IN_A**/RDQ48	T (LVDS)*	PR63A	3	RLM0_GPLLT_IN_A**/RDQ67	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR42B	3	RLM0_GDLLC_FB_A/RDQ39	C	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C
N20	PR42A	3	RLM0_GDLLT_FB_A/RDQ39	T	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T
GNDIO	GNDIO3	-			GNDIO3	-		
M22	PR41B	3	RLM0_GDLLC_IN_A**/RDQ39	C (LVDS)*	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*
M21	PR41A	3	RLM0_GDLLT_IN_A**/RDQ39	T (LVDS)*	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*
N19	PR40B	3	RDQ39	C	PR59B	3	RDQ58	C
M19	PR40A	3	RDQ39	T	PR59A	3	RDQ58	T
VCCIO	VCCIO3	3			VCCIO	3		
GNDIO	GNDIO3	-			GNDIO3	-		
L22	PR30B	3	RDQ31	C	PR49B	3	RDQ50	C
K22	PR30A	3	RDQ31	T	PR49A	3	RDQ50	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
F6	PL5A	7	LDQ8	T	PL18A	7	LDQ21	T
F5	PL5B	7	LDQ8	C	PL18B	7	LDQ21	C
VCCIO	VCCIO7	7			VCCIO7	7		
E4	PL6A	7	LDQ8	T (LVDS)*	PL19A	7	LDQ21	T (LVDS)*
E3	PL6B	7	LDQ8	C (LVDS)*	PL19B	7	LDQ21	C (LVDS)*
E2	PL7A	7	LDQ8	T	PL20A	7	LDQ21	T
E1	PL7B	7	LDQ8	C	PL20B	7	LDQ21	C
GND	GNDIO7	-			GNDIO7	-		
H6	PL8A	7	LDQS8	T (LVDS)*	PL21A	7	LDQS21	T (LVDS)*
H5	PL8B	7	LDQ8	C (LVDS)*	PL21B	7	LDQ21	C (LVDS)*
F2	PL9A	7	LDQ8	T	PL22A	7	LDQ21	T
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL9B	7	LDQ8	C	PL22B	7	LDQ21	C
H8	PL10A	7	LDQ8	T (LVDS)*	PL23A	7	LDQ21	T (LVDS)*
J9	PL10B	7	LDQ8	C (LVDS)*	PL23B	7	LDQ21	C (LVDS)*
G4	PL11A	7	LDQ8	T	PL24A	7	LDQ21	T
GND	GNDIO7	-			GNDIO7	-		
G3	PL11B	7	LDQ8	C	PL24B	7	LDQ21	C
H7	PL12A	7	LDQ16	T (LVDS)*	PL25A	7	LDQ29	T (LVDS)*
J8	PL12B	7	LDQ16	C (LVDS)*	PL25B	7	LDQ29	C (LVDS)*
G2	PL13A	7	LDQ16	T	PL26A	7	LDQ29	T
G1	PL13B	7	LDQ16	C	PL26B	7	LDQ29	C
H3	PL14A	7	LDQ16	T (LVDS)*	PL27A	7	LDQ29	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
H4	PL14B	7	LDQ16	C (LVDS)*	PL27B	7	LDQ29	C (LVDS)*
J5	PL15A	7	LDQ16	T	PL28A	7	LDQ29	T
J4	PL15B	7	LDQ16	C	PL28B	7	LDQ29	C
J3	PL16A	7	LDQS16	T (LVDS)*	PL29A	7	LDQS29	T (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
K4	PL16B	7	LDQ16	C (LVDS)*	PL29B	7	LDQ29	C (LVDS)*
H1	PL17A	7	LDQ16	T	PL30A	7	LDQ29	T
H2	PL17B	7	LDQ16	C	PL30B	7	LDQ29	C
VCCIO	VCCIO7	7			VCCIO7	7		
K6	PL18A	7	LDQ16	T (LVDS)*	PL31A	7	LDQ29	T (LVDS)*
K7	PL18B	7	LDQ16	C (LVDS)*	PL31B	7	LDQ29	C (LVDS)*
J1	PL19A	7	LDQ16	T	PL32A	7	LDQ29	T
J2	PL19B	7	LDQ16	C	PL32B	7	LDQ29	C
GND	GNDIO7	-			GNDIO7	-		
VCCIO	VCCIO7	7			VCCIO7	7		
K3	PL23A	7	LDQ24	T	PL36A	7	LDQ37	T
K2	PL23B	7	LDQ24	C	PL36B	7	LDQ37	C
GND	GNDIO7	-			GNDIO7	-		
K1	PL24A	7	LDQS24***	T (LVDS)*	PL37A	7	LDQS37***	T (LVDS)*

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F14	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C(LVDS)*
F13	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
GNDIO	GNDIO2	-			GNDIO2	-		
H11	PR14B	2		C	PR14B	2	RDQ15	C
G11	PR14A	2		T	PR14A	2	RDQ15	T
E13	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C(LVDS)*
F12	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C(LVDS)*
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			VCCIO2	2		
F4	XRES	-			XRES	-		
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G18	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K19	VCCIO2	2			VCCIO2	2		
N19	VCCIO3	3			VCCIO3	3		
P15	VCCIO3	3			VCCIO3	3		
T18	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		
AA18	VCCIO4	4			VCCIO4	4		
R14	VCCIO4	4			VCCIO4	4		
V16	VCCIO4	4			VCCIO4	4		
W13	VCCIO4	4			VCCIO4	4		
AA5	VCCIO5	5			VCCIO5	5		
R9	VCCIO5	5			VCCIO5	5		
V7	VCCIO5	5			VCCIO5	5		
W10	VCCIO5	5			VCCIO5	5		
N4	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
T5	VCCIO6	6			VCCIO6	6		
V2	VCCIO6	6			VCCIO6	6		
E2	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
J8	VCCIO7	7			VCCIO7	7		
K4	VCCIO7	7			VCCIO7	7		
AA22	VCCIO8	8			VCCIO8	8		
U19	VCCIO8	8			VCCIO8	8		
H11	VCCAUX	-			VCCAUX	-		
H12	VCCAUX	-			VCCAUX	-		
L15	VCCAUX	-			VCCAUX	-		
L8	VCCAUX	-			VCCAUX	-		
M15	VCCAUX	-			VCCAUX	-		
M8	VCCAUX	-			VCCAUX	-		
R11	VCCAUX	-			VCCAUX	-		
R12	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A16	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B13	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
D16	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
D7	GND	-			GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	NC	-			NC	-		
F14	NC	-			NC	-		
F13	NC	-			NC	-		
G12	NC	-			NC	-		
G13	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P16	GND	-			GND	-		
P17	GND	-			GND	-		
P18	GND	-			GND	-		
P20	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
R15	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R20	GND	-			GND	-		
R21	GND	-			GND	-		
R24	GND	-			GND	-		
R7	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T13	GND	-			GND	-		
T14	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T20	GND	-			GND	-		
T21	GND	-			GND	-		
T24	GND	-			GND	-		
T7	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U20	GND	-			GND	-		
V14	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V27	GND	-			GND	-		
V4	GND	-			GND	-		
W23	GND	-			GND	-		
W8	GND	-			GND	-		
Y14	GND	-			GND	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO1	-			GNDIO1	-		
F19	PT59B	1		C	PT68B	1		C
D18	PT59A	1		T	PT68A	1		T
L18	NC	-			PT67B	1		C
K19	NC	-			PT67A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A18	PT57B	1	VREF2_1	C	PT66B	1	VREF2_1	C
B18	PT57A	1	VREF1_1	T	PT66A	1	VREF1_1	T
G18	PT56B	1	PCLKC1_0	C	PT65B	1	PCLKC1_0	C
E18	PT56A	1	PCLKT1_0	T	PT65A	1	PCLKT1_0	T
F18	PT55B	0	PCLKC0_0	C	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G19	PT55A	0	PCLKT0_0	T	PT64A	0	PCLKT0_0	T
H18	PT54B	0	VREF2_0	C	PT63B	0	VREF2_0	C
K18	PT54A	0	VREF1_0	T	PT63A	0	VREF1_0	T
VCCIO	VCCIO0	0			VCCIO0	0		
J18	PT53B	0		C	PT60B	0		C
L17	PT53A	0		T	PT60A	0		T
G17	PT52B	0		C	PT59B	0		C
-	-	-			GNDIO0	-		
J17	PT52A	0		T	PT59A	0		T
H17	PT51B	0		C	PT58B	0		C
-	-	-			VCCIO0	0		
K17	PT51A	0		T	PT58A	0		T
B17	PT50B	0		C	PT57B	0		C
GNDIO	GNDIO0	-			-	-		
A17	PT50A	0		T	PT57A	0		T
D17	PT49B	0		C	PT56B	0		C
VCCIO	VCCIO0	0			-	-		
F17	PT49A	0		T	PT56A	0		T
B16	PT48B	0		C	PT55B	0		C
A16	PT48A	0		T	PT55A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
E17	PT47B	0		C	PT52B	0		C
C17	PT47A	0		T	PT52A	0		T
K16	PT46B	0		C	PT51B	0		C
J15	PT46A	0		T	PT51A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
G16	PT45B	0		C	PT50B	0		C
H15	PT45A	0		T	PT50A	0		T
A15	PT44B	0		C	PT49B	0		C
B15	PT44A	0		T	PT49A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
L16	PT43B	0		C	PT48B	0		C
K15	PT43A	0		T	PT48A	0		T
F16	PT42B	0		C	PT47B	0		C
E16	PT42A	0		T	PT47A	0		T
E15	PT41B	0		C	PT46B	0		C

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL}, I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT}.
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.