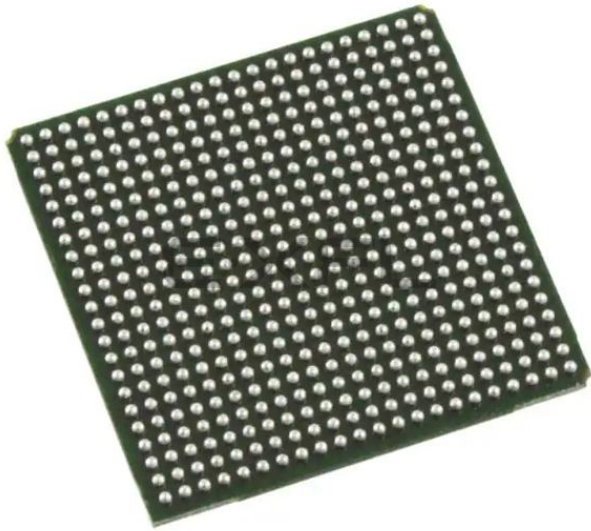




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

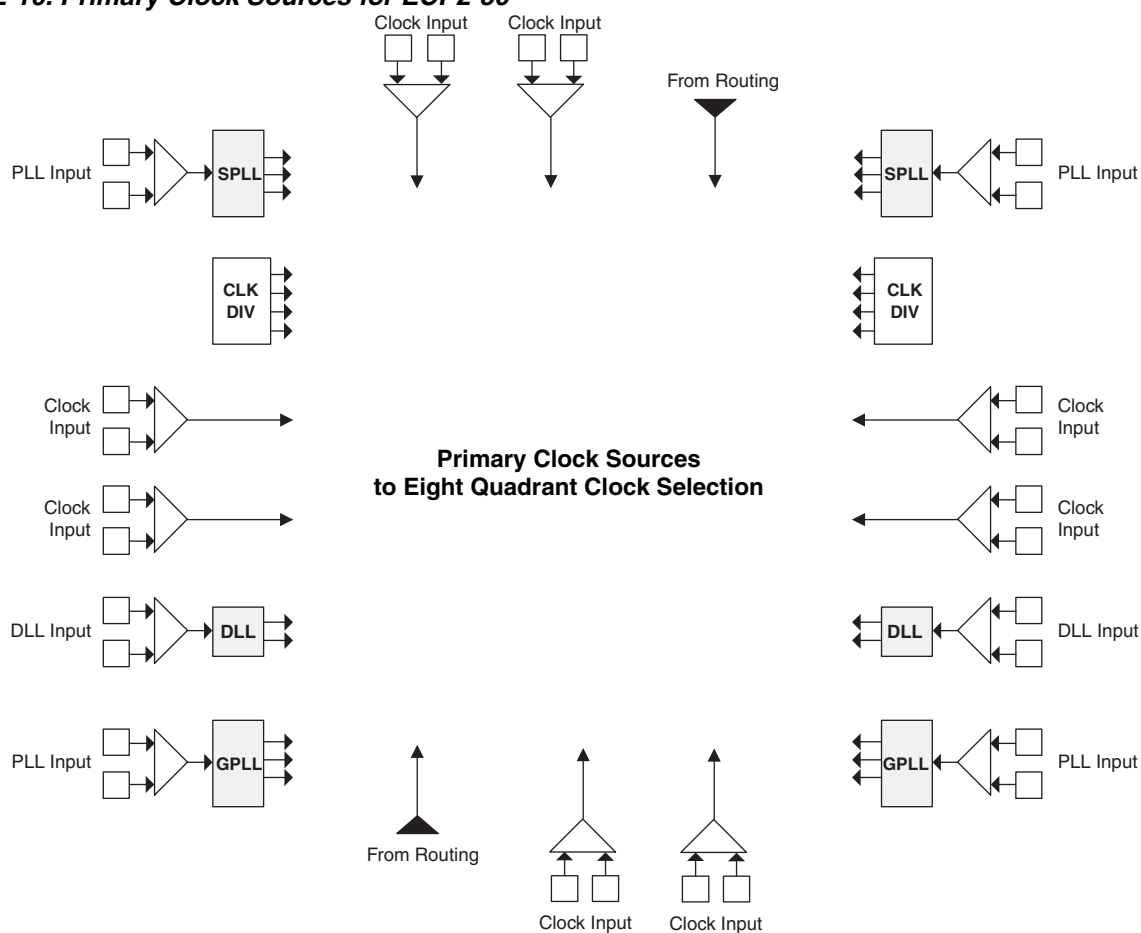
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	297
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12e-6fn484i

Figure 2-10. Primary Clock Sources for ECP2-50



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPPLLs. All LatticeECP2M devices have six SPPLLs.

sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

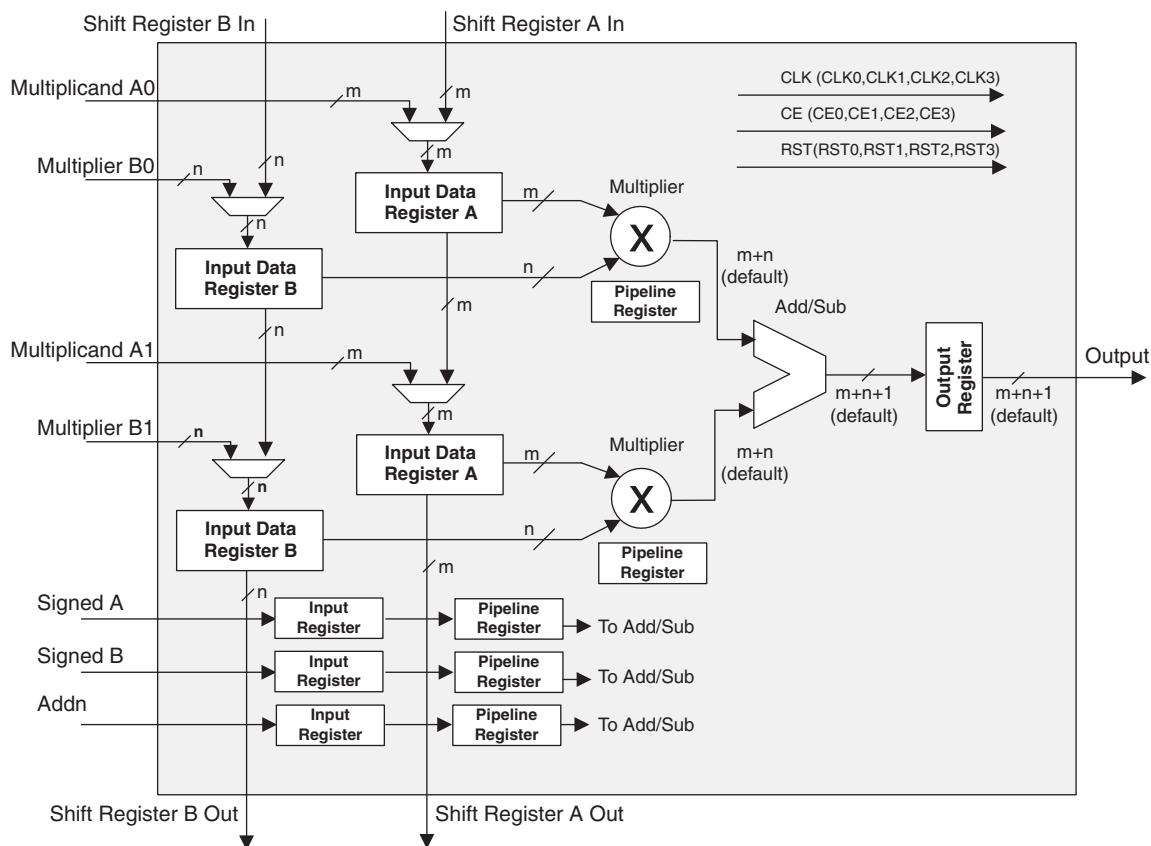
EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

Figure 2-25. MULTADDSUB



LatticeECP2/M External Switching Characteristics⁹

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL) ¹									
t _{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

SERDES High Speed Data Receiver (LatticeECP2M Family Only)

Table 3-11. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units
RX-CID _S	Stream of nontransitions ¹ (CID = Consecutive Identical Digits) @ 10 ⁻¹² BER		7 @ 3.125 Gbps 20 @ 1.25 Gbps		Bits
V _{RX-DIFF-S}	Differential input sensitivity	100	—	—	mV, p-p
V _{RX-IN}	Input levels	0	—	V _{CCR_X} + 0.8	V
V _{RX-CM-DC}	Input common mode range (DC coupled)	0.5	—	1.2	V
V _{RX-CM-AC}	Input common mode range (AC coupled) ³	0	—	1.5	V
T _{RX-RELOCK}	CDR re-lock time ²	—	—	3000	Bits
Z _{RX-TERM}	Input termination 50/75 Ohm/High Z	—	50		Ohms
RL _{RX-RL}	Return loss (without package)	—	9	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.
3. AC coupling is used to interface to LVPECL and LVDS.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-12. Receiver Total Jitter Tolerance Specification¹

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.54	UI, p-p
Random		600 mV differential eye	—	—	0.26	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.61	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.81	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.53	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	250 Mbps ²	600 mV differential eye	—	—	0.42	UI, p-p
Random		600 mV differential eye	—	—	0.10	UI, p-p
Total		600 mV differential eye	—	—	0.60	UI, p-p

1. Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.
2. Jitter specification is limited by measurement equipment capability.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*	
6	VCCAUX	-			VCCAUX	-			
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*	
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
9	VCCIO7	7			VCCIO7	7			
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
11	GND	-			GND	-			
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
16	VCC	-			VCC	-			
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
21	GND	-			GND	-			
22	VCC	-			VCC	-			
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
25	LLM0_PLCCAP	6			LLM0_PLCCAP	6			
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
28	PL22A	6			PL22A	6			
29	VCC	-			VCC	-			
30	GND	-			GND	-			
31	VCCIO6	6			VCCIO6	6			
32	TCK	-			TCK	-			
33	TDI	-			TDI	-			
34	TDO	-			TDO	-			
35	VCCJ	-			VCCJ	-			
36	TMS	-			TMS	-			
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
39	VCCAUX	-			VCCAUX	-			
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T	
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C	
42	VCCIO5	5			VCCIO5	5			
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T	
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C	
45	NC	5			PB16A	5	BDQ15	T	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
46	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
47	PL30A	6	LDQ28		PL44A	6	LDQ42		
48	TCK	-			TCK	-			
49	TDI	-			TDI	-			
50	TDO	-			TDO	-			
51	VCCJ	-			VCCJ	-			
52	TMS	-			TMS	-			
53	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
54	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
55	VCCIO5	5			VCCIO5	5			
56	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
57	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
58	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
59	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
60	GND	-			GND	-			
61	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
62	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
63	VCCIO5	5			VCCIO5	5			
64	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
65	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
66	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
67	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
68	GND	-			GND	-			
69	PB20A	5	BDQ24	T	PB30A	5	BDQ33	T	
70	VCCAUX	-			VCCAUX	-			
71	PB20B	5	BDQ24	C	PB30B	5	BDQ33	C	
72	PB22A	5	BDQ24	T	PB32A	5	BDQ33	T	
73	PB22B	5	BDQ24	C	PB32B	5	BDQ33	C	
74	VCC	-			VCC	-			
75	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T	
76	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C	
77	GND	-			GND	-			
78	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T	
79	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C	
80	VCC	-			VCC	-			
81	GND	-			GND	-			
82	PB34A	4	BDQ33	T	PB42A	4	BDQS42	T	
83	PB34B	4	BDQ33	C	PB42B	4	BDQ42	C	
84	PB36A	4	BDQ33	T	PB44A	4	BDQ42	T	
85	PB36B	4	BDQ33	C	PB44B	4	BDQ42	C	
86	VCCAUX	-			VCCAUX	-			
87	PB40A	4	BDQ42	T	PB50A	4	BDQ51	T	
88	PB40B	4	BDQ42	C	PB50B	4	BDQ51	C	
89	GND	-			GND	-			
90	PB42A	4	BDQS42	T	PB52A	4	BDQ51	T	
91	PB42B	4	BDQ42	C	PB52B	4	BDQ51	C	

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A5	A5	PT36B	0		C
A3	A3	PT35B	0		C
A4	A4	PT36A	0		T
VCCIO	VCCIO	VCCIO0	0		
B3	B3	PT35A	0		T
A2	A2	PT34B	0		C
C7	C7	PT33B	0		C
B2	B2	PT34A	0		T
D7	D7	PT33A	0		T
D6	D6	PT32B	0		C
GND	GND	GNDIO0	-		
F7	F7	PT31B	0		C
C6	C6	PT32A	0		T
VCCIO	VCCIO	VCCIO0	0		
F6	F6	PT31A	0		T
C4	C4	PT30B	0		C
B4	B4	PT30A	0		T
-	GND	GNDIO0	0		
-	VCC	VCCIO	0		
D5	D5	PT2B	0	VREF2_0	C
E5	E5	PT2A	0	VREF1_0	T
G7	G7	VCC	-		
G9	G9	VCC	-		
H7	H7	VCC	-		
J10	J10	VCC	-		
K10	K10	VCC	-		
K8	K8	VCC	-		
G8	G8	VCCAUX	-		
H10	H10	VCCAUX	-		
J7	J7	VCCAUX	-		
K9	K9	VCCAUX	-		
C5	C5	VCCIO0	0		
E7	E7	VCCIO0	0		
C12	C12	VCCIO1	1		
E10	E10	VCCIO1	1		
E14	E14	VCCIO2	2		
G12	G12	VCCIO2	2		
K12	K12	VCCIO3	3		
M14	M14	VCCIO3	3		
M10	M10	VCCIO4	4		
P12	P12	VCCIO4	4		
M7	M7	VCCIO5	5		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
B15	PT40B	1		C	PT49B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
A15	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A14	PT39A	1		T	PT48A	1		T
B14	PT39B	1		C	PT48B	1		C
D14	PT37B	1		C	PT46B	1		C
E14	PT36B	1		C	PT45B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
C13	PT37A	1		T	PT46A	1		T
F14	PT36A	1		T	PT45A	1		T
A13	PT35B	1		C	PT44B	1		C
E13	PT34B	1		C	PT43B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B13	PT35A	1		T	PT44A	1		T
D13	PT34A	1		T	PT43A	1		T
E12	PT33B	1		C	PT42B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
D12	PT33A	1		T	PT42A	1		T
A12	PT31B	1		C	PT40B	1		C
B12	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C
VCCIO	VCCIO1	1			VCCIO1	1		
A11	PT31A	1		T	PT40A	1		T
C12	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T
F12	XRES	1			XRES	1		
B10	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
B11	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
C11	PT26B	0		C	PT35B	0		C
A10	PT27B	0		C	PT36B	0		C
C10	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
A9	PT27A	0		T	PT36A	0		T
A8	PT24B	0		C	PT33B	0		C
E11	PT25B	0		C	PT34B	0		C
A7	PT24A	0		T	PT33A	0		T
F11	PT25A	0		T	PT34A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
B8	PT23B	0		C	PT32B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B9	PT23A	0		T	PT32A	0		T
C8	PT20B	0		C	PT29B	0		C
B7	PT21B	0		C	PT30B	0		C
D8	PT20A	0		T	PT29A	0		T

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U9	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
W9	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
V9	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
Y8	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AA8	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W10	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
V10	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
AB8	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AA9	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB9	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AB10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
Y10	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AA10	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
U10	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
U11	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
AB11	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AA11	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y11	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
W11	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AB12	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AA12	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AB13	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T
AB14	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
GNDIO	GNDIO5	-			GNDIO5	-		
U12	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
V12	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C
Y12	PB41A	4	BDQ42	T	PB50A	4	BDQ51	T
W12	PB41B	4	BDQ42	C	PB50B	4	BDQ51	C
AA13	PB42A	4	BDQS42	T	PB51A	4	BDQS51	T
GNDIO	GNDIO4	-			GNDIO4	-		
Y13	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C
U13	PB43A	4	BDQ42	T	PB52A	4	BDQ51	T
U14	PB43B	4	BDQ42	C	PB52B	4	BDQ51	C
AB15	PB44A	4	BDQ42	T	PB53A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
AA14	PB44B	4	BDQ42	C	PB53B	4	BDQ51	C
AB16	PB45A	4	BDQ42	T	PB54A	4	BDQ51	T
AB17	PB45B	4	BDQ42	C	PB54B	4	BDQ51	C

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L2	NC	-			NC	-		
L1	NC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
M2	NC	-			NC	-		
M1	NC	-			NC	-		
N2	NC	-			NC	-		
GND	GNDIO7	-			GNDIO7	-		
M8	VCC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
GND	GNDIO7	-			GNDIO7	-		
N1	PL12A	7	LDQ16		PL18A	7	LDQ22	
L8	PL13A	7	LDQ16	T	PL19A	7	LDQ22	T
K8	PL13B	7	LDQ16	C	PL19B	7	LDQ22	C
VCCIO	VCCIO7	7			VCCIO7	7		
L6	PL14A	7	LDQ16	T (LVDS)*	PL20A	7	LDQ22	T (LVDS)*
K5	PL14B	7	LDQ16	C (LVDS)*	PL20B	7	LDQ22	C (LVDS)*
L7	PL15A	7	LDQ16	T	PL21A	7	LDQ22	T
L5	PL15B	7	LDQ16	C	PL21B	7	LDQ22	C
GND	GNDIO7	-			GNDIO7	-		
P1	PL16A	7	LDQS16	T (LVDS)*	PL22A	7	LDQS22	T (LVDS)*
P2	PL16B	7	LDQ16	C (LVDS)*	PL22B	7	LDQ22	C (LVDS)*
M6	PL17A	7	LDQ16	T	PL23A	7	LDQ22	T
VCCIO	VCCIO7	7			VCCIO7	7		
N8	PL17B	7	LDQ16	C	PL23B	7	LDQ22	C
R1	PL18A	7	LDQ16	T (LVDS)*	PL24A	7	LDQ22	T (LVDS)*
R2	PL18B	7	LDQ16	C (LVDS)*	PL24B	7	LDQ22	C (LVDS)*
M7	PL19A	7	PCLKT7_0/LDQ16	T	PL25A	7	PCLKT7_0/LDQ22	T
GND	GNDIO7	-			GNDIO7	-		
N9	PL19B	7	PCLKC7_0/LDQ16	C	PL25B	7	PCLKC7_0/LDQ22	C
M4	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	PL27A	6	PCLKT6_0/LDQ31	T (LVDS)*
M5	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*	PL27B	6	PCLKC6_0/LDQ31	C (LVDS)*
N7	PL22A	6	VREF2_6/LDQ25	T	PL28A	6	VREF2_6/LDQ31	T
P9	PL22B	6	VREF1_6/LDQ25	C	PL28B	6	VREF1_6/LDQ31	C
N3	PL23A	6	LDQ25	T (LVDS)*	PL29A	6	LDQ31	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
N4	PL23B	6	LDQ25	C (LVDS)*	PL29B	6	LDQ31	C (LVDS)*
N5	PL24A	6	LDQ25	T	PL30A	6	LDQ31	T
P7	PL24B	6	LDQ25	C	PL30B	6	LDQ31	C
T1	NC	-			PL31A	6	LDQS31	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
T2	NC	-			PL31B	6	LDQ31	C (LVDS)*
P8	NC	-			PL32A	6	LDQ31	T
P6	NC	-			PL32B	6	LDQ31	C
VCCIO	VCCIO6	6			VCCIO6	6		
P5	NC	-			PL33A	6	LDQ31	T (LVDS)*
P4	NC	-			PL33B	6	LDQ31	C (LVDS)*

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L2	PL24B	7	LDQ24	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
L1	PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T	PL38A	7	LUM0_SPLLT_IN_A/LDQ37	T	
VCCIO	VCCIO7	7			VCCIO7	7			
M2	PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C	
M1	PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T	PL39A	7	LUM0_SPLLT_FB_A/LDQ37	T	
N2	PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
M8	VCCPLL	7			NC	-			
VCCIO	VCCIO7	7			VCCIO7	7			
GND	GNDIO7	-			GNDIO7	-			
N1	PL37A	7	LDQ41		PL50A	7	LDQ54		
L8	PL38A	7	LDQ41	T	PL51A	7	LDQ54	T	
K8	PL38B	7	LDQ41	C	PL51B	7	LDQ54	C	
VCCIO	VCCIO7	7			VCCIO7	7			
L6	PL39A	7	LDQ41	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*	
K5	PL39B	7	LDQ41	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*	
L7	PL40A	7	LDQ41	T	PL53A	7	LDQ54	T	
L5	PL40B	7	LDQ41	C	PL53B	7	LDQ54	C	
GND	GNDIO7	-			GNDIO7	-			
P1	PL41A	7	LDQS41	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*	
P2	PL41B	7	LDQ41	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*	
M6	PL42A	7	LDQ41	T	PL55A	7	LDQ54	T	
VCCIO	VCCIO7	7			VCCIO7	7			
N8	PL42B	7	LDQ41	C	PL55B	7	LDQ54	C	
R1	PL43A	7	LDQ41	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*	
R2	PL43B	7	LDQ41	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*	
M7	PL44A	7	PCLKT7_0/LDQ41	T	PL57A	7	PCLKT7_0/LDQ54	T	
GND	GNDIO7	-			GNDIO7	-			
N9	PL44B	7	PCLKC7_0/LDQ41	C	PL57B	7	PCLKC7_0/LDQ54	C	
M4	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*	
M5	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*	
N7	PL47A	6	VREF2_6/LDQ50	T	PL60A	6	VREF2_6/LDQ63	T	
P9	PL47B	6	VREF1_6/LDQ50	C	PL60B	6	VREF1_6/LDQ63	C	
N3	PL48A	6	LDQ50	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
N4	PL48B	6	LDQ50	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*	
N5	PL49A	6	LDQ50	T	PL62A	6	LDQ63	T	
P7	PL49B	6	LDQ50	C	PL62B	6	LDQ63	C	
T1	PL50A	6	LDQS50	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
T2	PL50B	6	LDQ50	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*	
P8	PL51A	6	LDQ50	T	PL64A	6	LDQ63	T	
P6	PL51B	6	LDQ50	C	PL64B	6	LDQ63	C	
VCCIO	VCCIO6	6			VCCIO6	6			
P5	PL52A	6	LDQ50	T (LVDS)*	PL65A	6	LDQ63	T (LVDS)*	
P4	PL52B	6	LDQ50	C (LVDS)*	PL65B	6	LDQ63	C (LVDS)*	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K1	PL27B	7	LDQ29	C (LVDS)*
K5	PL28A	7	LDQ29	T
K7	PL28B	7	LDQ29	C
GND	GNDIO7	-		
K4	PL29A	7	LDQS29	T (LVDS)*
K3	PL29B	7	LDQ29	C (LVDS)*
L8	PL30A	7	LDQ29	T
VCCIO	VCCIO7	7		
L6	PL30B	7	LDQ29	C
L2	PL31A	7	LDQ29	T (LVDS)*
L1	PL31B	7	LDQ29	C (LVDS)*
L7	PL32A	7	LDQ29	T
GND	GNDIO7	-		
L5	PL32B	7	LDQ29	C
L4	PL33A	7	LDQ37	T (LVDS)*
L3	PL33B	7	LDQ37	C (LVDS)*
M8	PL34A	7	LDQ37	T
M6	PL34B	7	LDQ37	C
VCCIO	VCCIO7	7		
M2	PL35A	7	LDQ37	T (LVDS)*
M1	PL35B	7	LDQ37	C (LVDS)*
M7	PL36A	7	LDQ37	T
M5	PL36B	7	LDQ37	C
GND	GNDIO7	-		
M4	PL37A	7	LDQS37	T (LVDS)*
M3	PL37B	7	LDQ37	C (LVDS)*
N6	PL38A	7	LUM0_SPLLT_IN_A/LDQ37	T
VCCIO	VCCIO7	7		
N8	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C
N5	PL39A	7	LUM0_SPLLT_FB_A/LDQ37	T
N7	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C
GND	GNDIO7	-		
VCCIO	VCCIO7	7		
T9	PL50A	7	LDQ54	
R9	PL51A	7	LDQ54	T
P7	PL51B	7	LDQ54	C
VCCIO	VCCIO7	7		
N2	PL52A	7	LDQ54	T (LVDS)*
N1	PL52B	7	LDQ54	C (LVDS)*
P6	PL53A	7	LDQ54	T
P5	PL53B	7	LDQ54	C
GND	GNDIO7	-		
P4	PL54A	7	LDQS54	T (LVDS)*

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AB6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T	
AB7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA8	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AB8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C	
AA9	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T	
Y9	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C	
AB9	PB24A	4	BDQS24****	T	PB42A	4	BDQS42****	T	
GNDIO	GNDIO4	-			GNDIO4	-			
AB10	PB24B	4	BDQ24	C	PB42B	4	BDQ42	C	
AA10	PB25A	4	BDQ24	T	PB43A	4	BDQ42	T	
Y11	PB25B	4	BDQ24	C	PB43B	4	BDQ42	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
V10	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T	
U11	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C	
V11	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T	
W11	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C	
AA11	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T	
AB11	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T11	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T	
U12	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA12	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T	
Y12	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C	
V12	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T	
W12	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C	
AB12	PB35A	4	BDQ33	T	PB53A	4	BDQ51	T	
AA13	PB35B	4	BDQ33	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T12	PB36A	4	BDQ33	T	PB54A	4	BDQ51	T	
U13	PB36B	4	BDQ33	C	PB54B	4	BDQ51	C	
V13	PB37A	4	BDQ33	T	PB55A	4	BDQ51	T	
T13	PB37B	4	BDQ33	C	PB55B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AB13	PB38A	4	BDQ42	T	PB56A	4	BDQ60	T	
AB14	PB38B	4	BDQ42	C	PB56B	4	BDQ60	C	
U14	PB39A	4	BDQ42	T	PB57A	4	BDQ60	T	
T14	PB39B	4	BDQ42	C	PB57B	4	BDQ60	C	
AA14	PB40A	4	BDQ42	T	PB58A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	BDQ42	C	PB58B	4	BDQ60	C	
W14	PB41A	4	BDQ42	T	PB59A	4	BDQ60	T	
V14	PB41B	4	BDQ42	C	PB59B	4	BDQ60	C	
AB15	PB42A	4	BDQS42	T	PB60A	4	BDQS60	T	

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	GND	-		
L12	GND	-		
L13	GND	-		
M10	GND	-		
M11	GND	-		
M12	GND	-		
M13	GND	-		
N10	GND	-		
N11	GND	-		
N12	GND	-		
N13	GND	-		
N15	GND	-		
N20	GND	-		
N3	GND	-		
N8	GND	-		
P14	GND	-		
P9	GND	-		
R10	GND	-		
R13	GND	-		
T19	GND	-		
T4	GND	-		
W16	GND	-		
W2	GND	-		
W21	GND	-		
W7	GND	-		
Y10	GND	-		
Y13	GND	-		
Y15	NC	-		
W15	NC	-		
AB20	NC	-		
AB21	NC	-		
AA21	NC	-		
AA20	NC	-		
AB19	NC	-		
AB18	NC	-		
Y22	NC	-		
Y21	NC	-		
Y17	NC	-		
Y18	NC	-		
Y16	NC	-		
W17	NC	-		
Y19	NC	-		
Y20	NC	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
M26	PR27A	2	RDQS27	T (LVDS)*	PR37A	2	RDQS37	T (LVDS)*	
L30	PR26B	2	RDQ27	C	PR36B	2	RDQ37	C	
GNDIO	GNDIO2	-			GNDIO2	-			
L29	PR26A	2	RDQ27	T	PR36A	2	RDQ37	T	
L28	PR25B	2	RDQ27	C (LVDS)*	PR35B	2	RDQ37	C (LVDS)*	
L27	PR25A	2	RDQ27	T (LVDS)*	PR35A	2	RDQ37	T (LVDS)*	
H29	PR24B	2	RDQ27	C	PR34B	2	RDQ37	C	
VCCIO	VCCIO2	2			VCCIO2	2			
G29	PR24A	2	RDQ27	T	PR34A	2	RDQ37	T	
L22	PR23B	2	RDQ27	C (LVDS)*	PR33B	2	RDQ37	C (LVDS)*	
M22	PR23A	2	RDQ27	T (LVDS)*	PR33A	2	RDQ37	T (LVDS)*	
F30	PR21B	2		C	PR31B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
F29	PR21A	2		T	PR31A	2	RDQ28	T	
-	-	-			-	-			
-	-	-			-	-			
E30	PR20B	2		C (LVDS)*	PR30B	2	RDQ28	C (LVDS)*	
E29	PR20A	2		T (LVDS)*	PR30A	2	RDQ28	T (LVDS)*	
VCCIO	VCCIO2	2			-	-			
L25	PR19B	2		C	PR29B	2	RDQ28	C	
L26	PR19A	2		T	PR29A	2	RDQ28	T	
-	-	-			VCCIO2	2			
H28	PR18B	2		C (LVDS)*	PR28B	2	RDQ28	C (LVDS)*	
J28	PR18A	2		T (LVDS)*	PR28A	2	RDQS28	T (LVDS)*	
G28	PR16B	2		C	PR27B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
G27	PR16A	2		T	PR27A	2	RDQ28	T	
L24	NC	-			PR26B	2	RDQ28	C (LVDS)*	
L23	NC	-			PR26A	2	RDQ28	T (LVDS)*	
D30	NC	-			PR25B	2	RDQ28	C	
-	-	-			VCCIO2	2			
D29	NC	-			PR25A	2	RDQ28	T	
K24	NC	-			PR24B	2	RDQ28	C (LVDS)*	
K25	NC	-			PR24A	2	RDQ28	T (LVDS)*	
J27	NC	-			PR22B	2		C	
-	-	-			GNDIO2	-			
K26	NC	-			PR22A	2		T	
K23	PR15B	2		C (LVDS)*	PR21B	2		C (LVDS)*	
K22	PR15A	2		T (LVDS)*	PR21A	2		T (LVDS)*	
J22	PR14B	2		C	PR20B	2		C	
VCCIO	VCCIO2	-			VCCIO2	2			
J23	PR14A	2		T	PR20A	2		T	
-	-	-			GNDIO2	-			
-	-	-			-	-			
J26	NC	-			PR17B	2	RDQ15	C (LVDS)*	
H26	NC	-			PR17A	2	RDQ15	T (LVDS)*	
H27	NC	-			PR16B	2	RDQ15	C	
G26	NC	-			PR16A	2	RDQ15	T	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AC19	PB96A	4	BDQS96	T
AD20	PB96B	4	BDQ96	C
AB18	PB97A	4	BDQ96	T
AC20	PB97B	4	BDQ96	C
AE20	PB98A	4	BDQ96	T
AE21	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4		
AC23	PB99A	4	BDQ96	T
AD23	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-		
AH18	LRC_SQ_VCCR3	13		
AK19	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOU3	13		T
AK21	LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOU3N	13		C
AH22	LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOU2N	13		C
AH23	LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOU2P	13		T
AH19	LRC_SQ_VCCR2	13		
AJ20	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCR1	13		
AK25	LRC_SQ_HDOU1P	13		T
AH25	LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOU1N	13		C
AH26	LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOU0N	13		C
AK27	LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOU0P	13		T
AH27	LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5Q208I	131	1.2V	-5	PQFP	208	IND	20
LFE2-20E-6Q208I	131	1.2V	-6	PQFP	208	IND	20
LFE2-20E-5F256I	193	1.2V	-5	fpBGA	256	IND	20
LFE2-20E-6F256I	193	1.2V	-6	fpBGA	256	IND	20
LFE2-20E-5F484I	331	1.2V	-5	fpBGA	484	IND	20
LFE2-20E-6F484I	331	1.2V	-6	fpBGA	484	IND	20
LFE2-20E-5F672I	402	1.2V	-5	fpBGA	672	IND	20
LFE2-20E-6F672I	402	1.2V	-6	fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484I	331	1.2V	-5	fpBGA	484	IND	35
LFE2-35E-6F484I	331	1.2V	-6	fpBGA	484	IND	35
LFE2-35E-5F672I	450	1.2V	-5	fpBGA	672	IND	35
LFE2-35E-6F672I	450	1.2V	-6	fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484I	339	1.2V	-5	fpBGA	484	IND	50
LFE2-50E-6F484I	339	1.2V	-6	fpBGA	484	IND	50
LFE2-50E-5F672I	500	1.2V	-5	fpBGA	672	IND	50
LFE2-50E-6F672I	500	1.2V	-6	fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672I	500	1.2V	-5	fpBGA	672	IND	70
LFE2-70E-6F672I	500	1.2V	-6	fpBGA	672	IND	70
LFE2-70E-5F900I	583	1.2V	-5	fpBGA	900	IND	70
LFE2-70E-6F900I	583	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100