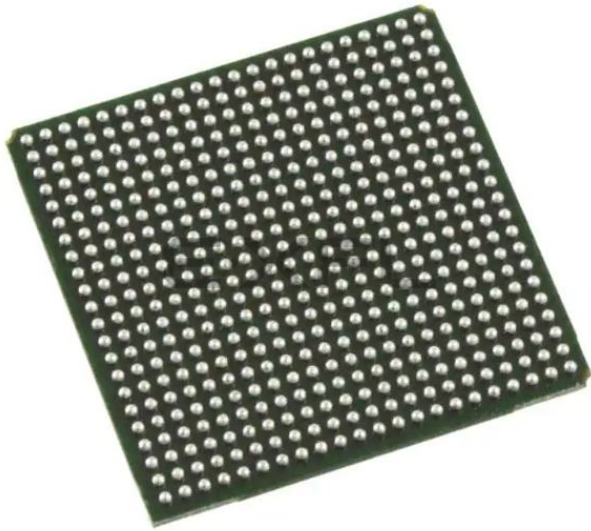




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	297
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12se-6f484c

Features

■ High Logic Density for System Integration

- 6K to 95K LUTs
- 90 to 583 I/Os

■ Embedded SERDES (LatticeECP2M Only)

- Data Rates 250 Mbps to 3.125 Gbps
- Up to 16 channels per device
PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.

■ sysDSP™ Block

- 3 to 42 blocks for high performance multiply and accumulate
- Each block supports
 - One 36x36, four 18x18 or eight 9x9 multipliers

■ Flexible Memory Resources

- 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
 - 18Kbit block
 - Single, pseudo dual and true dual port
 - Byte Enable Mode support
- 12K to 202Kbits distributed RAM
 - Single port and pseudo dual port

■ sysCLOCK Analog PLLs and DLLs

- Two GPLLs and up to six SPLLs per device
 - Clock multiply, divide, phase & delay adjust
 - Dynamic PLL adjustment
- Two general purpose DLLs per device

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- Source synchronous standards support
 - SPI4.2, SFI4 (DDR Mode), XGMII
 - High Speed ADC/DAC devices
- Dedicated DDR and DDR2 memory support
 - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
- Dedicated DQS support

■ Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces

- LVTTTL and LVCMOS 33/25/18/15/12
- SSTL 3/2/18 I, II
- HSTL15 I and HSTL18 I, II
- PCI and Differential HSTL, SSTL
- LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL

■ Flexible Device Configuration

- 1149.1 Boundary Scan compliant
- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual boot images supported
- TransFR™ I/O for simple field updates
- Soft Error Detect macro embedded

■ Optional Bitstream Encryption (LatticeECP2/M “S” Versions Only)

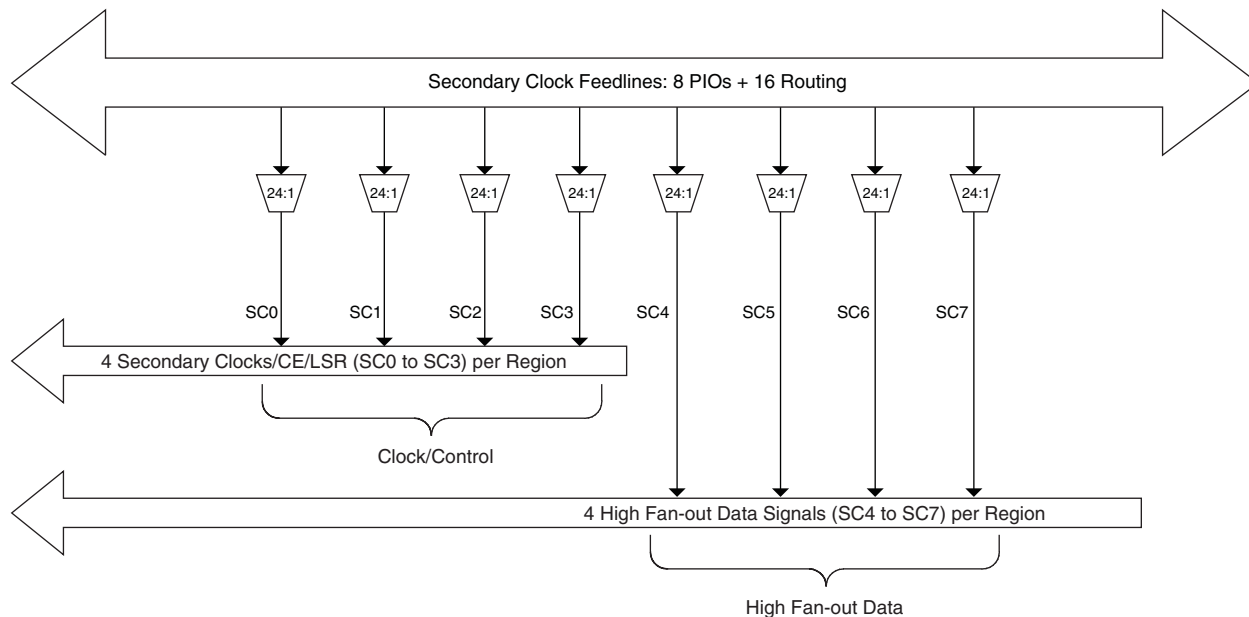
■ System Level Support

- ispTRACY™ internal logic analyzer capability
- On-chip oscillator for initialization & general use
- 1.2V power supply

Table 1-1. LatticeECP2 (Including “S-Series”) Family Selection

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

Figure 2-16. Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

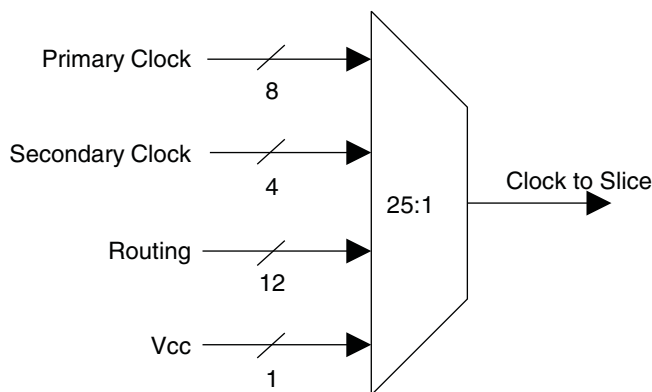
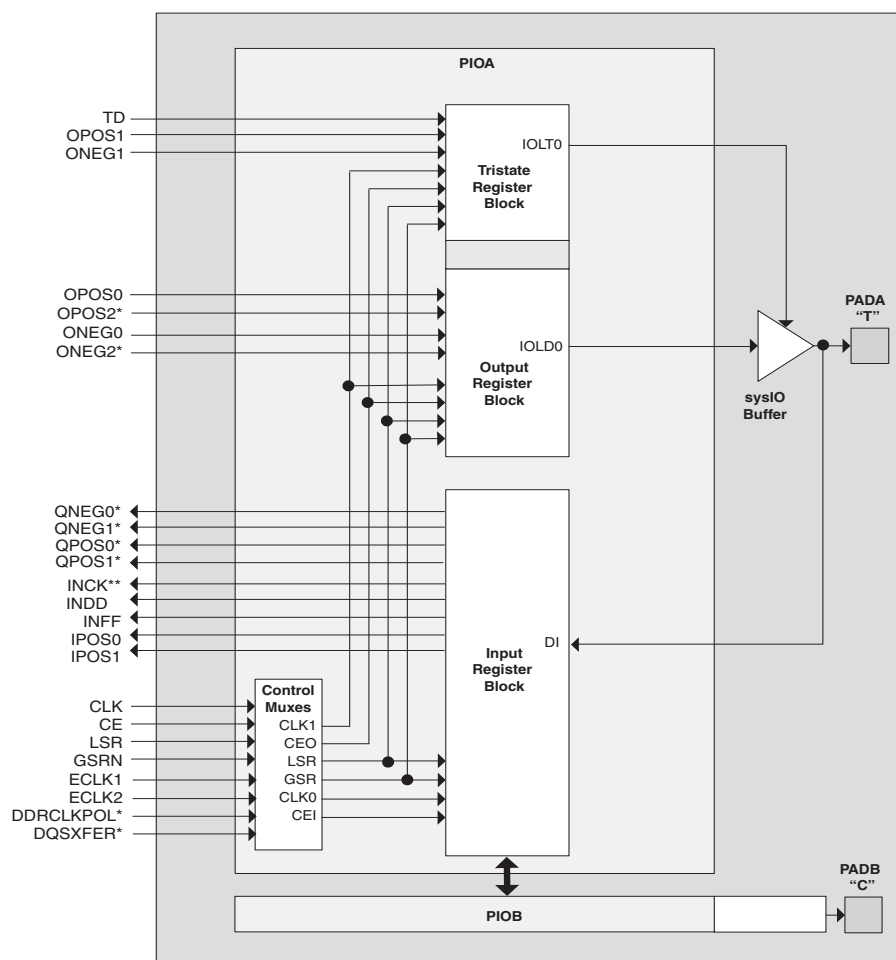


Figure 2-28. PIC Diagram



*Signals are available on left/right/bottom edges only.
** Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-28. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.40	—	1.70	—	1.90	—	ns
		LFE2M70	1.40	—	1.70	—	1.90	—	ns
		LFE2M100	1.40	—	1.70	—	1.90	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IO}	Clock Frequency of I/O Register and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)¹									
t _{COE}	Clock to Output - PIO Output Register	LFE2-6	—	2.60	—	2.90	—	3.20	ns
		LFE2-12	—	2.60	—	2.90	—	3.20	ns
		LFE2-20	—	2.60	—	2.90	—	3.20	ns
		LFE2-35	—	2.60	—	2.90	—	3.20	ns
		LFE2-50	—	2.60	—	2.90	—	3.20	ns
		LFE2-70	—	2.60	—	2.90	—	3.20	ns
		LFE2M20	—	2.60	—	2.90	—	3.20	ns
		LFE2M35	—	2.60	—	2.90	—	3.20	ns
		LFE2M50	—	3.10	—	3.40	—	3.70	ns
		LFE2M70	—	3.10	—	3.40	—	3.70	ns
		LFE2M100	—	3.10	—	3.40	—	3.70	ns

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)¹									
t _{COPLL} ¹⁰	Clock to Output - PIO Output Register	LFE2-6	—	2.30	—	2.60	—	2.80	ns
		LFE2-12	—	2.30	—	2.60	—	2.80	ns
		LFE2-20	—	2.30	—	2.60	—	2.80	ns
		LFE2-35	—	2.30	—	2.60	—	2.80	ns
		LFE2-50	—	2.30	—	2.60	—	2.80	ns
		LFE2-70	—	2.30	—	2.60	—	2.80	ns
		LFE2M20	—	2.30	—	2.60	—	2.80	ns
		LFE2M35	—	2.30	—	2.60	—	2.80	ns
		LFE2M50	—	2.60	—	2.90	—	3.10	ns
		LFE2M70	—	2.60	—	2.90	—	3.10	ns
		LFE2M100	—	2.70	—	3.00	—	3.20	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	LFE2-6	0.70	—	0.80	—	0.90	—	ns
		LFE2-12	0.70	—	0.80	—	0.90	—	ns
		LFE2-20	0.70	—	0.80	—	0.90	—	ns
		LFE2-35	0.70	—	0.80	—	0.90	—	ns
		LFE2-50	0.70	—	0.80	—	0.90	—	ns
		LFE2-70	0.70	—	0.80	—	0.90	—	ns
		LFE2M20	0.70	—	0.80	—	0.90	—	ns
		LFE2M35	0.70	—	0.80	—	0.90	—	ns
		LFE2M50	0.70	—	0.80	—	0.90	—	ns
		LFE2M70	0.70	—	0.80	—	0.90	—	ns
		LFE2M100	0.80	—	0.90	—	1.00	—	ns

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps) ⁵									
t _{SUXGMII}	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{DVBCKXGMII}	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
t _{DVACKXGMII}	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

- General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
- DDR timing numbers based on SSTL25 for BGA packages only.
- DDR2 timing numbers based on SSTL18 for BGA packages only.
- SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
- XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
- IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
- Using the LVDS I/O standard.
- ECP2-6 and ECP2-12 do not support SPI4.2
- The AC numbers do not apply to PCLK6 and PCLK7.
- Applies to CLKOP only.
- Please refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#) for best performance.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]_SQ_VCCI _{Bm}	—	Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_VCCO _{Bm}	—	Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_HDOUT _{Nm}	O	High-speed output, negative channel m
[LOC]_SQ_HDOUT _{Pm}	O	High-speed output, positive channel m
[LOC]_SQ_HDIN _{Nm}	I	High-speed input, negative channel m
[LOC]_SQ_HDIN _{Pm}	I	High-speed input, positive channel m
[LOC]_SQ_VCCTX _m ⁴	—	Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.
[LOC]_SQ_VCCR _{Xm} ⁴	—	Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#).
5. There may be SPLs that do not have dedicated I/Os.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
5	GND	-			GND	-			
6	PL6A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ16	T (LVDS)*	
7	VCCAUX	-			VCCAUX	-			
8	PL6B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ16	C (LVDS)*	
9	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
10	VCCIO7	7			VCCIO7	7			
11	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
12	VCC	-			VCC	-			
13	GND	-			GND	-			
14	VCCIO7	7			VCCIO7	7			
15	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
16	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
17	GND	-			GND	-			
18	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
19	VCC	-			VCC	-			
20	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
21	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
22	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*	
23	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T	
24	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C	
25	GND	-			GND	-			
26	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*	
27	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*	
28	VCC	-			VCC	-			
29	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
30	VCCAUX	-			VCCAUX	-			
31	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*	
32	GND	-			GND	-			
33	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T	
34	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*	
35	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C	
36	PL23A	6			PL33A	6	LDQ34		
37	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*	
38	VCCIO6	6			VCCIO6	6			
39	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*	
40	VCC	-			VCC	-			
41	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*	
42	GND	-			GND	-			
43	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
44	VCCIO6	6			VCCIO6	6			
45	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L2	NC	-			NC	-		
L1	NC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
M2	NC	-			NC	-		
M1	NC	-			NC	-		
N2	NC	-			NC	-		
GND	GNDIO7	-			GNDIO7	-		
M8	VCC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
GND	GNDIO7	-			GNDIO7	-		
N1	PL12A	7	LDQ16		PL18A	7	LDQ22	
L8	PL13A	7	LDQ16	T	PL19A	7	LDQ22	T
K8	PL13B	7	LDQ16	C	PL19B	7	LDQ22	C
VCCIO	VCCIO7	7			VCCIO7	7		
L6	PL14A	7	LDQ16	T (LVDS)*	PL20A	7	LDQ22	T (LVDS)*
K5	PL14B	7	LDQ16	C (LVDS)*	PL20B	7	LDQ22	C (LVDS)*
L7	PL15A	7	LDQ16	T	PL21A	7	LDQ22	T
L5	PL15B	7	LDQ16	C	PL21B	7	LDQ22	C
GND	GNDIO7	-			GNDIO7	-		
P1	PL16A	7	LDQS16	T (LVDS)*	PL22A	7	LDQS22	T (LVDS)*
P2	PL16B	7	LDQ16	C (LVDS)*	PL22B	7	LDQ22	C (LVDS)*
M6	PL17A	7	LDQ16	T	PL23A	7	LDQ22	T
VCCIO	VCCIO7	7			VCCIO7	7		
N8	PL17B	7	LDQ16	C	PL23B	7	LDQ22	C
R1	PL18A	7	LDQ16	T (LVDS)*	PL24A	7	LDQ22	T (LVDS)*
R2	PL18B	7	LDQ16	C (LVDS)*	PL24B	7	LDQ22	C (LVDS)*
M7	PL19A	7	PCLKT7_0/LDQ16	T	PL25A	7	PCLKT7_0/LDQ22	T
GND	GNDIO7	-			GNDIO7	-		
N9	PL19B	7	PCLKC7_0/LDQ16	C	PL25B	7	PCLKC7_0/LDQ22	C
M4	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	PL27A	6	PCLKT6_0/LDQ31	T (LVDS)*
M5	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*	PL27B	6	PCLKC6_0/LDQ31	C (LVDS)*
N7	PL22A	6	VREF2_6/LDQ25	T	PL28A	6	VREF2_6/LDQ31	T
P9	PL22B	6	VREF1_6/LDQ25	C	PL28B	6	VREF1_6/LDQ31	C
N3	PL23A	6	LDQ25	T (LVDS)*	PL29A	6	LDQ31	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
N4	PL23B	6	LDQ25	C (LVDS)*	PL29B	6	LDQ31	C (LVDS)*
N5	PL24A	6	LDQ25	T	PL30A	6	LDQ31	T
P7	PL24B	6	LDQ25	C	PL30B	6	LDQ31	C
T1	NC	-			PL31A	6	LDQS31	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
T2	NC	-			PL31B	6	LDQ31	C (LVDS)*
P8	NC	-			PL32A	6	LDQ31	T
P6	NC	-			PL32B	6	LDQ31	C
VCCIO	VCCIO6	6			VCCIO6	6		
P5	NC	-			PL33A	6	LDQ31	T (LVDS)*
P4	NC	-			PL33B	6	LDQ31	C (LVDS)*

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GND	GNDIO5	-			GNDIO5	-			
W10	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
Y10	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AA10	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AC8	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD8	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AB8	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AB10	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AE6	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
AF6	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
AA11	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AC9	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AB9	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	
AD9	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y11	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AB11	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
AE7	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
AF7	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AC10	PB20A	5	BDQ24	T	PB20A	5	BDQ24	T	
AD10	PB20B	5	BDQ24	C	PB20B	5	BDQ24	C	
AA12	PB21A	5	BDQ24	T	PB21A	5	BDQ24	T	
W12	PB21B	5	BDQ24	C	PB21B	5	BDQ24	C	
AB12	PB22A	5	BDQ24	T	PB22A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
Y12	PB22B	5	BDQ24	C	PB22B	5	BDQ24	C	
AD12	PB23A	5	BDQ24	T	PB23A	5	BDQ24	T	
AC12	PB23B	5	BDQ24	C	PB23B	5	BDQ24	C	
AC13	PB24A	5	BDQS24	T	PB24A	5	BDQS24	T	
GND	GNDIO5	-			GNDIO5	-			
AA13	PB24B	5	BDQ24	C	PB24B	5	BDQ24	C	
AD13	PB25A	5	BDQ24	T	PB25A	5	BDQ24	T	
AC14	PB25B	5	BDQ24	C	PB25B	5	BDQ24	C	
AE8	PB26A	5	BDQ24	T	PB26A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB26B	5	BDQ24	C	PB26B	5	BDQ24	C	
AB15	PB27A	5	BDQ24	T	PB27A	5	BDQ24	T	
Y13	PB27B	5	BDQ24	C	PB27B	5	BDQ24	C	
AE9	PB28A	5	BDQ24	T	PB28A	5	BDQ24	T	
GND	GNDIO5	-			GNDIO5	-			
AF9	PB28B	5	BDQ24	C	PB28B	5	BDQ24	C	
W13	PB29A	5	BDQ33	T	PB29A	5	BDQ33	T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W7	PL72B	6	LDQ71	C
W4	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*
W3	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*
W6	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T
GND	GNDIO6	-		
W8	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C
Y8	LLM0_PLLCAP	6		
Y1	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*
Y2	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*
Y5	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T
Y6	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C
Y4	PL78A	6	LDQ80	T (LVDS)*
VCCIO	VCCIO6	6		
Y3	PL78B	6	LDQ80	C (LVDS)*
AA6	PL79A	6	LDQ80	T
AA8	PL79B	6	LDQ80	C
AA2	PL80A	6	LDQS80	T (LVDS)*
GND	GNDIO6	-		
AA1	PL80B	6	LDQ80	C (LVDS)*
AA7	PL81A	6	LDQ80	T
AA5	PL81B	6	LDQ80	C
VCCIO	VCCIO6	6		
AA4	PL82A	6	LDQ80	T (LVDS)*
AA3	PL82B	6	LDQ80	C (LVDS)*
AB7	PL83A	6	LDQ80	T
AB5	PL83B	6	LDQ80	C
GND	GNDIO6	-		
AB2	PL84A	6	LDQ88	T (LVDS)*
AB1	PL84B	6	LDQ88	C (LVDS)*
AB8	PL85A	6	LDQ88	T
AB6	PL85B	6	LDQ88	C
VCCIO	VCCIO6	6		
AB4	PL86A	6	LDQ88	T (LVDS)*
AB3	PL86B	6	LDQ88	C (LVDS)*
AC7	PL87A	6	LDQ88	T
AC5	PL87B	6	LDQ88	C
GND	GNDIO6	-		
AC2	PL88A	6	LDQS88	T (LVDS)*
AC1	PL88B	6	LDQ88	C (LVDS)*
AC6	PL89A	6	LDQ88	T
VCCIO	VCCIO6	6		
AD6	PL89B	6	LDQ88	C
AD1	PL90A	6	LDQ88	T (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F14	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C(LVDS)*	
F13	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
GNDIO	GNDIO2	-			GNDIO2	-			
H11	PR14B	2		C	PR14B	2	RDQ15	C	
G11	PR14A	2		T	PR14A	2	RDQ15	T	
E13	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C(LVDS)*	
F12	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C(LVDS)*	
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
GNDIO	GNDIO2	-			GNDIO2	-			
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
F4	XRES	-			XRES	-			
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12			
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T	
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T	
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T	
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12			
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T	
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C	
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T	
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T	
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
T1	PL65A	6	LLM0_GDLLT_FB_A	T
T2	PL65B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	-		
R7	LLM0_PLLCAP	6		
T6	PL67A	6	LDQ71	T (LVDS)*
T7	PL67B	6	LDQ71	C (LVDS)*
U1	PL68A	6	LDQ71	T
U2	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
T3	PL69A	6	LDQ71	T (LVDS)*
U3	PL69B	6	LDQ71	C (LVDS)*
U6	PL70A	6	LDQ71	T
U5	PL70B	6	LDQ71	C
GNDIO	GNDIO6	-		
V5	PL71A	6	LDQS71	T (LVDS)*
U4	PL71B	6	LDQ71	C (LVDS)*
V1	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		
V3	PL72B	6	LDQ71	C
W1	PL73A	6	LDQ71	T (LVDS)*
Y1	PL73B	6	LDQ71	C (LVDS)*
AA1	PL74A	6	LDQ71	T
GNDIO	GNDIO6	-		
AA2	PL74B	6	LDQ71	C
V4	TCK	-		
Y2	TDI	-		
Y3	TMS	-		
W3	TDO	-		
W4	VCCJ	-		
W5	PB2A	5	BDQ6	T
Y4	PB2B	5	BDQ6	C
W6	PB3A	5	BDQ6	T
V6	PB3B	5	BDQ6	C
AA3	PB4A	5	BDQ6	T
AB2	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5		
T8	PB5A	5	BDQ6	T
U7	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-		
U8	PB6A	5	BDQS6	T
T9	PB6B	5	BDQ6	C
V8	PB7A	5	BDQ6	T
W8	PB7B	5	BDQ6	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
-	-	-			VCCIO5	5			
-	-	-			GNDIO5	-			
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T	
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C	
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T	
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C	
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C	
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T	
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C	
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C	
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T	
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C	
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C	
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T	
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C	
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T	
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C	
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T	
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C	
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T	
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C	
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T	
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C	
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T	
GNDIO	GNDIO4	-			GNDIO4	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L5	PL23A	7	LDQ27	T (LVDS)*	PL33A	7	LDQ37	T (LVDS)*	
L4	PL23B	7	LDQ27	C (LVDS)*	PL33B	7	LDQ37	C (LVDS)*	
N9	PL24A	7	LDQ27	T	PL34A	7	LDQ37	T	
N7	PL24B	7	LDQ27	C	PL34B	7	LDQ37	C	
K2	PL25A	7	LDQ27	T (LVDS)*	PL35A	7	LDQ37	T (LVDS)*	
K1	PL25B	7	LDQ27	C (LVDS)*	PL35B	7	LDQ37	C (LVDS)*	
P9	PL26A	7	LDQ27	T	PL36A	7	LDQ37	T	
P7	PL26B	7	LDQ27	C	PL36B	7	LDQ37	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M6	PL27A	7	LDQS27	T (LVDS)*	PL37A	7	LDQS37	T (LVDS)*	
M5	PL27B	7	LDQ27	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
N5	PL28A	7	LDQ27	T	PL38A	7	LDQ37	T	
N6	PL28B	7	LDQ27	C	PL38B	7	LDQ37	C	
M4	PL29A	7	LDQ27	T (LVDS)*	PL39A	7	LDQ37	T (LVDS)*	
M3	PL29B	7	LDQ27	C (LVDS)*	PL39B	7	LDQ37	C (LVDS)*	
P6	PL30A	7	LDQ27	T	PL40A	7	LDQ37	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P8	PL30B	7	LDQ27	C	PL40B	7	LDQ37	C	
L3	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	
L2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	
P5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	
P4	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	
L1	PL34A	7	LDQ36	T (LVDS)*	PL44A	7	LDQ46	T (LVDS)*	
M2	PL34B	7	LDQ36	C (LVDS)*	PL44B	7	LDQ46	C (LVDS)*	
R5	PL35A	7	LDQ36	T	PL45A	7	LDQ46	T	
R4	PL35B	7	LDQ36	C	PL45B	7	LDQ46	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M1	PL36A	7	LDQS36	T (LVDS)*	PL46A	7	LDQS46	T (LVDS)*	
N2	PL36B	7	LDQ36	C (LVDS)*	PL46B	7	LDQ46	C (LVDS)*	
R8	PL37A	7	LDQ36	T	PL47A	7	LDQ46	T	
T9	PL37B	7	LDQ36	C	PL47B	7	LDQ46	C	
P3	PL38A	7	LDQ36	T (LVDS)*	PL48A	7	LDQ46	T (LVDS)*	
P2	PL38B	7	LDQ36	C (LVDS)*	PL48B	7	LDQ46	C (LVDS)*	
N1	PL39A	7	PCLKT7_0/LDQ36	T	PL49A	7	PCLKT7_0/LDQ46	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P1	PL39B	7	PCLKC7_0/LDQ36	C	PL49B	7	PCLKC7_0/LDQ46	C	
T5	PL41A	6	PCLKT6_0	T (LVDS)*	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	
T4	PL41B	6	PCLKC6_0	C (LVDS)*	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	
U7	PL42A	6	VREF2_6	T	PL52A	6	VREF2_6/LDQ55	T	
T8	PL42B	6	VREF1_6	C	PL52B	6	VREF1_6/LDQ55	C	
R3	PL43A	6		T (LVDS)*	PL53A	6	LDQ55	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
R2	PL43B	6		C (LVDS)*	PL53B	6	LDQ55	C (LVDS)*	
R1	PL44A	6		T	PL54A	6	LDQ55	T	
T1	PL44B	6		C	PL54B	6	LDQ55	C	
GNDIO	GNDIO6	-			GNDIO6	-			
-	-	-			VCCIO6	6			
T3	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB16	GND	-			GND	-		
AB17	GND	-			GND	-		
AB18	GND	-			GND	-		
AB19	GND	-			GND	-		
AB26	GND	-			GND	-		
AB31	GND	-			GND	-		
AB4	GND	-			GND	-		
AB9	GND	-			GND	-		
AC16	GND	-			GND	-		
AC17	GND	-			GND	-		
AC18	GND	-			GND	-		
AC19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE27	GND	-			GND	-		
AE31	GND	-			GND	-		
AE4	GND	-			GND	-		
AE8	GND	-			GND	-		
AF12	GND	-			GND	-		
AF16	GND	-			GND	-		
AF19	GND	-			GND	-		
AF23	GND	-			GND	-		
AG31	GND	-			GND	-		
AH31	GND	-			GND	-		
AH4	GND	-			GND	-		
AJ14	GND	-			GND	-		
AJ21	GND	-			GND	-		
AK27	GND	-			GND	-		
AK8	GND	-			GND	-		
AL10	GND	-			GND	-		
AL16	GND	-			GND	-		
AL19	GND	-			GND	-		
AL2	GND	-			GND	-		
AL25	GND	-			GND	-		
AL33	GND	-			GND	-		
AP1	GND	-			GND	-		
AP10	GND	-			GND	-		
AP13	GND	-			GND	-		
AP22	GND	-			GND	-		
AP25	GND	-			GND	-		
AP34	GND	-			GND	-		
D10	GND	-			GND	-		
D16	GND	-			GND	-		
D19	GND	-			GND	-		
D2	GND	-			GND	-		
D25	GND	-			GND	-		
D33	GND	-			GND	-		
E27	GND	-			GND	-		
E8	GND	-			GND	-		
F14	GND	-			GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F21	GND	-			GND	-		
G31	GND	-			GND	-		
G4	GND	-			GND	-		
J12	GND	-			GND	-		
J16	GND	-			GND	-		
J19	GND	-			GND	-		
J23	GND	-			GND	-		
K27	GND	-			GND	-		
K31	GND	-			GND	-		
K4	GND	-			GND	-		
K8	GND	-			GND	-		
M16	GND	-			GND	-		
M17	GND	-			GND	-		
M18	GND	-			GND	-		
M19	GND	-			GND	-		
N16	GND	-			GND	-		
N17	GND	-			GND	-		
N18	GND	-			GND	-		
N19	GND	-			GND	-		
N26	GND	-			GND	-		
N31	GND	-			GND	-		
N4	GND	-			GND	-		
N9	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R19	GND	-			GND	-		
T12	GND	-			GND	-		
T13	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T19	GND	-			GND	-		
T20	GND	-			GND	-		
T22	GND	-			GND	-		
T23	GND	-			GND	-		
T26	GND	-			GND	-		
T31	GND	-			GND	-		
T4	GND	-			GND	-		
T9	GND	-			GND	-		
U12	GND	-			GND	-		
U13	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U19	GND	-			GND	-		
U20	GND	-			GND	-		