Lattice Semiconductor Corporation - LFE2-12SE-6FN256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12se-6fn256i

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2/M family of devices has two DLLs per device.

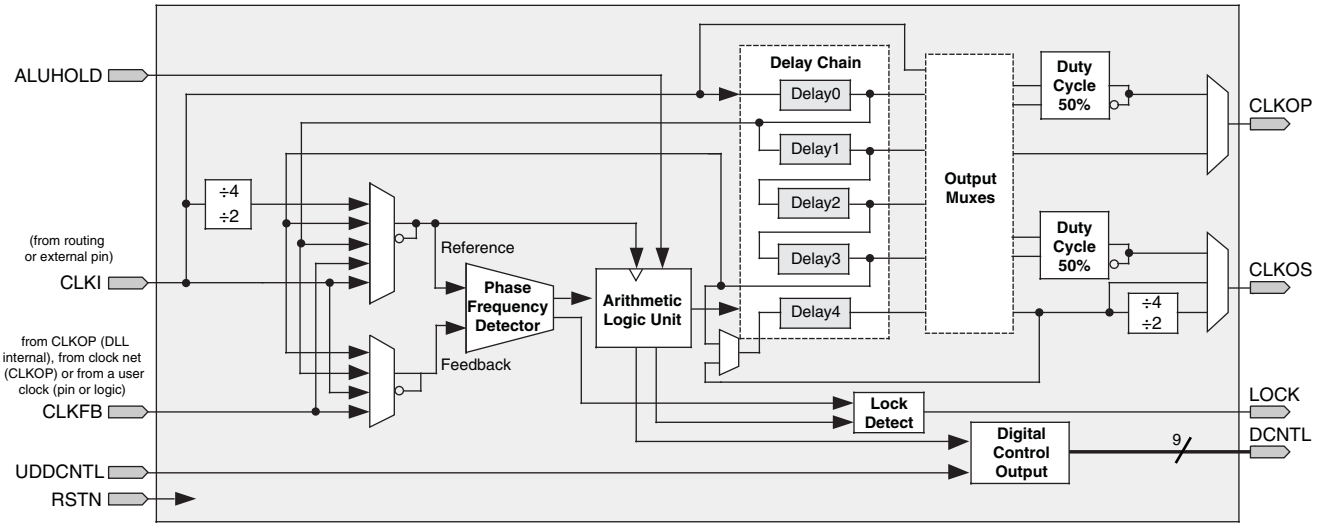
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is fed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLLDELA delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-6 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-6. Delay Locked Loop Diagram (DLL)



LatticeECP2 Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply Current	ECP2-6	10	mA
		ECP2-12	20	mA
		ECP2-20	30	mA
		ECP2-35	50	mA
		ECP2-50	70	mA
		ECP2-70	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	24	mA
		ECP2-12	24	mA
		ECP2-20	24	mA
		ECP2-35	24	mA
		ECP2-50	24	mA
		ECP2-70	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2-6	2	mA
		ECP2-12	2	mA
		ECP2-20	2	mA
		ECP2-35	2	mA
		ECP2-50	2	mA
		ECP2-70	2	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at normal voltage.

RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

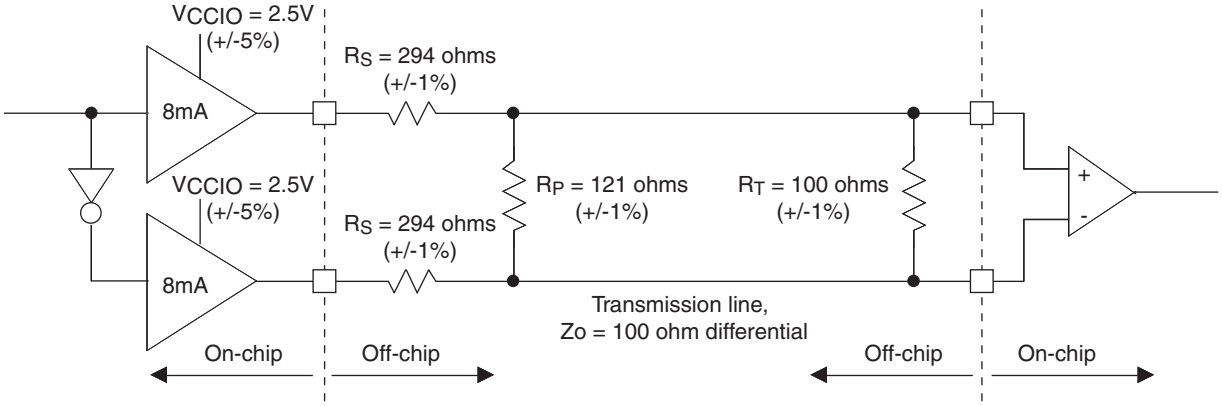


Table 3-5. RSDS DC Conditions[1]

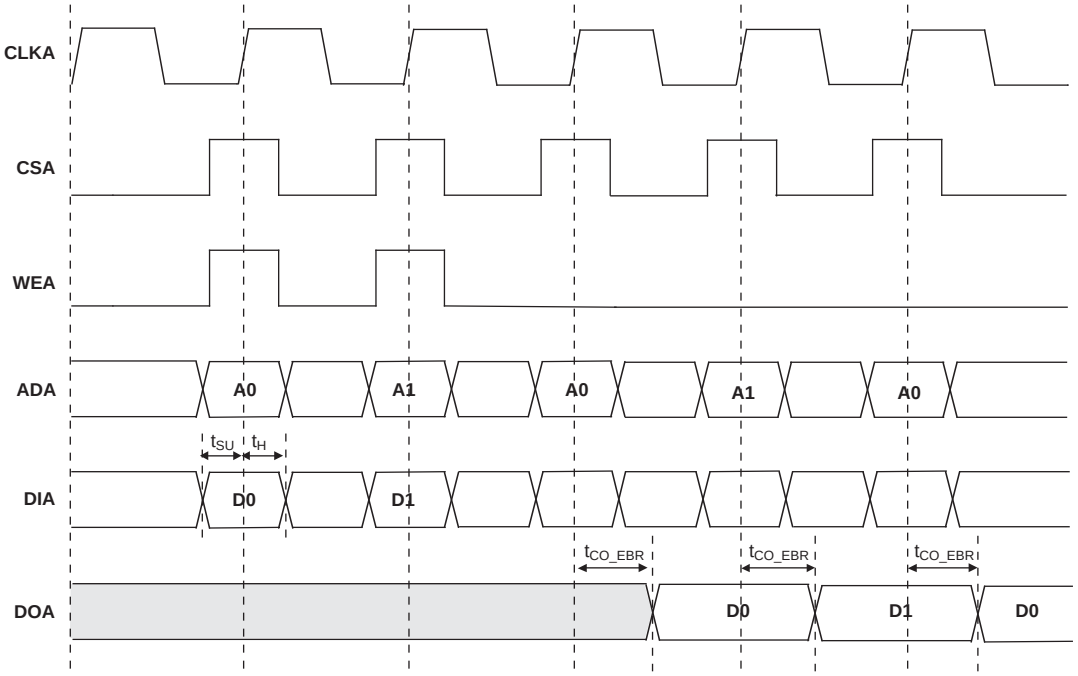
Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

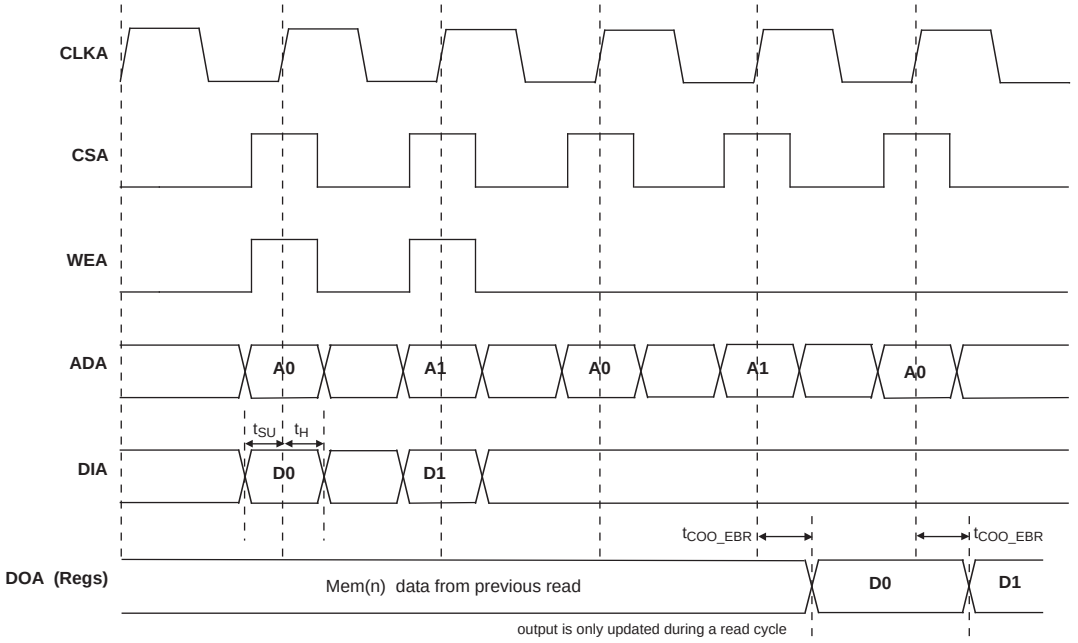
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



LatticeECP2/M Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.04	-0.02	0.00	ns
BLVDS25	BLVDS	-0.04	-0.09	-0.15	ns
MLVDS	LVDS	-0.15	-0.15	-0.15	ns
RSDS	RSDS	-0.15	-0.15	-0.15	ns
LVPECL33	LVPECL	0.16	0.15	0.13	ns
HSTL18_I	HSTL_18 class I	0.01	-0.01	-0.04	ns
HSTL18_II	HSTL_18 class II	0.01	-0.01	-0.04	ns
HSTL18D_I	Differential HSTL 18 class I	0.01	-0.01	-0.04	ns
HSTL18D_II	Differential HSTL 18 class II	0.01	-0.01	-0.04	ns
HSTL15_I	HSTL_15 class I	0.01	-0.01	-0.04	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	-0.01	-0.04	ns
SSTL33_I	SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33_II	SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL33D_I	Differential SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33D_II	Differential SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL25_I	SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25_II	SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25D_II	Differential SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL18_I	SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18_II	SSTL_18 class II	-0.01	-0.04	-0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18D_II	Differential SSTL_18 class II	-0.01	-0.04	-0.07	ns
LVTTL33	LVTTL	-0.16	-0.16	-0.16	ns
LVCMOS33	LVCMOS 3.3	-0.08	-0.12	-0.16	ns
LVCMOS25	LVCMOS 2.5	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS 1.8	-0.16	-0.17	-0.17	ns
LVCMOS15	LVCMOS 1.5	-0.14	-0.14	-0.14	ns
LVCMOS12	LVCMOS 1.2	-0.04	-0.01	0.01	ns
PCI33	PCI	-0.08	-0.12	-0.16	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E[4]	0.25	0.19	0.13	ns
LVDS25	LVDS 2.5	0.10	0.13	0.17	ns
BLVDS25	BLVDS 2.5	0.00	-0.01	-0.03	ns
MLVDS	MLVDS 2.5[4]	0.00	-0.01	-0.03	ns
RSDS	RSDS 2.5[4]	0.25	0.19	0.13	ns
LVPECL33	LVPECL 3.3[4]	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18_II	HSTL_18 class II	-0.30	-0.34	-0.37	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.34	-0.37	ns

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor[5, 6]	2	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	20	—	420	MHz
		With external capacitor[5]	5	—	50	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.156	—	210	MHz
		With external capacitor[5]	0.039	—	25	MHz
f_{VCO}	PLL VCO Frequency		640	—	1280	MHz
f_{PFD}	Phase Detector Input Frequency	Without external capacitor	20	—	420	MHz
		With external capacitor[5, 6]	2	—	50	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	±0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	—	±125	ps
		$50 \leq f_{OUT} < 100$ MHz	—		0.025	UIPP
		$f_{OUT} < 50$ MHz	—	—	0.04	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—	150	µs
		With external capacitor[5]	—	—	500	µs
t_{PA}	Programmable Delay Unit		85	130	360	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor[5]	20	—	—	µs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. f_{OUT} (max) = f_{IN} * 10 for f_{IN} < 5MHz.

LatticeECP2/M sysCONFIG Port Timing Specifications (Continued)

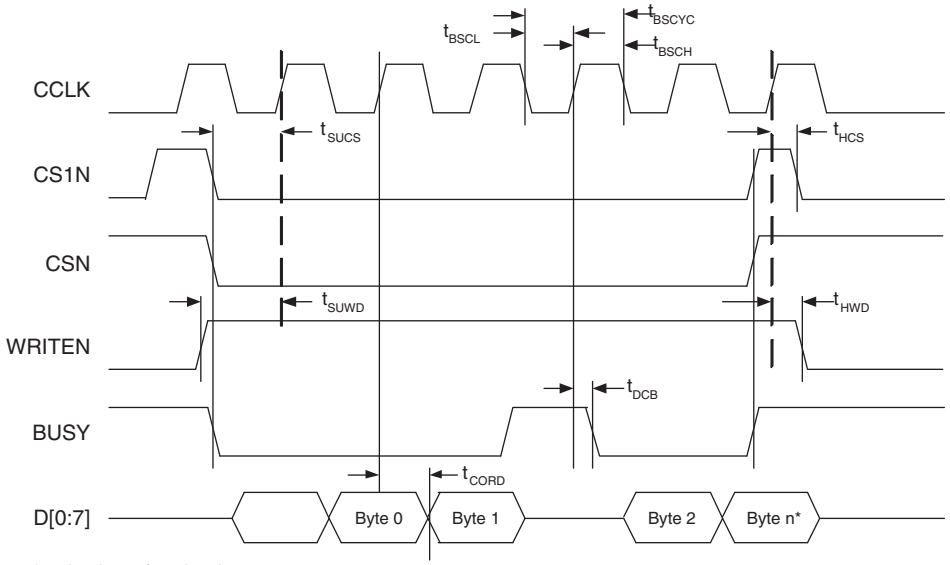
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
f_{MAXSPI}	Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1)	—	20	MHz
	Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0)	—	50	MHz
	Max. CCLK Frequency - Encrypted Bitstream	—	10	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	2	—	ns
t_{SUMCDI}	DI Setup to CCLK	7	—	ns
t_{HMCDI}	DI Hold from CCLK	1	—	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.
2. For SED (Soft Error Detect), the SEDCLKIN operating frequency must be at least 20MHz. SEDCLKIN is derived from Master Clock Frequency that has a +/-30% variation..

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
Duty Cycle	40	60	%

Figure 3-14. sysCONFIG Parallel Port Read Cycle



*n = last byte of read cycle.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Bottom Edge of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Single Ended User I/O		339	500	500	583
Differential Pair User I/O		169	249	249	290
Configuration	TAP Pins	5	5	5	5
	Muxed Pins	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7
Non Configuration	Muxed Pins	68	79	79	89
	Dedicated Pins	3	3	3	3
VCC		16	20	20	26
VCCAUX		16	16	16	17
VCCPLL		4	4	2	4
VCCIO	Bank0	4	5	5	6
	Bank1	4	5	5	6
	Bank2	4	5	5	6
	Bank3	4	5	5	6
	Bank4	4	5	5	6
	Bank5	4	5	5	6
	Bank6	4	5	5	6
	Bank7	4	5	5	6
	Bank8	2	2	2	2
GND, GND0 to GND7		60	72	72	104
NC		0	3	5	101
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	50/25	67/33	67/33	84/42
	Bank1	46/23	66/33	66/33	76/38
	Bank2	38/19	56/28	56/28	74/37
	Bank3	22/11	48/24	48/24	48/24
	Bank4	46/23	62/31	62/31	72/35
	Bank5	46/23	68/34	68/34	80/40
	Bank6	40/20	64/32	64/32	64/32
	Bank7	37/18	55/27	55/27	71/35
	Bank8	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0
	Bank2 (Right Edge)	9	13	13	18
	Bank3 (Right Edge)	5	12	12	12
	Bank4 (Bottom Edge)	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0
	Bank6 (Left Edge)	10	16	16	16
	Bank7 (Left Edge)	8	12	12	16
	Bank8 (Right Edge)	0	0	0	0

LatticeECP2 Power Supply and NC

Signals	144 TQFP[3]	208 PQFP[3]	256 fpBGA[4]	484 fpBGA[4]
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	**LFE2-6:** G7, G9, G10, H7, J10, K10, K8 **LFE2-12/LFE2-20:** G7, G9, G10, H7, J10, K10, K8	**LFE2-12/LFE2-20:** N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 **LFE2-35/LFE2-50:** J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	**LFE2-12/LFE2-20:** None **LFE2-35:** N6, N18 **LFE2-50:** N6, N18, K6, J16
GND[1]	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC[2]	**LFE2-6:** 45, 46, 124, 127 **LFE2-12:** 127	None	**LFE2-6:** K6, R3, P4 **LFE2-12/LFE2-20:** None	**LFE2-12:** E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-20/LFE2-35:** K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-50:** None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
G5	VCCAUX	-			VCCAUX	0		
K5	VCCAUX	-			VCCAUX	0		
R5	VCCAUX	-			VCCAUX	1		
V7	VCCAUX	-			VCCAUX	1		
V11	VCCAUX	-			VCCAUX	2		
V8	VCCAUX	-			VCCAUX	2		
V13	VCCAUX	-			VCCAUX	3		
V15	VCCAUX	-			VCCAUX	3		
M17	VCCAUX	-			VCCAUX	4		
P17	VCCAUX	-			VCCAUX	4		
E17	VCCAUX	-			VCCAUX	5		
G18	VCCAUX	-			VCCAUX	5		
D11	VCCAUX	-			VCCAUX	6		
F13	VCCAUX	-			VCCAUX	6		
C5	VCCAUX	-			VCCAUX	7		
E6	VCCAUX	-			VCCAUX	7		
G10	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
H8	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
G11	VCCIO1	1			VCCIO1	1		
G12	VCCIO1	1			VCCIO1	1		
G13	VCCIO1	1			VCCIO1	1		
G14	VCCIO1	1			VCCIO1	1		
H14	VCCIO2	2			VCCIO2	2		
H15	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K16	VCCIO2	2			VCCIO2	2		
L16	VCCIO3	3			VCCIO3	3		
M16	VCCIO3	3			VCCIO3	3		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR18B	2	RDQ16	C (LVDS)*	PR24B	2	RDQ22	C (LVDS)*
K22	PR18A	2	RDQ16	T (LVDS)*	PR24A	2	RDQ22	T (LVDS)*
M24	PR17B	2	RDQ16	C	PR23B	2	RDQ22	C
N23	PR17A	2	RDQ16	T	PR23A	2	RDQ22	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR16B	2	RDQ16	C (LVDS)*	PR22B	2	RDQ22	C (LVDS)*
K25	PR16A	2	RDQS16	T (LVDS)*	PR22A	2	RDQS22	T (LVDS)*
M20	PR15B	2	RDQ16	C	PR21B	2	RDQ22	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR15A	2	RDQ16	T	PR21A	2	RDQ22	T
L22	PR14B	2	RDQ16	C (LVDS)*	PR20B	2	RDQ22	C (LVDS)*
M22	PR14A	2	RDQ16	T (LVDS)*	PR20A	2	RDQ22	T (LVDS)*
K21	PR13B	2	RDQ16	C	PR19B	2	RDQ22	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR13A	2	RDQ16	T	PR19A	2	RDQ22	T
K24	PR12B	2	RDQ16	C (LVDS)*	PR18B	2	RDQ22	C (LVDS)*
J24	PR12A	2	RDQ16	T (LVDS)*	PR18A	2	RDQ22	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	NC	-			NC	-		
J25	NC	-			NC	-		
J23	NC	-			NC	-		
K23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
H26	NC	-			NC	-		
H25	NC	-			NC	-		
H24	NC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
H23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR11B	2	RDQ8	C	PR17B	2	RDQ14	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR11A	2	RDQ8	T	PR17A	2	RDQ14	T
F26	PR10B	2	RDQ8	C (LVDS)*	PR16B	2	RDQ14	C (LVDS)*
F25	PR10A	2	RDQ8	T (LVDS)*	PR16A	2	RDQ14	T (LVDS)*
K20	PR9B	2	RDQ8	C	PR15B	2	RDQ14	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR9A	2	RDQ8	T	PR15A	2	RDQ14	T
E26	PR8B	2	RDQ8	C (LVDS)*	PR14B	2	RDQ14	C (LVDS)*
E25	PR8A	2	RDQS8	T (LVDS)*	PR14A	2	RDQS14	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR7B	2	RDQ8	C	PR13B	2	RDQ14	C
H22	PR7A	2	RDQ8	T	PR13A	2	RDQ14	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L2	PL24B	7	LDQ24	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*
L1	PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T	PL38A	7	LUM0_SPLLT_IN_A/LDQ37	T
VCCIO	VCCIO7	7			VCCIO7	7		
M2	PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C
M1	PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T	PL39A	7	LUM0_SPLLT_FB_A/LDQ37	T
N2	PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C
GND	GNDIO7	-			GNDIO7	-		
M8	VCCPLL	7			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
GND	GNDIO7	-			GNDIO7	-		
N1	PL37A	7	LDQ41		PL50A	7	LDQ54	
L8	PL38A	7	LDQ41	T	PL51A	7	LDQ54	T
K8	PL38B	7	LDQ41	C	PL51B	7	LDQ54	C
VCCIO	VCCIO7	7			VCCIO7	7		
L6	PL39A	7	LDQ41	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*
K5	PL39B	7	LDQ41	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*
L7	PL40A	7	LDQ41	T	PL53A	7	LDQ54	T
L5	PL40B	7	LDQ41	C	PL53B	7	LDQ54	C
GND	GNDIO7	-			GNDIO7	-		
P1	PL41A	7	LDQS41	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*
P2	PL41B	7	LDQ41	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*
M6	PL42A	7	LDQ41	T	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7			VCCIO7	7		
N8	PL42B	7	LDQ41	C	PL55B	7	LDQ54	C
R1	PL43A	7	LDQ41	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*
R2	PL43B	7	LDQ41	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*
M7	PL44A	7	PCLKT7_0/LDQ41	T	PL57A	7	PCLKT7_0/LDQ54	T
GND	GNDIO7	-			GNDIO7	-		
N9	PL44B	7	PCLKC7_0/LDQ41	C	PL57B	7	PCLKC7_0/LDQ54	C
M4	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
M5	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
N7	PL47A	6	VREF2_6/LDQ50	T	PL60A	6	VREF2_6/LDQ63	T
P9	PL47B	6	VREF1_6/LDQ50	C	PL60B	6	VREF1_6/LDQ63	C
N3	PL48A	6	LDQ50	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
N4	PL48B	6	LDQ50	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*
N5	PL49A	6	LDQ50	T	PL62A	6	LDQ63	T
P7	PL49B	6	LDQ50	C	PL62B	6	LDQ63	C
T1	PL50A	6	LDQS50	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
T2	PL50B	6	LDQ50	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*
P8	PL51A	6	LDQ50	T	PL64A	6	LDQ63	T
P6	PL51B	6	LDQ50	C	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6			VCCIO6	6		
P5	PL52A	6	LDQ50	T (LVDS)*	PL65A	6	LDQ63	T (LVDS)*
P4	PL52B	6	LDQ50	C (LVDS)*	PL65B	6	LDQ63	C (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
K28	PR25A	2	RDQ29	T (LVDS)*
J24	PR24B	2	RDQ21	C
J26	PR24A	2	RDQ21	T
GND	GNDIO2	-		
K29	PR23B	2	RDQ21	C (LVDS)*
K30	PR23A	2	RDQ21	T (LVDS)*
J23	PR22B	2	RDQ21	C
J25	PR22A	2	RDQ21	T
VCCIO	VCCIO2	99		
J27	PR21B	2	RDQ21	C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2	RDQ21	C
GND	GNDIO2	-		
H24	PR20A	2	RDQ21	T
J29	PR19B	2	RDQ21	C (LVDS)*
J30	PR19A	2	RDQ21	T (LVDS)*
H25	PR18B	2	RDQ21	C
VCCIO	VCCIO2	2		
H23	PR18A	2	RDQ21	T
G27	PR15B	2	RUM1_SPLLC_FB_A/RDQ12	C
GND	GNDIO2	-		
H27	PR15A	2	RUM1_SPLLT_FB_A/RDQ12	T
G29	PR14B	2	RUM1_SPLLC_IN_A/RDQ12	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A/RDQ12	T (LVDS)*
VCCIO	VCCIO2	2		
GND	GNDIO2	-		
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
VCCIO	VCCIO2	2		
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO2	-		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
VCCIO	VCCIO2	2		
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO1	-		
C25	PT99B	1		C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D25	PT99A	1		T
J22	PT98B	1		C
J21	PT98A	1		T
VCCIO	VCCIO1	1		
B25	PT97B	1		C
A25	PT97A	1		T
E24	PT96B	1		C
F24	PT96A	1		T
GND	GNDIO1	-		
F23	PT95B	1		C
H22	PT95A	1		T
D24	PT94B	1		C
C24	PT94A	1		T
VCCIO	VCCIO1	1		
E23	PT93B	1		C
G23	PT93A	1		T
B24	PT92B	1		C
A24	PT92A	1		T
C27	PT91B	1		C
GND	GNDIO1	-		
D27	PT91A	1		T
C26	PT90B	1		C
D26	PT90A	1		T
A27	PT89B	1		C
VCCIO	VCCIO1	1		
B27	PT89A	1		T
A28	PT88B	1		C
B28	PT88A	1		T
A29	PT87B	1		C
B29	PT87A	1		T
GND	GNDIO1	-		
VCCIO	VCCIO1	1		
H21	PT80B	1		C
F22	PT80A	1		T
VCCIO	VCCIO1	1		
B23	PT79B	1		C
A23	PT79A	1		T
G24	PT78B	1		C
E22	PT78A	1		T
GND	GNDIO1	-		
D22	PT77B	1		C
C22	PT77A	1		T
G22	PT76B	1		C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R19	GND	-		
R20	GND	-		
T11	GND	-		
T12	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T19	GND	-		
T20	GND	-		
U11	GND	-		
U12	GND	-		
U13	GND	-		
U14	GND	-		
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U19	GND	-		
U20	GND	-		
V12	GND	-		
V13	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V18	GND	-		
V19	GND	-		
V28	GND	-		
V3	GND	-		
W12	GND	-		
W13	GND	-		
W14	GND	-		
W15	GND	-		
W16	GND	-		
W17	GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M19	PR50A	3	RDQ52	T (LVDS)*
M18	PR49B	3	RDQ52	C
VCCIO	VCCIO3	3		
L16	PR49A	3	RDQ52	T
L22	PR48B	3	RDQ52	C (LVDS)*
L21	PR48A	3	RDQ52	T (LVDS)*
GNDIO	GNDIO3	-		
K22	PR46B	3	RLM3_SPLLC_FB_A	C
VCCIO	VCCIO3	3		
K21	PR46A	3	RLM3_SPLLT_FB_A	T
L17	PR45B	3	RLM3_SPLLC_IN_A	C (LVDS)*
L18	PR45A	3	RLM3_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-		
L20	PR44B	3		C
L19	PR44A	3		T
K16	PR43B	3		C (LVDS)*
K17	PR43A	3		T (LVDS)*
VCCIO	VCCIO3	3		
J16	PR42B	3	VREF2_3	C
K18	PR42A	3	VREF1_3	T
J22	PR41B	3	PCLKC3_0	C (LVDS)*
J21	PR41A	3	PCLKT3_0	T (LVDS)*
H22	PR39B	2	PCLKC2_0/RDQ36	C
H21	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-		
J17	PR38B	2	RDQ36	C (LVDS)*
J18	PR38A	2	RDQ36	T (LVDS)*
J20	PR37B	2	RDQ36	C
J19	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2		
H16	PR36B	2	RDQ36	C (LVDS)*
H17	PR36A	2	RDQS36	T (LVDS)*
G22	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-		
G21	PR35A	2	RDQ36	T
H20	PR34B	2	RDQ36	C (LVDS)*
H19	PR34A	2	RDQ36	T (LVDS)*
G16	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2		
H18	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
F22	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C (LVDS)*
F21	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T (LVDS)*
G20	PR30B	2	RDQ27	C

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AC15	PB27B	5	BDQ24	C	PB42B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AD15	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T
AF15	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C
AG10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T
AG9	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C
AH14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T
AG12	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
AG15	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T
AG13	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C
GNDIO	GNDIO5	-			GNDIO5	-		
AF16	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T
AH15	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C
AC16	PB43A	5	VREF2_5/BDQ42	T	PB52A	5	VREF2_5/BDQ51	T
AE16	PB43B	5	VREF1_5/BDQ42	C	PB52B	5	VREF1_5/BDQ51	C
AG11	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T
AF11	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AJ14	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
AK14	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C
AK15	PB50A	4	VREF2_4/BDQ51	T	PB59A	4	VREF2_4/BDQ60	T
AK16	PB50B	4	VREF1_4/BDQ51	C	PB59B	4	VREF1_4/BDQ60	C
AF18	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
GNDIO	GNDIO4	-			GNDIO4	-		
AD16	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AJ15	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AG16	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
AE17	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
AC17	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
AH16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
AK17	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AG20	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
GNDIO	GNDIO4	-			GNDIO4	-		
AG21	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
AG18	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T
AJ16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C
AF21	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T
AG22	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T
AF19	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AH17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
D19	PT93B	1		C
E18	PT93A	1		T
D18	PT92B	1		C
C17	PT92A	1		T
A17	PT91B	1		C
B17	PT91A	1		T
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
J18	PT75B	1		C
J19	PT75A	1		T
H17	PT74B	1		C
J17	PT74A	1		T
F18	PT73B	1		C
F17	PT73A	1		T
GNDIO	GNDIO1	-		
A16	PT72B	1		C
B16	PT72A	1		T
G17	PT71B	1		C
G16	PT71A	1		T
VCCIO	VCCIO1	1		
H16	PT70B	1		C
F16	PT70A	1		T
J16	PT69B	1		C
G15	PT69A	1		T
GNDIO	GNDIO1	-		
C16	PT68B	1		C
D16	PT68A	1		T
J15	PT67B	1		C
H15	PT67A	1		T
VCCIO	VCCIO1	1		
A15	PT66B	1	VREF2_1	C
B15	PT66A	1	VREF1_1	T
F15	PT65B	1	PCLKC1_0	C
E16	PT65A	1	PCLKT1_0	T
C15	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
D15	PT64A	0	PCLKT0_0	T
C14	PT63B	0	VREF2_0	C
E15	PT63A	0	VREF1_0	T
G14	PT62B	0		C
VCCIO	VCCIO0	0		
J14	PT62A	0		T
F14	PT61B	0		C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		