Lattice Semiconductor Corporation - LFE2-12SE-6T144I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	93
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12se-6t144i

IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3[2]	3.135	3.3	3.465	—	—	—
LVCMOS 2.5[2]	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2[2]	1.14	1.2	1.26	—	—	—
LVTTL[2]	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18[2] Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2[2] Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3[2] Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL[2] 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL[2] 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

MLVDS

The LatticeECP2/M devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Multipoint Low Voltage Differential Signaling)

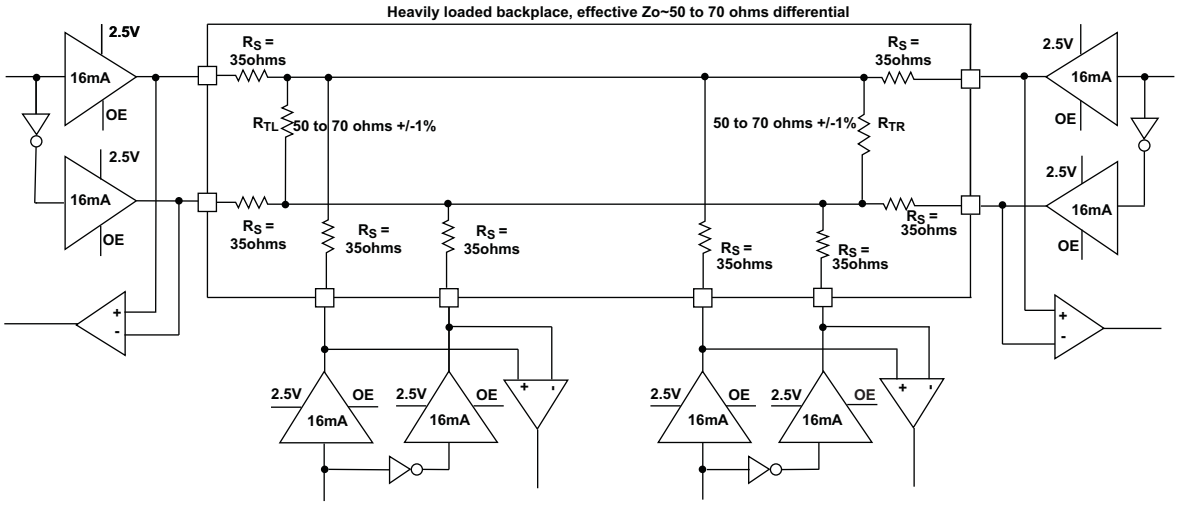

Table 3-6. MLVDS DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

LatticeECP2 Power Supply and NC

Signals	144 TQFP[3]	208 PQFP[3]	256 fpBGA[4]	484 fpBGA[4]
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	**LFE2-6:** G7, G9, G10, H7, J10, K10, K8 **LFE2-12/LFE2-20:** G7, G9, G10, H7, J10, K10, K8	**LFE2-12/LFE2-20:** N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 **LFE2-35/LFE2-50:** J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	**LFE2-12/LFE2-20:** None **LFE2-35:** N6, N18 **LFE2-50:** N6, N18, K6, J16
GND[1]	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC[2]	**LFE2-6:** 45, 46, 124, 127 **LFE2-12:** 127	None	**LFE2-6:** K6, R3, P4 **LFE2-12/LFE2-20:** None	**LFE2-12:** E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-20/LFE2-35:** K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 **LFE2-50:** None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP

LFE2-12E/SE					LFE2-20E/SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
3	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*
4	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*
5	GND	-			GND	-		
6	PL6A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ16	T (LVDS)*
7	VCCAUX	-			VCCAUX	-		
8	PL6B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ16	C (LVDS)*
9	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*
10	VCCIO7	7			VCCIO7	7		
11	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*
12	VCC	-			VCC	-		
13	GND	-			GND	-		
14	VCCIO7	7			VCCIO7	7		
15	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*
16	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*
17	GND	-			GND	-		
18	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T
19	VCC	-			VCC	-		
20	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C
21	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*
22	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
23	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T
24	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C
25	GND	-			GND	-		
26	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
27	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
28	VCC	-			VCC	-		
29	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
30	VCCAUX	-			VCCAUX	-		
31	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
32	GND	-			GND	-		
33	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
34	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*
35	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
36	PL23A	6			PL33A	6	LDQ34	
37	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*
38	VCCIO6	6			VCCIO6	6		
39	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*
40	VCC	-			VCC	-		
41	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*
42	GND	-			GND	-		
43	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*
44	VCCIO6	6			VCCIO6	6		
45	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO6	-			GNDIO6	-		
L2	PL24A	6	LDQ28	T (LVDS)*	PL24A	6	LDQ28	T (LVDS)*
K2	PL25A	6	LDQ28	T	PL25A	6	LDQ28	T
L3	PL24B	6	LDQ28	C (LVDS)*	PL24B	6	LDQ28	C (LVDS)*
K1	PL25B	6	LDQ28	C	PL25B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
L4	PL26A	6	LDQ28	T (LVDS)*	PL26A	6	LDQ28	T (LVDS)*
L1	PL27A	6	LDQ28	T	PL27A	6	LDQ28	T
L5	PL26B	6	LDQ28	C (LVDS)*	PL26B	6	LDQ28	C (LVDS)*
M1	PL27B	6	LDQ28	C	PL27B	6	LDQ28	C
GND	GNDIO6	-			GNDIO6	-		
N1	PL29A	6	LDQ28	T	PL29A	6	LDQ28	T
N2	PL28A	6	LDQS28	T (LVDS)*	PL28A	6	LDQS28	T (LVDS)*
P1	PL29B	6	LDQ28	C	PL29B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL28B	6	LDQ28	C (LVDS)*	PL28B	6	LDQ28	C (LVDS)*
R1	PL30A	6	LDQ28	T (LVDS)*	PL30A	6	LDQ28	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
R2	PL30B	6	LDQ28	C (LVDS)*	PL30B	6	LDQ28	C (LVDS)*
N4	TDI	-			TDI	-		
M4	TCK	-			TCK	-		
P3	TDO	-			TDO	-		
N3	TMS	-			TMS	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
K6	NC	-			PB3A	5	BDQ6	
M6	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
R3	NC	-			PB5A	5	BDQ6	T
P4	NC	-			PB5B	5	BDQ6	C
-	-	-			VCCIO	5		
-	-	-			GNDIO5	5		
N5	PB3A	5	BDQ6	T	PB21A	5	BDQ24	T
N6	PB3B	5	BDQ6	C	PB21B	5	BDQ24	C
T2	PB4A	5	BDQ6	T	PB22A	5	BDQ24	T
P6	PB5A	5	BDQ6	T	PB23A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB4B	5	BDQ6	C	PB22B	5	BDQ24	C
R6	PB5B	5	BDQ6	C	PB23B	5	BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
R4	PB6A	5	BDQS6	T	PB24A	5	BDQS24	T
L6	PB7A	5	BDQ6	T	PB25A	5	BDQ24	T
T4	PB6B	5	BDQ6	C	PB24B	5	BDQ24	C
L7	PB7B	5	BDQ6	C	PB25B	5	BDQ24	C
N7	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A6	PT21A	0		T	PT30A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
C7	PT17B	0		C	PT26B	0		C
D10	PT18B	0		C	PT27B	0		C
C6	PT17A	0		T	PT26A	0		T
E10	PT18A	0		T	PT27A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F10	PT15B	0		C	PT24B	0		C
B6	PT16B	0		C	PT25B	0		C
D9	PT15A	0		T	PT24A	0		T
B5	PT16A	0		T	PT25A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
A5	PT13B	0		C	PT22B	0		C
F9	PT14B	0		C	PT23B	0		C
A4	PT13A	0		T	PT22A	0		T
E9	PT14A	0		T	PT23A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
G8	PT11B	0		C	PT20B	0		C
A3	PT12B	0		C	PT21B	0		C
E8	PT11A	0		T	PT20A	0		T
A2	PT12A	0		T	PT21A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
-	-	-			VCCIO0	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
-	-	-			GNDIO0	-		
E7	PT8B	0		C	PT8B	0		C
F8	PT9B	0		C	PT9B	0		C
F7	PT8A	0		T	PT8A	0		T
D7	PT9A	0		T	PT9A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D4	PT6B	0		C	PT6B	0		C
D5	PT7B	0		C	PT7B	0		C
C4	PT6A	0		T	PT6A	0		T
D6	PT7A	0		T	PT7A	0		T
GNDIO	GNDIO0	-			GNDIO	-		
J7	PT4B	0		C	PT4B	0		C
B2	PT5B	0		C	PT5B	0		C
H7	PT4A	0		T	PT4A	0		T
B1	PT5A	0		T	PT5A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
D3	PT3B	0		C	PT3B	0		C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C2	PT3A	0		T	PT3A	0		T
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
G10	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
H8	VCCIO0	0			VCCIO0	0		
G11	VCCIO1	1			VCCIO1	1		
G12	VCCIO1	1			VCCIO1	1		
G13	VCCIO1	1			VCCIO1	1		
G14	VCCIO1	1			VCCIO1	1		
H14	VCCIO2	2			VCCIO2	2		
H15	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K16	VCCIO2	2			VCCIO2	2		
L16	VCCIO3	3			VCCIO3	3		
M16	VCCIO3	3			VCCIO3	3		
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AH24	PB89A	4	BDQ87	T
AH25	PB89B	4	BDQ87	C
VCCIO	VCCIO4	4		
AJ26	PB90A	4	BDQ87	T
AK26	PB90B	4	BDQ87	C
AF25	PB91A	4	BDQ87	T
AG25	PB91B	4	BDQ87	C
GND	GNDIO4	-		
AK22	PB92A	4	BDQ96	T
AJ22	PB92B	4	BDQ96	C
AE22	PB93A	4	BDQ96	T
AF22	PB93B	4	BDQ96	C
AG22	PB94A	4	BDQ96	T
VCCIO	VCCIO4	4		
AH22	PB94B	4	BDQ96	C
AG24	PB95A	4	BDQ96	T
AG23	PB95B	4	BDQ96	C
AE23	PB96A	4	BDQS96	
GND	GNDIO4	-		
AC22	PB97A	4	BDQ96	
AJ23	PB98A	4	BDQ96	T
VCCIO	VCCIO4	4		
AK23	PB98B	4	BDQ96	C
AD24	PB99A	4	BDQ96	T
AF24	PB99B	4	BDQ96	C
AC23	PB100A	4	VREF2_4/BDQ96	T
GND	GNDIO4	-		
AE24	PB100B	4	VREF1_4/BDQ96	C
AE25	CFG2	8		
AB22	CFG1	8		
AE26	CFG0	8		
AA22	PROGRAMN	8		
AD25	CCLK	8		
AD26	INITN	8		
AC24	DONE	8		
GND	GNDIO4	-		
AC25	PR90B	8	WRITEN	C
AE27	PR90A	8	CS1N	T
AC26	PR89B	8	CSN	C
AE28	PR89A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8		
AD27	PR88B	8	D1	C
AD28	PR88A	8	D2	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
P25	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2		
P23	PR51A	2	RDQ54	T
P27	PR50B	2	RDQ54	C (LVDS)*
P28	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-		
VCCIO	VCCIO2	2		
N24	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
N26	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
N23	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
N25	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2		
P29	PR37B	2	RDQ37	C (LVDS)*
P30	PR37A	2	RDQS37	T (LVDS)*
M26	PR36B	2	RDQ37	C
GND	GNDIO2	-		
M24	PR36A	2	RDQ37	T
N29	PR35B	2	RDQ37	C (LVDS)*
N30	PR35A	2	RDQ37	T (LVDS)*
M25	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2		
M23	PR34A	2	RDQ37	T
M27	PR33B	2	RDQ37	C (LVDS)*
M28	PR33A	2	RDQ37	T (LVDS)*
L26	PR32B	2	RDQ29	C
GND	GNDIO2	-		
L24	PR32A	2	RDQ29	T
M29	PR31B	2	RDQ29	C (LVDS)*
M30	PR31A	2	RDQ29	T (LVDS)*
L25	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2		
L23	PR30A	2	RDQ29	T
L27	PR29B	2	RDQ29	C (LVDS)*
L28	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-		
K24	PR28B	2	RDQ29	C
K26	PR28A	2	RDQ29	T
L29	PR27B	2	RDQ29	C (LVDS)*
L30	PR27A	2	RDQ29	T (LVDS)*
VCCIO	VCCIO2	2		
K23	PR26B	2	RDQ29	C
K25	PR26A	2	RDQ29	T
K27	PR25B	2	RDQ29	C (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
K28	PR25A	2	RDQ29	T (LVDS)*
J24	PR24B	2	RDQ21	C
J26	PR24A	2	RDQ21	T
GND	GNDIO2	-		
K29	PR23B	2	RDQ21	C (LVDS)*
K30	PR23A	2	RDQ21	T (LVDS)*
J23	PR22B	2	RDQ21	C
J25	PR22A	2	RDQ21	T
VCCIO	VCCIO2	99		
J27	PR21B	2	RDQ21	C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2	RDQ21	C
GND	GNDIO2	-		
H24	PR20A	2	RDQ21	T
J29	PR19B	2	RDQ21	C (LVDS)*
J30	PR19A	2	RDQ21	T (LVDS)*
H25	PR18B	2	RDQ21	C
VCCIO	VCCIO2	2		
H23	PR18A	2	RDQ21	T
G27	PR15B	2	RUM1_SPLLC_FB_A/RDQ12	C
GND	GNDIO2	-		
H27	PR15A	2	RUM1_SPLLT_FB_A/RDQ12	T
G29	PR14B	2	RUM1_SPLLC_IN_A/RDQ12	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A/RDQ12	T (LVDS)*
VCCIO	VCCIO2	2		
GND	GNDIO2	-		
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
VCCIO	VCCIO2	2		
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO2	-		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
VCCIO	VCCIO2	2		
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO1	-		
C25	PT99B	1		C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
U10	VCCIO6	6		
U9	VCCIO6	6		
V10	VCCIO6	6		
W10	VCCIO6	6		
W9	VCCIO6	6		
Y9	VCCIO6	6		
L10	VCCIO7	7		
L9	VCCIO7	7		
M10	VCCIO7	7		
N10	VCCIO7	7		
P10	VCCIO7	7		
R10	VCCIO7	7		
AA21	VCCIO8	8		
Y21	VCCIO8	8		
AA15	VCCAUX	-		
AB11	VCCAUX	-		
AB19	VCCAUX	-		
AB20	VCCAUX	-		
J11	VCCAUX	-		
J12	VCCAUX	-		
J19	VCCAUX	-		
K19	VCCAUX	-		
L22	VCCAUX	-		
M9	VCCAUX	-		
N9	VCCAUX	-		
P21	VCCAUX	-		
P9	VCCAUX	-		
T10	VCCAUX	-		
T21	VCCAUX	-		
V9	VCCAUX	-		
W22	VCCAUX	-		
A1	GND	-		
A30	GND	-		
AC28	GND	-		
AC3	GND	-		
AH13	GND	-		
AH18	GND	-		
AH23	GND	-		
AH28	GND	-		
AH3	GND	-		
AH8	GND	-		
AK1	GND	-		
AK30	GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
W19	NC	-		
W18	NC	-		
V17	NC	-		
V18	NC	-		
D15	NC	-		
G14	NC	-		
G15	NC	-		
D14	NC	-		
E15	NC	-		
E14	NC	-		
F15	NC	-		
F14	NC	-		
F13	NC	-		
G12	NC	-		
G13	NC	-		
H8	VCCPLL	-		
H15	VCCPLL	-		
R8	VCCPLL	-		
R15	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N23	PR37A	3	PCLKT3_0	T (LVDS)*	PR41A	3	PCLKT3_0	T*
N24	PR35B	2	PCLKC2_0/RDQ32	C	PR39B	2	PCLKC2_0/RDQ36	C
N25	PR35A	2	PCLKT2_0/RDQ32	T	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-			GNDIO2	-		
M22	PR34B	2	RDQ32	C (LVDS)*	PR38B	2	RDQ36	C*
M24	PR34A	2	RDQ32	T (LVDS)*	PR38A	2	RDQ36	T*
M23	PR33B	2	RDQ32	C	PR37B	2	RDQ36	C
N26	PR33A	2	RDQ32	T	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2			VCCIO2	2		
L22	PR32B	2	RDQ32	C (LVDS)*	PR36B	2	RDQ36	C*
L24	PR32A	2	RDQS32	T (LVDS)*	PR36A	2	RDQS36	T*
L23	PR31B	2	RDQ32	C	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-			GNDIO2	-		
M20	PR31A	2	RDQ32	T	PR35A	2	RDQ36	T
M26	PR30B	2	RDQ32	C (LVDS)*	PR34B	2	RDQ36	C*
L26	PR30A	2	RDQ32	T (LVDS)*	PR34A	2	RDQ36	T*
K22	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2			VCCIO2	2		
M19	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
K25	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C*
K26	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T*
K24	PR26B	2	RDQ23	C	PR30B	2	RDQ27	C
K23	PR26A	2	RDQ23	T	PR30A	2	RDQ27	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR25B	2	RDQ23	C (LVDS)*	PR29B	2	RDQ27	C*
K21	PR25A	2	RDQ23	T (LVDS)*	PR29A	2	RDQ27	T*
J23	PR24B	2	RDQ23	C	PR28B	2	RDQ27	C
J24	PR24A	2	RDQ23	T	PR28A	2	RDQ27	T
VCCIO	VCCIO2	2			VCCIO2	2		
K20	PR23B	2	RDQ23	C (LVDS)*	PR27B	2	RDQ27	C*
J21	PR23A	2	RDQS23	T (LVDS)*	PR27A	2	RDQS27	T*
H21	PR22B	2	RDQ23	C	PR26B	2	RDQ27	C
GNDIO	GNDIO2	-			GNDIO2	-		
K18	PR22A	2	RDQ23	T	PR26A	2	RDQ27	T
H22	PR21B	2	RDQ23	C (LVDS)*	PR25B	2	RDQ27	C*
J20	PR21A	2	RDQ23	T (LVDS)*	PR25A	2	RDQ27	T*
J25	PR20B	2	RDQ23	C	PR24B	2	RDQ27	C
VCCIO	VCCIO2	2			VCCIO2	2		
J26	PR20A	2	RDQ23	T	PR24A	2	RDQ27	T
G21	PR19B	2	RDQ23	C (LVDS)*	PR23B	2	RDQ27	C*
J19	PR19A	2	RDQ23	T (LVDS)*	PR23A	2	RDQ27	T*
GNDIO	GNDIO2	-			GNDIO2	-		
H23	PR18B	2	RDQ15	C	PR21B	2		C
H24	PR18A	2	RDQ15	T	PR21A	2		T
H25	PR17B	2	RDQ15	C (LVDS)*	PR20B	2		C*
H26	PR17A	2	RDQ15	T (LVDS)*	PR20A	2		T*
VCCIO	VCCIO2	2			VCCIO2	2		
G22	PR16B	2	RDQ15	C	PR19B	2		C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
GNDIO	GNDIO2	-		
M27	PR47B	2	RDQ45	C (LVDS)*
M28	PR47A	2	RDQ45	T (LVDS)*
H30	PR46B	2	RDQ45	C
G30	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2		
M25	PR45B	2	RDQ45	C (LVDS)*
M26	PR45A	2	RDQS45	T (LVDS)*
L30	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-		
L29	PR44A	2	RDQ45	T
L28	PR43B	2	RDQ45	C (LVDS)*
L27	PR43A	2	RDQ45	T (LVDS)*
H29	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2		
G29	PR42A	2	RDQ45	T
L22	PR41B	2	RDQ45	C (LVDS)*
M22	PR41A	2	RDQ45	T (LVDS)*
F30	PR40B	2		C
GNDIO	GNDIO2	-		
F29	PR40A	2		T
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E30	PR34B	2	RDQ32	C (LVDS)*
E29	PR34A	2	RDQ32	T (LVDS)*
-	-	-		
L25	PR33B	2	RDQ32	C
L26	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2		
H28	PR32B	2	RDQ32	C (LVDS)*
J28	PR32A	2	RDQS32	T (LVDS)*
G28	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-		
G27	PR31A	2	RDQ32	T
L24	PR30B	2	RDQ32	C (LVDS)*
L23	PR30A	2	RDQ32	T (LVDS)*
D30	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2		
D29	PR29A	2	RDQ32	T
K24	PR28B	2	RDQ32	C (LVDS)*
K25	PR28A	2	RDQ32	T (LVDS)*
J27	PR26B	2	RDQ23	C
GNDIO	GNDIO2	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AN29	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AM28	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AL27	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AM29	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AL29	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AL30	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AK30	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AK29	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AM30	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AL31	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AM31	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AN30	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AP30	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T
AL32	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AP31	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AN31	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AP32	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AM34	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AP33	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AN32	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AM32	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AN34	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AM33	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AN33	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AH28	CFG2	8			CFG2	8		
AD24	CFG1	8			CFG1	8		
AJ29	CFG0	8			CFG0	8		
AF25	PROGRAMN	8			PROGRAMN	8		
AJ28	CCLK	8			CCLK	8		
AE25	INITN	8			INITN	8		
AK31	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE24	WRITEN***	8			WRITEN***	8		
AJ30	CS1N***	8			CS1N***	8		
AD25	CSN***	8			CSN***	8		
AG29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG28	D1***	8			D1***	8		
AG30	D2***	8			D2***	8		
AH29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF26	D4***	8			D4***	8		
AH30	D5***	8			D5***	8		
AE26	D6***	8			D6***	8		
AJ31	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG27	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AK32	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8		
AK33	BUSY/SISPI***	8			BUSY/SISPI***	8		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E4	NC	-			NC	-		
E9	NC	-			NC	-		
F10	NC	-			NC	-		
F25	NC	-			NC	-		
F26	NC	-			NC	-		
F27	NC	-			NC	-		
F28	NC	-			NC	-		
F29	NC	-			NC	-		
F30	NC	-			NC	-		
F31	NC	-			NC	-		
F32	NC	-			NC	-		
F33	NC	-			NC	-		
F34	NC	-			NC	-		
F5	NC	-			NC	-		
F6	NC	-			NC	-		
F7	NC	-			NC	-		
F8	NC	-			NC	-		
F9	NC	-			NC	-		
G10	NC	-			NC	-		
G11	NC	-			NC	-		
G24	NC	-			NC	-		
G25	NC	-			NC	-		
G26	NC	-			NC	-		
G27	NC	-			NC	-		
G28	NC	-			NC	-		
G29	NC	-			NC	-		
G30	NC	-			NC	-		
G33	NC	-			NC	-		
G34	NC	-			NC	-		
G7	NC	-			NC	-		
G8	NC	-			NC	-		
G9	NC	-			NC	-		
H10	NC	-			NC	-		
H11	NC	-			NC	-		
H24	NC	-			NC	-		
H25	NC	-			NC	-		
H26	NC	-			NC	-		
H27	NC	-			NC	-		
H28	NC	-			NC	-		
H29	NC	-			NC	-		
H8	NC	-			NC	-		
H9	NC	-			NC	-		
J10	NC	-			NC	-		
J11	NC	-			NC	-		
J24	NC	-			NC	-		
J25	NC	-			NC	-		
J26	NC	-			NC	-		
J9	NC	-			NC	-		
K10	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484C	331	1.2V	-5	fpBGA	484	COM	35
LFE2-35E-6F484C	331	1.2V	-6	fpBGA	484	COM	35
LFE2-35E-7F484C	331	1.2V	-7	fpBGA	484	COM	35
LFE2-35E-5F672C	450	1.2V	-5	fpBGA	672	COM	35
LFE2-35E-6F672C	450	1.2V	-6	fpBGA	672	COM	35
LFE2-35E-7F672C	450	1.2V	-7	fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484C	339	1.2V	-5	fpBGA	484	COM	50
LFE2-50E-6F484C	339	1.2V	-6	fpBGA	484	COM	50
LFE2-50E-7F484C	339	1.2V	-7	fpBGA	484	COM	50
LFE2-50E-5F672C	500	1.2V	-5	fpBGA	672	COM	50
LFE2-50E-6F672C	500	1.2V	-6	fpBGA	672	COM	50
LFE2-50E-7F672C	500	1.2V	-7	fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672C	500	1.2V	-5	fpBGA	672	COM	70
LFE2-70E-6F672C	500	1.2V	-6	fpBGA	672	COM	70
LFE2-70E-7F672C	500	1.2V	-7	fpBGA	672	COM	70
LFE2-70E-5F900C	583	1.2V	-5	fpBGA	900	COM	70
LFE2-70E-6F900C	583	1.2V	-6	fpBGA	900	COM	70
LFE2-70E-7F900C	583	1.2V	-7	fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144I	90	1.2V	-5	TQFP	144	IND	6
LFE2-6E-6T144I	90	1.2V	-6	TQFP	144	IND	6
LFE2-6E-5F256I	190	1.2V	-5	fpBGA	256	IND	6
LFE2-6E-6F256I	190	1.2V	-6	fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144I	93	1.2V	-5	TQFP	144	IND	12
LFE2-12E-6T144I	93	1.2V	-6	TQFP	144	IND	12
LFE2-12E-5Q208I	131	1.2V	-5	PQFP	208	IND	12
LFE2-12E-6Q208I	131	1.2V	-6	PQFP	208	IND	12
LFE2-12E-5F256I	193	1.2V	-5	fpBGA	256	IND	12
LFE2-12E-6F256I	193	1.2V	-6	fpBGA	256	IND	12
LFE2-12E-5F484I	297	1.2V	-5	fpBGA	484	IND	12
LFE2-12E-6F484I	297	1.2V	-6	fpBGA	484	IND	12

Date	Version	Section	Change Summary
June 2013 (cont.)	04.0 (cont.)	DC and Switching Characteristics	sysCLOCK SPLL Timing table – Corrected signal names for t_{RST} parameter.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added t_{SUMCDI} and t_{HMCDI} parameters.
September 2013	04.1	Architecture	Updated Selectable Master Clock (CCLK) Frequencies during Configuration table.
		DC and Switching Characteristics	Added information on f_{MAXSPI} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.