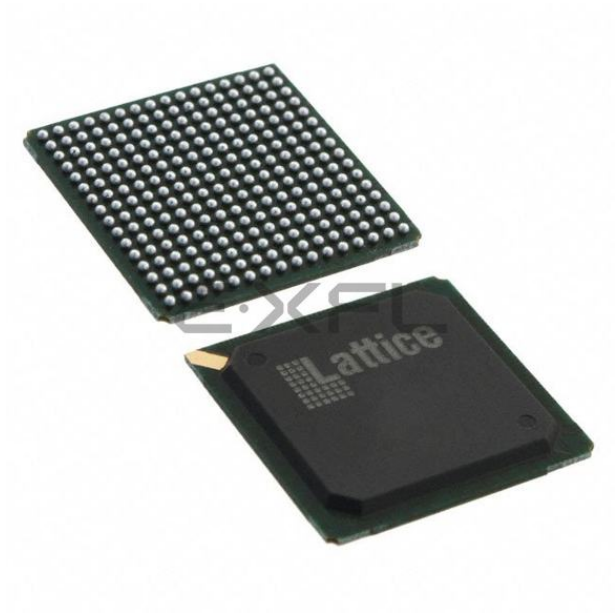
Lattice Semiconductor Corporation - LFE2-12SE-7FN256C Datasheet



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Applications of Embedded - FPGAs

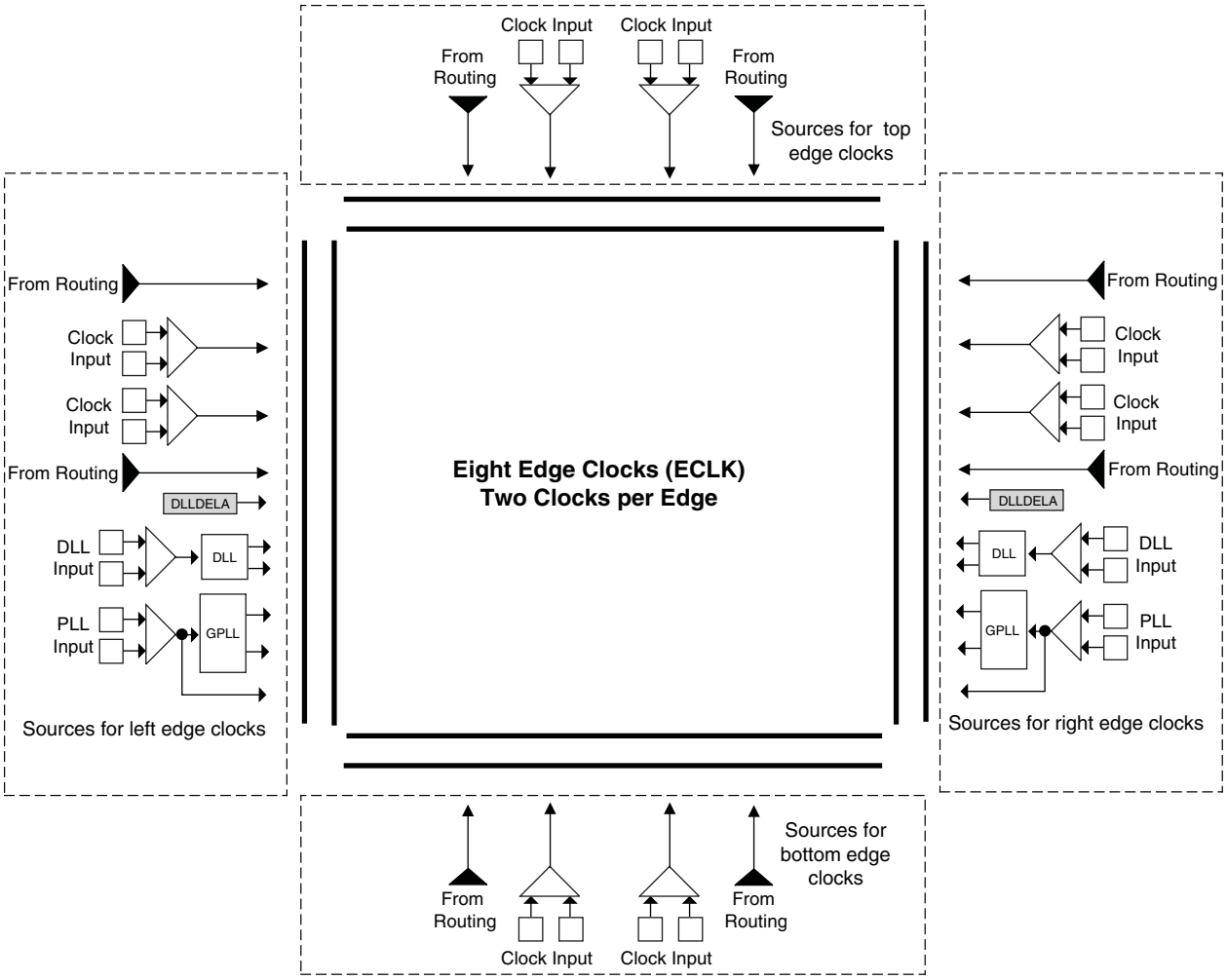
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	226304
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-12se-7fn256c

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

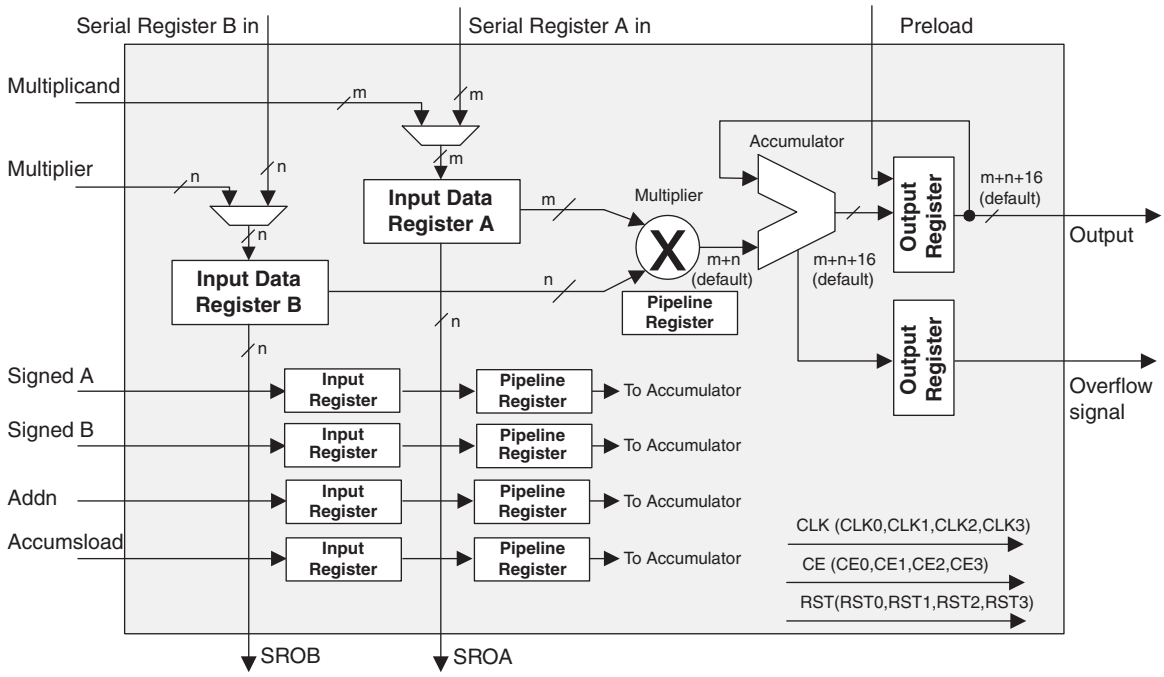
Figure 2-12. Edge Clock Sources



MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in the LatticeECP2/M family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-24 shows the MAC sysDSP element.

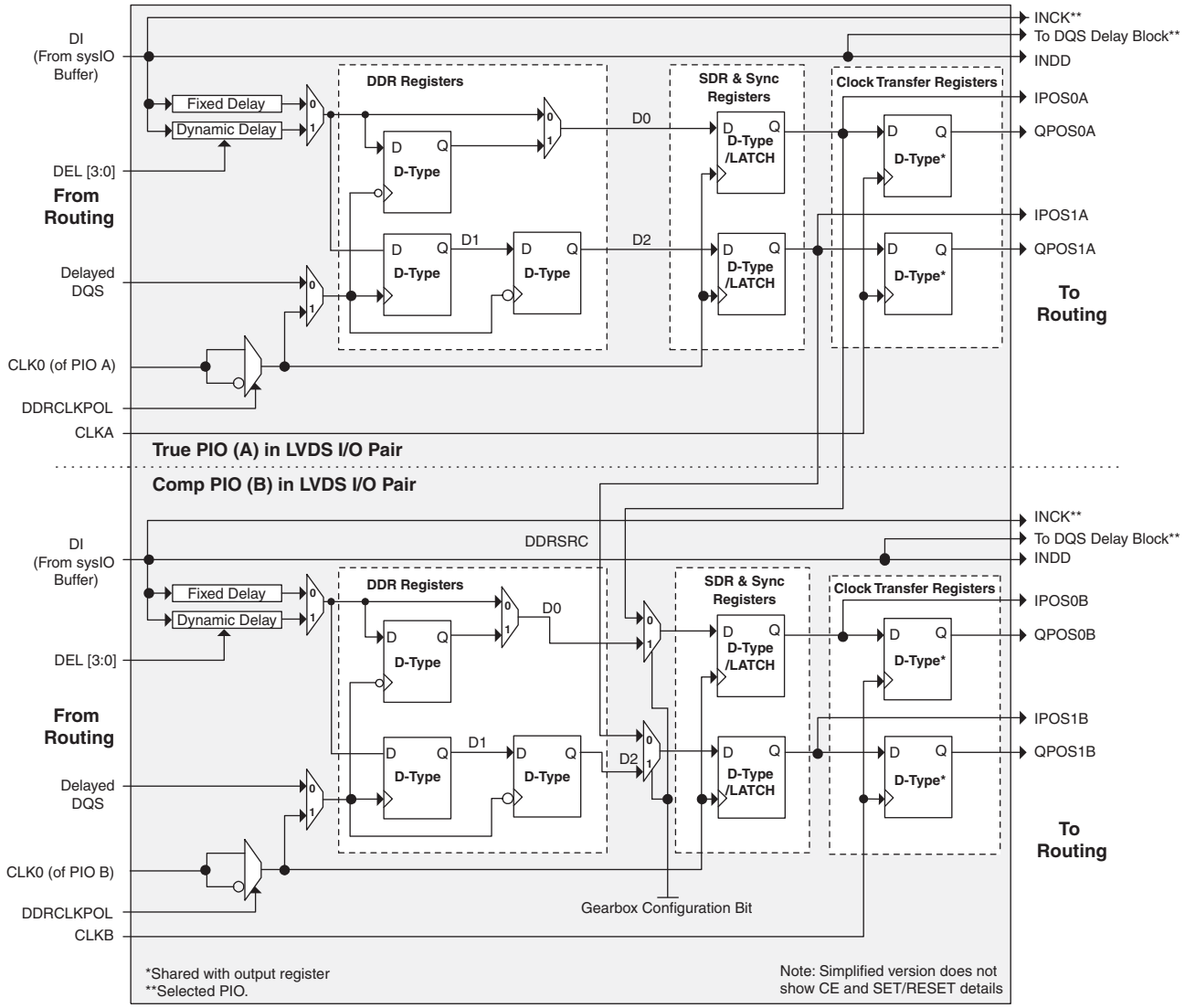
Figure 2-24. MAC sysDSP



By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

Figure 2-29. Input Register Block for Left, Right and Bottom Edges



LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps)[5]									
$t_{SUXGMII}$	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t_{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
$t_{DVBCKXGMII}$	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
$t_{DVACKXGMII}$	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f_{MAX_EDGE}[7]	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to TN1159, LatticeECP2/M Pin Assignment Recommendations for best performance.

Figure 3-7. DDR and DDR2 Parameters

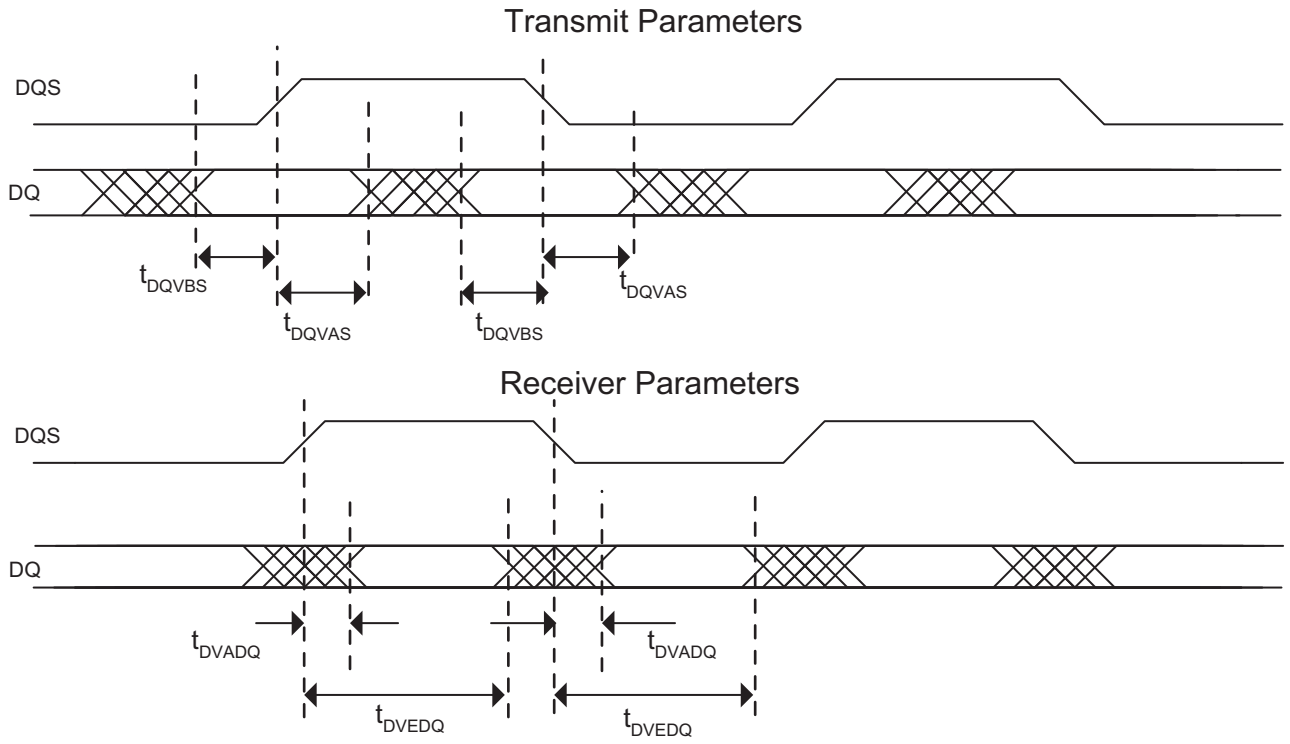
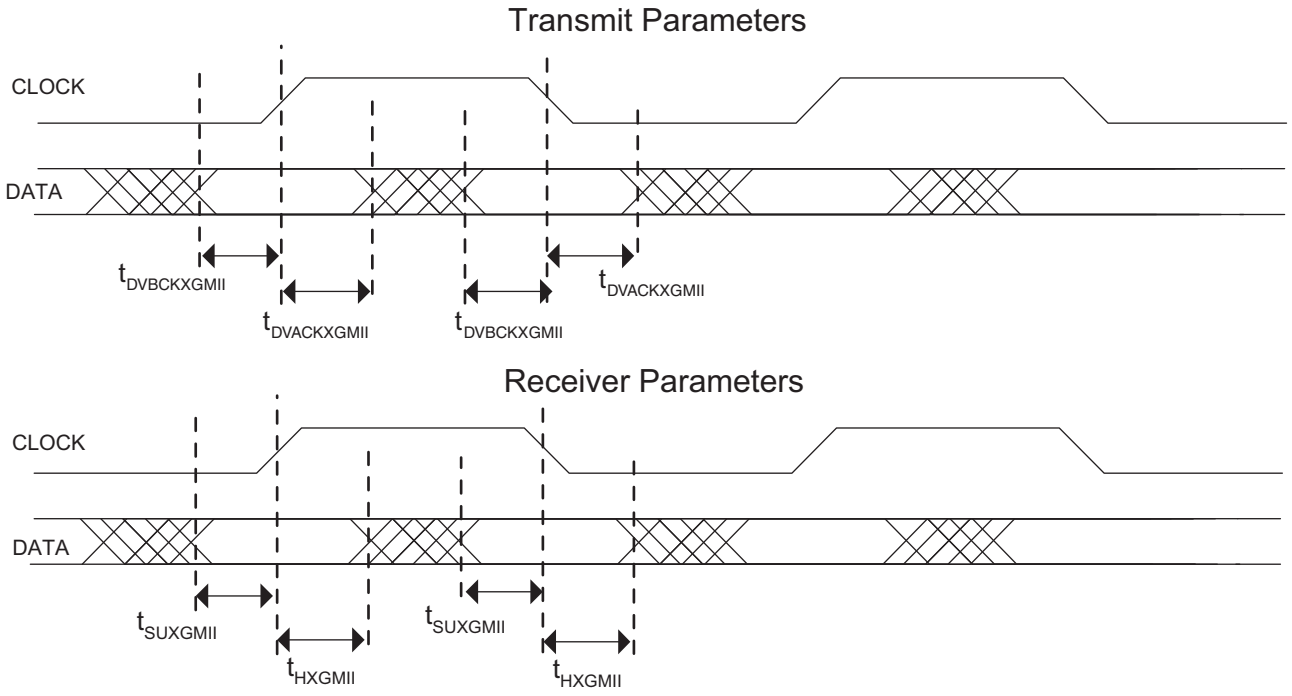


Figure 3-8. XGMII Parameters



LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
92	PB44A	4	BDQ42	T	PB54A	4	BDQ51	T
93	VCCIO4	4			VCCIO4	4		
94	PB44B	4	BDQ42	C	PB54B	4	BDQ51	C
95	PB48A	4	BDQ51	T	PB58A	4	BDQ60	T
96	PB48B	4	BDQ51	C	PB58B	4	BDQ60	C
97	VCC	-			VCC	-		
98	PB52A	4	BDQ51	T	PB60A	4	BDQS60	T
99	PB52B	4	BDQ51	C	PB60B	4	BDQ60	C
100	VCCIO4	4			VCCIO4	4		
101	PB54A	4	BDQ51		PB63A	4	BDQ60	
102	GND	-			GND	-		
103	PB55A	4	VREF2_4/BDQ51	T	PB64A	4	VREF2_4/BDQ60	T
104	PB55B	4	VREF1_4/BDQ51	C	PB64B	4	VREF1_4/BDQ60	C
105	CFG1	8			CFG1	8		
106	PROGRAMN	8			PROGRAMN	8		
107	CFG2	8			CFG2	8		
108	INITN	8			INITN	8		
109	CFG0	8			CFG0	8		
110	CCLK	8			CCLK	8		
111	DONE	8			DONE	8		
112	PR29A	8	D0/SPIFASTN		PR43A	8	D0/SPIFASTN	
113	VCCIO8	8			VCCIO8	8		
114	PR26A	8	D6		PR40A	8	D6	
115	GND	-			GND	-		
116	VCC	-			VCC	-		
117	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
118	VCCIO8	8			VCCIO8	8		
119	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
120	PR24B	8	DOUT/CSON	C	PR38B	8	DOUT/CSON	C
121	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
122	GND	-			GND	-		
123	VCCIO3	3			VCCIO3	3		
124	PR21A	3	RLM0_GPLLT_FB_A		PR31A	3	RLM0_GPLLT_FB_A/RDQ34	
125	VCCAUX	-			VCCAUX	-		
126	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
127	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
128	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
129	VCC	-			VCC	-		
130	PR18B	3	RLM0_GDLLC_FB_A	C	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
131	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
132	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
133	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
134	PR16B	3	VREF2_3	C	PR22B	3	VREF2_3/RDQ25	C
135	VCCIO3	3			VCCIO3	3		
136	PR16A	3	VREF1_3	T	PR22A	3	VREF1_3/RDQ25	T
137	PR15B	3	PCLKC3_0	C (LVDS)*	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T
GNDIO	GNDIO4	-			GNDIO4	-		
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO	4		
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
VCCIO	VCCIO7	7		
F4	PL2A	7	VREF2_7	T (LVDS)*
F3	PL2B	7	VREF1_7	C (LVDS)*
H4	PL3A	7		T
G5	PL3B	7		C
GND	GNDIO7	-		
D2	PL4A	7		T (LVDS)*
D1	PL4B	7		C (LVDS)*
E2	PL5A	7		T
VCCIO	VCCIO7	7		
E1	PL5B	7		C
GND	GNDIO7	-		
VCCIO	VCCIO7	7		
F1	PL14A	7	LUM1_SPLLT_IN_A/LDQ12	T (LVDS)*
F2	PL14B	7	LUM1_SPLLC_IN_A/LDQ12	C (LVDS)*
G1	PL15A	7	LUM1_SPLLT_FB_A/LDQ12	T
G2	PL15B	7	LUM1_SPLLC_FB_A/LDQ12	C
GND	GNDIO7	-		
H8	PL18A	7	LDQ21	T
H6	PL18B	7	LDQ21	C
VCCIO	VCCIO7	7		
G4	PL19A	7	LDQ21	T (LVDS)*
G3	PL19B	7	LDQ21	C (LVDS)*
H7	PL20A	7	LDQ21	T
H5	PL20B	7	LDQ21	C
GND	GNDIO7	-		
H2	PL21A	7	LDQS21	T (LVDS)*
H1	PL21B	7	LDQ21	C (LVDS)*
J6	PL22A	7	LDQ21	T
VCCIO	VCCIO7	7		
J8	PL22B	7	LDQ21	C
J2	PL23A	7	LDQ21	T (LVDS)*
J1	PL23B	7	LDQ21	C (LVDS)*
J5	PL24A	7	LDQ21	T
GND	GNDIO7	-		
J7	PL24B	7	LDQ21	C
J4	PL25A	7	LDQ29	T (LVDS)*
J3	PL25B	7	LDQ29	C (LVDS)*
K6	PL26A	7	LDQ29	T
K8	PL26B	7	LDQ29	C
VCCIO	VCCIO7	7		
K2	PL27A	7	LDQ29	T (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
G12	PT40B	0		C
E12	PT40A	0		T
VCCIO	VCCIO0	0		
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO0	-		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
VCCIO	VCCIO0	0		
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO0	-		
A11	PT32A	0		T
E10	PT31B	0		C
VCCIO	VCCIO0	0		
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO0	-		
VCCIO	VCCIO0	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO0	-		
D7	PT14A	0		T
D8	PT13B	0		C
VCCIO	VCCIO0	0		
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			-	-		
F16	XRES	-			XRES	-		
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F11	VCCIO0	0			VCCIO0	0		
J13	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	1		
D18	VCCIO1	1			VCCIO1	1		
F16	VCCIO1	1			VCCIO1	1		
J14	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
G25	VCCIO2	2			VCCIO2	2		
L21	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M25	VCCIO2	2			VCCIO2	2		
N18	VCCIO2	2			VCCIO2	2		
P18	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R25	VCCIO3	3			VCCIO3	3		
T21	VCCIO3	3			VCCIO3	3		
Y25	VCCIO3	3			VCCIO3	3		
AA16	VCCIO4	4			VCCIO4	4		
AC18	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V14	VCCIO4	4			VCCIO4	4		
AA11	VCCIO5	5			VCCIO5	5		
V13	VCCIO5	5			VCCIO5	5		
AE12	VCCIO5	5			VCCIO5	5		
AE7	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
P9	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R2	VCCIO6	6			VCCIO6	6		
T6	VCCIO6	6			VCCIO6	6		
Y2	VCCIO6	6			VCCIO6	6		
G2	VCCIO7	7			VCCIO7	7		
L6	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M2	VCCIO7	7			VCCIO7	7		
N9	VCCIO7	7			VCCIO7	7		
AC24	VCCIO8	8			VCCIO8	8		
U17	VCCIO8	8			VCCIO8	8		
J11	VCCAUX	-			VCCAUX	-		
J12	VCCAUX	-			VCCAUX	-		
J15	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
M18	VCCAUX	-			VCCAUX	-		
M9	VCCAUX	-			VCCAUX	-		
R18	VCCAUX	-			VCCAUX	-		
R9	VCCAUX	-			VCCAUX	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
T29	PR48B	3	RDQ52	C (LVDS)*	PR60B	3	RDQ64	C (LVDS)*
T28	PR48A	3	RDQ52	T (LVDS)*	PR60A	3	RDQ64	T (LVDS)*
R23	PR46B	3	RLM3_SPLLC_FB_A	C	PR58B	3	RLM3_SPLLC_FB_A/RDQ55	C
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			-	-		
R22	PR46A	3	RLM3_SPLLT_FB_A	T	PR58A	3	RLM3_SPLLT_FB_A/RDQ55	T
P30	PR45B	3	RLM3_SPLLC_IN_A	C (LVDS)*	PR57B	3	RLM3_SPLLC_IN_A/RDQ55	C (LVDS)*
R29	PR45A	3	RLM3_SPLLT_IN_A	T (LVDS)*	PR57A	3	RLM3_SPLLT_IN_A/RDQ55	T (LVDS)*
T27	PR44B	3		C	PR56B	3	RDQ55	C
-	-	-			VCCIO3	3		
T26	PR44A	3		T	PR56A	3	RDQ55	T
GNDIO	GNDIO3	-			GNDIO3	-		
N30	PR43B	3		C (LVDS)*	PR53B	3	RDQ55	C (LVDS)*
N29	PR43A	3		T (LVDS)*	PR53A	3	RDQ55	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
R27	PR42B	3	VREF2_3	C	PR52B	3	VREF2_3/RDQ55	C
R28	PR42A	3	VREF1_3	T	PR52A	3	VREF1_3/RDQ55	T
P29	PR41B	3	PCLKC3_0	C (LVDS)*	PR51B	3	PCLKC3_0/RDQ55	C (LVDS)*
P28	PR41A	3	PCLKT3_0	T (LVDS)*	PR51A	3	PCLKT3_0/RDQ55	T (LVDS)*
M30	PR39B	2	PCLKC2_0/RDQ36	C	PR49B	2	PCLKC2_0/RDQ46	C
M29	PR39A	2	PCLKT2_0/RDQ36	T	PR49A	2	PCLKT2_0/RDQ46	T
GNDIO	GNDIO2	-			GNDIO2	-		
P23	PR38B	2	RDQ36	C (LVDS)*	PR48B	2	RDQ46	C (LVDS)*
P24	PR38A	2	RDQ36	T (LVDS)*	PR48A	2	RDQ46	T (LVDS)*
R26	PR37B	2	RDQ36	C	PR47B	2	RDQ46	C
P27	PR37A	2	RDQ36	T	PR47A	2	RDQ46	T
VCCIO	VCCIO2	2			VCCIO2	2		
P25	PR36B	2	RDQ36	C (LVDS)*	PR46B	2	RDQ46	C (LVDS)*
P26	PR36A	2	RDQS36	T (LVDS)*	PR46A	2	RDQS46	T (LVDS)*
K30	PR35B	2	RDQ36	C	PR45B	2	RDQ46	C
GNDIO	GNDIO2	-			GNDIO2	-		
K29	PR35A	2	RDQ36	T	PR45A	2	RDQ46	T
N22	PR34B	2	RDQ36	C (LVDS)*	PR44B	2	RDQ46	C (LVDS)*
P22	PR34A	2	RDQ36	T (LVDS)*	PR44A	2	RDQ46	T (LVDS)*
J30	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C	PR43B	2	RUM3_SPLLC_FB_A/RDQ46	C
VCCIO	VCCIO2	2			VCCIO2	2		
J29	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T	PR43A	2	RUM3_SPLLT_FB_A/RDQ46	T
N24	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C (LVDS)*	PR42B	2	RUM3_SPLLC_IN_A/RDQ46	C (LVDS)*
N23	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T (LVDS)*	PR42A	2	RUM3_SPLLT_IN_A/RDQ46	T (LVDS)*
N25	PR30B	2	RDQ27	C	PR40B	2	RDQ37	C
N26	PR30A	2	RDQ27	T	PR40A	2	RDQ37	T
GNDIO	GNDIO2	-			GNDIO2	-		
M27	PR29B	2	RDQ27	C (LVDS)*	PR39B	2	RDQ37	C (LVDS)*
M28	PR29A	2	RDQ27	T (LVDS)*	PR39A	2	RDQ37	T (LVDS)*
H30	PR28B	2	RDQ27	C	PR38B	2	RDQ37	C
G30	PR28A	2	RDQ27	T	PR38A	2	RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
M25	PR27B	2	RDQ27	C (LVDS)*	PR37B	2	RDQ37	C (LVDS)*

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A21	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
D23	PT73B	1		C	PT82B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
E21	PT73A	1		T	PT82A	1		T
D26	PT72B	1		C	PT81B	1		C
E26	PT72A	1		T	PT81A	1		T
E23	PT71B	1		C	PT80B	1		C
-	-	-			VCCIO1	1		
G22	PT71A	1		T	PT80A	1		T
VCCIO	VCCIO1	1			-	-		
D22	PT70B	1		C	PT79B	1		C
F21	PT70A	1		T	PT79A	1		T
G18	PT69B	1		C	PT78B	1		C
H18	PT69A	1		T	PT78A	1		T
D20	PT68B	1		C	PT77B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
D21	PT68A	1		T	PT77A	1		T
E20	PT67B	1		C	PT76B	1		C
E19	PT67A	1		T	PT76A	1		T
D19	PT66B	1		C	PT75B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
E18	PT66A	1		T	PT75A	1		T
D18	PT65B	1		C	PT74B	1		C
C17	PT65A	1		T	PT74A	1		T
A17	PT64B	1		C	PT73B	1		C
B17	PT64A	1		T	PT73A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
J18	NC	-			PT66B	1		C
J19	NC	-			PT66A	1		T
H17	NC	-			PT65B	1		C
J17	NC	-			PT65A	1		T
F18	NC	-			PT64B	1		C
F17	NC	-			PT64A	1		T
-	-	-			GNDIO1	-		
A16	PT54B	1		C	PT63B	1		C
B16	PT54A	1		T	PT63A	1		T
G17	PT53B	1		C	PT62B	1		C
G16	PT53A	1		T	PT62A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
H16	PT52B	1		C	PT61B	1		C
F16	PT52A	1		T	PT61A	1		T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K13	VCCIO0	0			VCCIO0	0		
D17	VCCIO1	1			VCCIO1	1		
E22	VCCIO1	1			VCCIO1	1		
E25	VCCIO1	1			VCCIO1	1		
F19	VCCIO1	1			VCCIO1	1		
K18	VCCIO1	1			VCCIO1	1		
K19	VCCIO1	1			VCCIO1	1		
F28	VCCIO2	2			VCCIO2	2		
J25	VCCIO2	2			VCCIO2	2		
K28	VCCIO2	2			VCCIO2	2		
M21	VCCIO2	2			VCCIO2	2		
M24	VCCIO2	2			VCCIO2	2		
N21	VCCIO2	2			VCCIO2	2		
N28	VCCIO2	2			VCCIO2	2		
P21	VCCIO2	2			VCCIO2	2		
R25	VCCIO2	2			VCCIO2	2		
AA28	VCCIO3	3			VCCIO3	3		
AB25	VCCIO3	3			VCCIO3	3		
AE28	VCCIO3	3			VCCIO3	3		
T25	VCCIO3	3			VCCIO3	3		
U21	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		
V28	VCCIO3	3			VCCIO3	3		
W21	VCCIO3	3			VCCIO3	3		
W24	VCCIO3	3			VCCIO3	3		
AA18	VCCIO4	4			VCCIO4	4		
AA19	VCCIO4	4			VCCIO4	4		
AE19	VCCIO4	4			VCCIO4	4		
AF22	VCCIO4	4			VCCIO4	4		
AG17	VCCIO4	4			VCCIO4	4		
AG25	VCCIO4	4			VCCIO4	4		
AA12	VCCIO5	5			VCCIO5	5		
AA13	VCCIO5	5			VCCIO5	5		
AE12	VCCIO5	5			VCCIO5	5		
AF9	VCCIO5	5			VCCIO5	5		
AG14	VCCIO5	5			VCCIO5	5		
AG6	VCCIO5	5			VCCIO5	5		
AA3	VCCIO6	6			VCCIO6	6		
AB6	VCCIO6	6			VCCIO6	6		
AE3	VCCIO6	6			VCCIO6	6		
T6	VCCIO6	6			VCCIO6	6		
U10	VCCIO6	6			VCCIO6	6		
V10	VCCIO6	6			VCCIO6	6		
V3	VCCIO6	6			VCCIO6	6		
W10	VCCIO6	6			VCCIO6	6		
W7	VCCIO6	6			VCCIO6	6		
F3	VCCIO7	7			VCCIO7	7		
J6	VCCIO7	7			VCCIO7	7		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
J2	PL34B	7	LDQ32	C (LVDS)*
H1	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-		
J1	PL35B	7	LDQ32	C
GNDIO	GNDIO7	-		
L5	PL41A	7	LDQ45	T (LVDS)*
L4	PL41B	7	LDQ45	C (LVDS)*
N9	PL42A	7	LDQ45	T
N7	PL42B	7	LDQ45	C
K2	PL43A	7	LDQ45	T (LVDS)*
K1	PL43B	7	LDQ45	C (LVDS)*
P9	PL44A	7	LDQ45	T
P7	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-		
M6	PL45A	7	LDQS45	T (LVDS)*
M5	PL45B	7	LDQ45	C (LVDS)*
N5	PL46A	7	LDQ45	T
N6	PL46B	7	LDQ45	C
M4	PL47A	7	LDQ45	T (LVDS)*
M3	PL47B	7	LDQ45	C (LVDS)*
P6	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-		
P8	PL48B	7	LDQ45	C
L3	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
L2	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
P5	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T
P4	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
L1	PL52A	7	LDQ54	T (LVDS)*
M2	PL52B	7	LDQ54	C (LVDS)*
R5	PL53A	7	LDQ54	T
R4	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-		
M1	PL54A	7	LDQS54	T (LVDS)*
N2	PL54B	7	LDQ54	C (LVDS)*
R8	PL55A	7	LDQ54	T
T9	PL55B	7	LDQ54	C
P3	PL56A	7	LDQ54	T (LVDS)*
P2	PL56B	7	LDQ54	C (LVDS)*
N1	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-		
P1	PL57B	7	PCLKC7_0/LDQ54	C
T5	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
T4	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E5	ULC_SQ_REFCLKN	11		C	ULC_SQ_REFCLKN	11		C
D5	ULC_SQ_REFCLKP	11		T	ULC_SQ_REFCLKP	11		T
D6	ULC_SQ_VCCP	11			ULC_SQ_VCCP	11		
C5	ULC_SQ_HDINP2	11		T	ULC_SQ_HDINP2	11		T
D4	ULC_SQ_VCCIB2	11			ULC_SQ_VCCIB2	11		
C4	ULC_SQ_HDINN2	11		C	ULC_SQ_HDINN2	11		C
B5	ULC_SQ_VCCRX2	11			ULC_SQ_VCCRX2	11		
A5	ULC_SQ_HDOUTP2	11		T	ULC_SQ_HDOUTP2	11		T
D3	ULC_SQ_VCCOB2	11			ULC_SQ_VCCOB2	11		
A4	ULC_SQ_HDOUTN2	11		C	ULC_SQ_HDOUTN2	11		C
B4	ULC_SQ_VCCTX2	11			ULC_SQ_VCCTX2	11		
A3	ULC_SQ_HDOUTN3	11		C	ULC_SQ_HDOUTN3	11		C
C1	ULC_SQ_VCCOB3	11			ULC_SQ_VCCOB3	11		
A2	ULC_SQ_HDOUTP3	11		T	ULC_SQ_HDOUTP3	11		T
B3	ULC_SQ_VCCTX3	11			ULC_SQ_VCCTX3	11		
C3	ULC_SQ_HDINN3	11		C	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11			ULC_SQ_VCCIB3	11		
C2	ULC_SQ_HDINP3	11		T	ULC_SQ_HDINP3	11		T
B2	ULC_SQ_VCCRX3	11			ULC_SQ_VCCRX3	11		
AA13	VCC	-			VCC	-		
AA14	VCC	-			VCC	-		
AA15	VCC	-			VCC	-		
AA16	VCC	-			VCC	-		
AA17	VCC	-			VCC	-		
AA18	VCC	-			VCC	-		
AA19	VCC	-			VCC	-		
AA20	VCC	-			VCC	-		
AA21	VCC	-			VCC	-		
AA22	VCC	-			VCC	-		
AB14	VCC	-			VCC	-		
AB15	VCC	-			VCC	-		
AB20	VCC	-			VCC	-		
AB21	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N15	VCC	-			VCC	-		
N20	VCC	-			VCC	-		
N21	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
P14	VCC	-			VCC	-		
P15	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
P17	VCC	-			VCC	-		
P18	VCC	-			VCC	-		
P19	VCC	-			VCC	-		
P20	VCC	-			VCC	-		
P21	VCC	-			VCC	-		
P22	VCC	-			VCC	-		
R13	VCC	-			VCC	-		
R14	VCC	-			VCC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F21	GND	-			GND	-		
G31	GND	-			GND	-		
G4	GND	-			GND	-		
J12	GND	-			GND	-		
J16	GND	-			GND	-		
J19	GND	-			GND	-		
J23	GND	-			GND	-		
K27	GND	-			GND	-		
K31	GND	-			GND	-		
K4	GND	-			GND	-		
K8	GND	-			GND	-		
M16	GND	-			GND	-		
M17	GND	-			GND	-		
M18	GND	-			GND	-		
M19	GND	-			GND	-		
N16	GND	-			GND	-		
N17	GND	-			GND	-		
N18	GND	-			GND	-		
N19	GND	-			GND	-		
N26	GND	-			GND	-		
N31	GND	-			GND	-		
N4	GND	-			GND	-		
N9	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R19	GND	-			GND	-		
T12	GND	-			GND	-		
T13	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T19	GND	-			GND	-		
T20	GND	-			GND	-		
T22	GND	-			GND	-		
T23	GND	-			GND	-		
T26	GND	-			GND	-		
T31	GND	-			GND	-		
T4	GND	-			GND	-		
T9	GND	-			GND	-		
U12	GND	-			GND	-		
U13	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U19	GND	-			GND	-		
U20	GND	-			GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U22	GND	-			GND	-		
U23	GND	-			GND	-		
V12	GND	-			GND	-		
V13	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V18	GND	-			GND	-		
V19	GND	-			GND	-		
V20	GND	-			GND	-		
V22	GND	-			GND	-		
V23	GND	-			GND	-		
W12	GND	-			GND	-		
W13	GND	-			GND	-		
W15	GND	-			GND	-		
W16	GND	-			GND	-		
W17	GND	-			GND	-		
W18	GND	-			GND	-		
W19	GND	-			GND	-		
W20	GND	-			GND	-		
W22	GND	-			GND	-		
W23	GND	-			GND	-		
W26	GND	-			GND	-		
W31	GND	-			GND	-		
W4	GND	-			GND	-		
W9	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
Y18	GND	-			GND	-		
Y19	GND	-			GND	-		
A11	NC	-			NC	-		
A12	NC	-			NC	-		
A23	NC	-			NC	-		
A24	NC	-			NC	-		
AA11	NC	-			NC	-		
AB11	NC	-			NC	-		
AC26	NC	-			NC	-		
AC30	NC	-			NC	-		
AD11	NC	-			NC	-		
AD12	NC	-			NC	-		
AD13	NC	-			NC	-		
AD14	NC	-			NC	-		
AD15	NC	-			NC	-		
AD19	NC	-			NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD23	NC	-			NC	-		
AE10	NC	-			NC	-		
AE11	NC	-			NC	-		