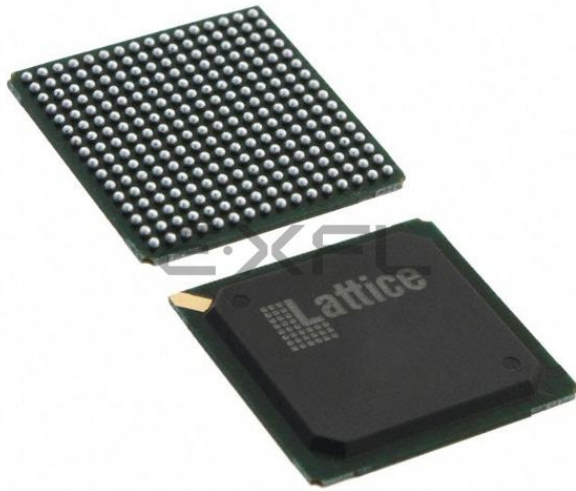




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20e-5fn256i

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2/M family of devices has two DLLs per device.

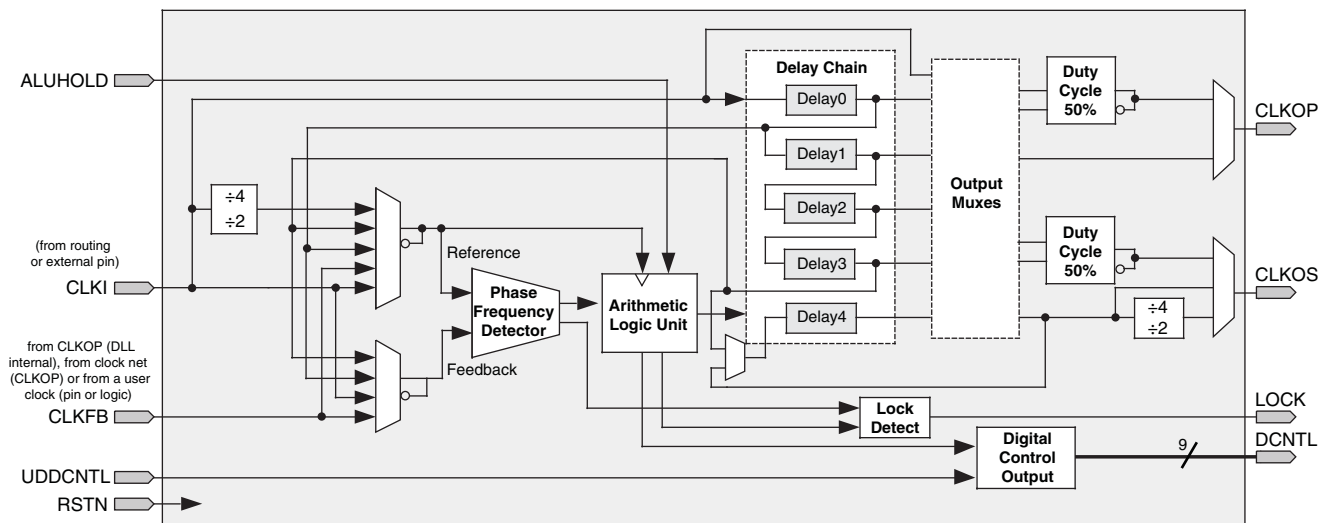
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is fed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLLDELA delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-6 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-6. Delay Locked Loop Diagram (DLL)



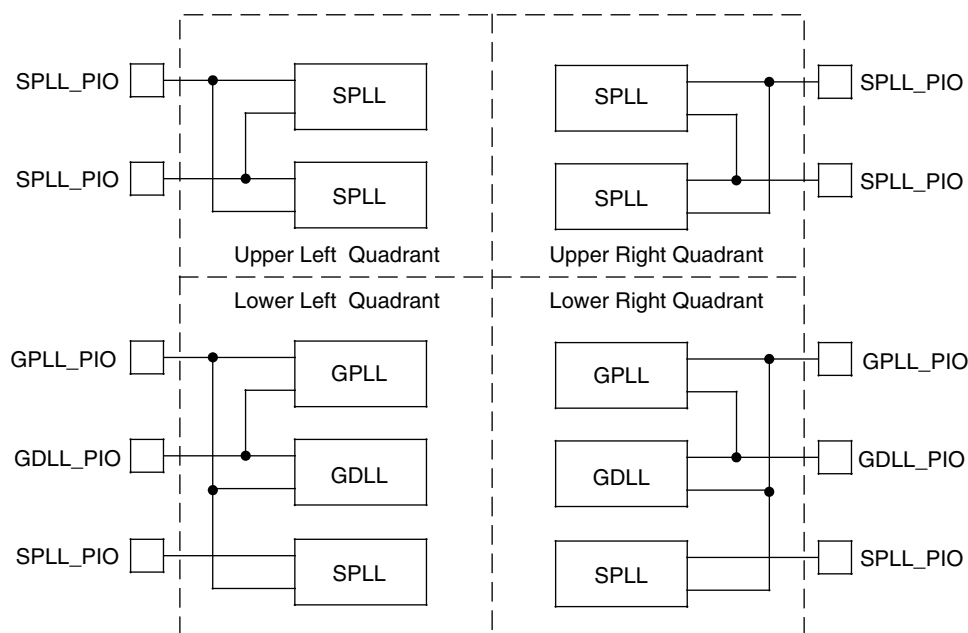
The DLLs in the LatticeECP2/M are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

GPLL/SPLL/GDLL PIO Input Pin Connections (LatticeECP2M Family Only)

All LatticeECP2M devices contain two GDLLs, two GPLLs and six SPLLs, arranged in quadrants as shown in Figure 2-8. In the LatticeECP2M devices GPLLs, SPLLs and GDLLs share their input pins. Figure 2-8 shows the sharing of SPLLs input pin connections in the upper two quadrants and the sharing of GDLL, GPLL and SPLL input pin connections in the lower two quadrants.

Figure 2-8. Sharing of PIO Pins by GPLL, SPLL and GDLL in LatticeECP2M Devices



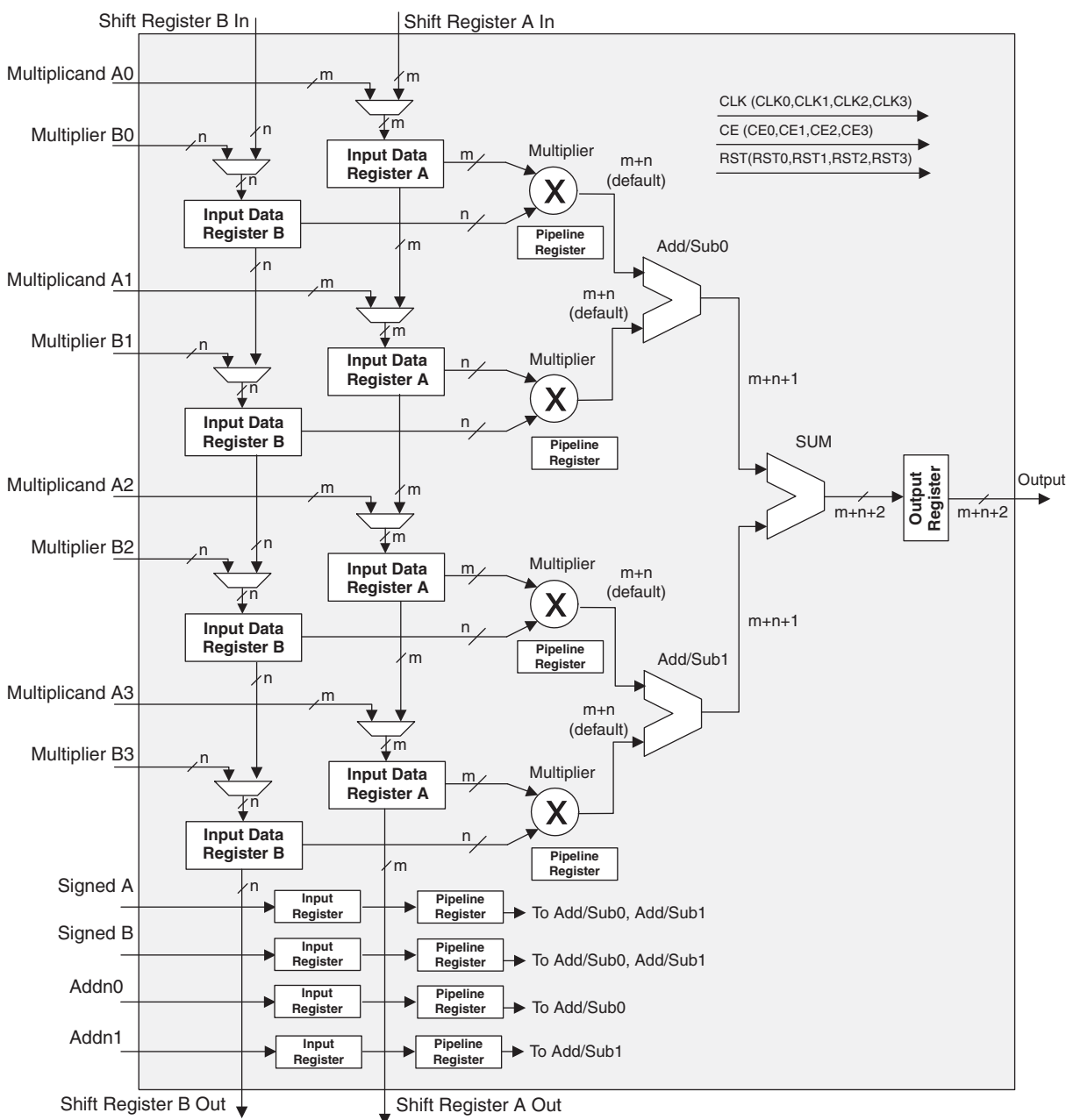
Clock Dividers

LatticeECP2/M devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 4$ or $\div 8$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL-DELA delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information about clock dividers, please see the list of additional technical documentation at the end of this data sheet. Figure 2-9 shows the clock divider connections.

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

Figure 2-26. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

Table 2-12. PIO Signals List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block flip-flops
CLK0, CLK1	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK ²	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0 ¹ , QPOS1 ¹	Input to the core	Gearbox pipelined inputs to the core
QNEG0 ¹ , QNEG1 ¹	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Output data from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.

2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs in left, right and bottom edges contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-29 shows the diagram of the input register block for left, right and bottom edges. The input register block for the top edge contains one memory element to register the input signal as shown in Figure 2-30. The following description applies to the input register block for PIOs in the left, right and bottom edges of the device.

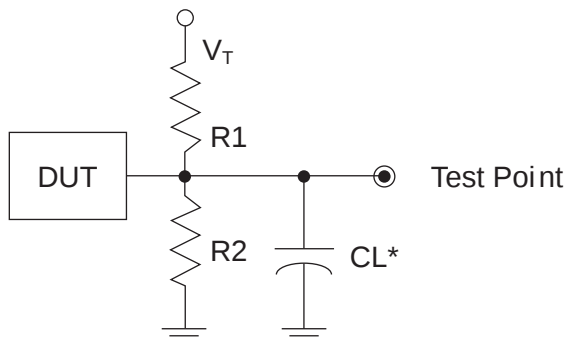
Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In DDR Mode, two registers are used to sample the data on the positive and negative edges of the DQS signal, creating two data streams, D0 and D1. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Switching Test Conditions

Figure 3-22 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-19.

Figure 3-22. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L → H, H → L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → H)	∞	1MΩ		V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H → Z)	∞	100		V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L → Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 (Cont.)

Pin Type		LFE2M50			LFE2M70		LFE2M100	
		484 fpBGA	672 fpBGA	900 fpBGA	900 fpBGA	1152 fpBGA	900 fpBGA	1152 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	2	2	2	4	4	4	4
	Bank3	2	1	1	3	4	3	5
	Bank4	3	1	3	3	3	3	3
	Bank5	2	3	3	2	3	2	3
	Bank6	1	2	2	3	4	3	5
	Bank7	3	3	3	4	4	4	5
	Bank8	0	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	0	0	0	0	72	0	80
	Bank3	0	0	0	0	64	0	80
	Bank4	50	24	48	48	40	48	44
	Bank5	60	60	50	40	40	40	46
	Bank6	52	54	60	62	66	62	82
	Bank7	60	60	68	70	74	70	90
	Bank8	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

Available Device Resources by Package, LatticeECP2

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA
PLL/DLL	ECP2-6	4	—	—	—
	ECP2-12	4	4	—	—
	ECP2-20	4	4	4	—
	ECP2-35	—	4	4	—
	ECP2-50	—	6	6	—
	ECP2-70	—	—	8	8

Available Device Resources by Package, LatticeECP2M

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA	1152 fpBGA
PLL/DLL	ECP2M20	10	10	—	—	—
	ECP2M35	10	10	10	—	—
	ECP2M50	—	10	10	10	—
	ECP2M70	—	—	—	10	10
	ECP2M100	—	—	—	10	10

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
V _{CC}	LFE2M35: AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 LFE2M50: L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	LFE2M50: AH1, AH4, AH5, AH2, AH7, AH12, AH9, AH10, AH13, C13, C10, C9, C12, C7, C2, C5, C4, C1, L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19 LFE2M70/LFE2M100: L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19
V _{CCIO0}	B12, B7, F11, J13, K12	D14, E6, E9, F12, K12, K13
V _{CCIO1}	D18, F16, J14, K15	D17, E22, E25, F19, K18, K19
V _{CCIO2}	G25, L21, M17, M25, N18	F28, J25, K28, M21, M24, N21, N28, P21, R25
V _{CCIO3}	P18, R17, R25, T21, Y25	AA28, AB25, AE28, T25, U21, V21, V28, W21, W24
V _{CCIO4}	AA16, AC18, U15, V14	AA18, AA19, AE19, AF22, AG17, AG25
V _{CCIO5}	AA11, AE12, AE7, U12, V13	AA12, AA13, AE12, AF9, AG14, AG6
V _{CCIO6}	P9, R10, R2, T6, Y2	AA3, AB6, AE3, T6, U10, V10, V3, W10, W7
V _{CCIO7}	G2, L6, M10, M2, N9	F3, J6, K3, M10, M7, N10, N3, P10, R6
V _{CCIO8}	AC24, U17	AA25, AD28
V _{CCJ}	AA7	AG1
V _{CCAUX}	LFE2M35: AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16 LFE2M50: J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16	LFE2M50: AJ7, B7, AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21 LFE2M70/LFE2M100: AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21
V _{CCPLL}	H7, K6, P7, R8, V18, P20, J17, G19	N13, N18, V13, V18
SERDES Power ³	LFE2M35: C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13 LFE2M50: AD13, AE13, AD16, AF16, AD17, AD18, AD14, AD15, AD19, AE19, AD23, AD24, AD20, AD21, AF22, AD22, AE25, AD25, C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13	LFE2M50: AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18 LFE2M70/LFE2M100: C13, B13, C10, A10, C9, C8, C12, C11, B7, C7, C3, C2, C6, C5, A4, C4, B1, C1, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18, AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, AH1, AJ1, AH4, AK4, AH5, AH6, AH2, AH3, AH7, AJ7, AH11, AH12, AH8, AH9, AK10, AH10, AJ13, AH13

LFE2-20E/SE Logic Signal Connections: 256 fpBGA

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C3	C3	PL2A	7	VREF2_7	T (LVDS)*
C2	C2	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO	VCCIO7	7		
-	GND	GNDIO7	7		
D3	D3	PL7A	7	LDQ8	T
D4	D4	PL6A	7	LDQ8	T (LVDS)*
D2	D2	PL7B	7	LDQ8	C
GND	GND	GNDIO7	-		
E4	E4	PL6B	7	LDQ8	C (LVDS)*
B1	B1	PL13A	7	LDQ16	T
C1	C1	PL13B	7	LDQ16	C
F5	F5	PL15A	7	LDQ16	T
VCCIO	VCC	VCCIO	7		
F4	F4	PL14A	7	LDQ16	T (LVDS)*
G6	G6	PL15B	7	LDQ16	C
G4	G4	PL14B	7	LDQ16	C (LVDS)*
D1	D1	PL16A	7	LDQS16	T (LVDS)*
GND	GND	GNDIO7	-		
E1	E1	PL16B	7	LDQ16	C (LVDS)*
F3	F3	PL17A	7	LDQ16	T
G3	G3	PL17B	7	LDQ16	C
VCCIO	VCCIO	VCCIO7	7		
F2	F2	PL18A	7	LDQ16	T (LVDS)*
F1	F1	PL18B	7	LDQ16	C (LVDS)*
GND	GND	GNDIO7	-		
G2	G2	PL19A	7	PCLKT7_0/LDQ16	T
G1	G1	PL19B	7	PCLKC7_0/LDQ16	C
H6	H6	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
H5	H5	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
H4	H4	PL22A	6	VREF2_6/LDQ25	T
GND	GND	GNDIO6	-		
H3	H3	PL22B	6	VREF1_6/LDQ25	C
H2	H2	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
H1	H1	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
G10	G10	VCC	-		
J4	J4	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T
J5	J5	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C
J6	J6	LLM0_PLLCAP	6		
K4	K4	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
GND	GND	GNDIO6	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
-	-	-			GNDIO7	-			
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*	
F4	PL3A	7		T	PL5A	7	LDQ8	T	
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*	
F5	PL3B	7		C	PL5B	7	LDQ8	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
G6	PL5A	7		T	PL7A	7	LDQ8	T	
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
G7	PL5B	7		C	PL7B	7	LDQ8	C	
GNDIO	GNDIO7	-			GNDIO7	-			
F1	NC	-			PL9A	7	LDQ8	T	
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*	
F2	NC	-			PL9B	7	LDQ8	C	
-	-	-			VCCIO7	7			
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*	
G1	NC	-			PL11A	7	LDQ8	T	
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*	
G2	NC	-			PL11B	7	LDQ8	C	
-	-	-			GNDIO	-			
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*	
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T	
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*	
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C	
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C	
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*	
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C	
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
VCCIO	VCCIO6	6			-	-			

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M6	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
M3	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T
GNDIO	GNDIO6	-			-	-		
M4	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C
-	-	-			VCCIO6	6		
N1	NC	-			PL24A	6	LDQ25	T
M2	NC	-			PL23A	6	LDQ25	T (LVDS)*
N2	NC	-			PL24B	6	LDQ25	C
M1	NC	-			PL23B	6	LDQ25	C (LVDS)*
-	-	-			GNDIO	-		
N3	NC	-			PL25A	6	LDQS25	T (LVDS)*
N5	NC	-			PL26A	6	LDQ25	T
N4	NC	-			PL25B	6	LDQ25	C (LVDS)*
-	-	-			VCCIO6	6		
P5	NC	-			PL26B	6	LDQ25	C
P1	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
P2	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
P4	PL18A	6	LLM0_GDLLT_FB_A	T	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T
-	-	-			GNDIO	-		
R4	PL18B	6	LLM0_GDLLC_FB_A	C	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C
P6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
R1	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
GNDIO	GNDIO6	-			-	-		
R3	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
R2	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A/LDQ34	C (LVDS)*
T4	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
T5	PL23A	6		T	PL33A	6	LDQ34	T
VCCIO	VCCIO6	6			VCCIO6	6		
T1	PL22A	6		T (LVDS)*	PL32A	6	LDQ34	T (LVDS)*
T3	PL23B	6		C	PL33B	6	LDQ34	C
T2	PL22B	6		C (LVDS)*	PL32B	6	LDQ34	C (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
-	-	-			VCCIO6	6		
V1	PL25A	6	LDQ28	T	PL39A	6	LDQ42	T
-	-	-			GNDIO	-		
V2	PL25B	6	LDQ28	C	PL39B	6	LDQ42	C
U1	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*
U3	PL27A	6	LDQ28	T	PL41A	6	LDQ42	T
VCCIO	VCCIO6	6			VCCIO6	6		
U2	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*
U4	PL27B	6	LDQ28	C	PL41B	6	LDQ42	C
R6	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*
R7	PL29A	6	LDQ28	T	PL43A	6	LDQ42	T
GNDIO	GNDIO6	-			GNDIO	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M19	NC	-			PR26A	3	RDQ25	T
J22	NC	-			PR23B	3	RDQ25	C (LVDS)*
-	-	-			GNDIO	-		
L22	NC	-			PR24B	3	RDQ25	C
H22	NC	-			PR23A	3	RDQ25	T (LVDS)*
K22	NC	-			PR24A	3	RDQ25	T
M20	PR16B	3	VREF2_3	C	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO3	3			VCCIO3	3		
L21	PR16A	3	VREF1_3	T	PR22A	3	VREF1_3/RDQ25	T
K21	PR15B	3	PCLKC3_0	C (LVDS)*	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J21	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
M18	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
L17	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T
L19	PR12B	2	RDQ10	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
K18	PR10B	2	RDQ10	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
L20	PR12A	2	RDQ10	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR10A	2	RDQS10	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
L18	PR11B	2	RDQ10	C	PR17B	2	RDQ16	C
K17	PR11A	2	RDQ10	T	PR17A	2	RDQ16	T
GNDIO	GNDIO2	-			GNDIO2	-		
J17	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*
G22	PR9B	2	RDQ10	C	PR15B	2	RDQ16	C
J18	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*
F22	PR9A	2	RDQ10	T	PR15A	2	RDQ16	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*
K20	PR7B	2	RDQ10	C	PR13B	2	RDQ16	C
G21	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*
J19	PR7A	2	RDQ10	T	PR13A	2	RDQ16	T
D22	NC	-			PR10B	2	RDQ8	C (LVDS)*
F21	NC	-			PR11B	2	RDQ8	C
-	-	-			GNDIO	-		
E21	NC	-			PR10A	2	RDQ8	T (LVDS)*
E22	NC	-			PR11A	2	RDQ8	T
H19	NC	-			PR8B	2	RDQ8	C (LVDS)*
G20	NC	-			PR9B	2	RDQ8	C
-	-	-			VCCIO2	2		
G19	NC	-			PR8A	2	RDQS8	T (LVDS)*
F20	NC	-			PR9A	2	RDQ8	T
G17	PR5B	2		C	PR7B	2	RDQ8	C
GNDIO	GNDIO2	-			GNDIO2	-		
E20	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AD2	PL90B	6	LDQ88	C (LVDS)*
AD7	PL91A	6	LDQ88	T
GND	GNDIO6	-		
AB9	PL91B	6	LDQ88	C
AD5	TCK	-		
AE7	TDI	-		
AD4	TMS	-		
AA9	TDO	-		
AD3	VCCJ	-		
AC8	PB2A	5	VREF2_5/BDQ6	T
AE8	PB2B	5	VREF1_5/BDQ6	C
AD8	PB3A	5	BDQ6	T
AF8	PB3B	5	BDQ6	C
AG7	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5		
AH7	PB4B	5	BDQ6	C
AC9	PB5A	5	BDQ6	T
AE9	PB5B	5	BDQ6	C
AD9	PB6A	5	BDQS6	T
GND	GNDIO5	-		
AF9	PB6B	5	BDQ6	C
AB10	PB7A	5	BDQ6	T
AA10	PB7B	5	BDQ6	C
AJ7	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5		
AK7	PB8B	5	BDQ6	C
AC10	PB9A	5	BDQ6	T
AE10	PB9B	5	BDQ6	C
AJ8	PB10A	5	BDQ6	T
GND	GNDIO5	-		
AK8	PB10B	5	BDQ6	C
AF6	PB11A	5	BDQ15	T
AF7	PB11B	5	BDQ15	C
AG5	PB12A	5	BDQ15	T
AH5	PB12B	5	BDQ15	C
AG6	PB13A	5	BDQ15	T
AH6	PB13B	5	BDQ15	C
VCCIO	VCCIO5	5		
AJ4	PB14A	5	BDQ15	T
AK4	PB14B	5	BDQ15	C
GND	GNDIO5	-		
AJ5	PB15A	5	BDQS15	T
AK5	PB15B	5	BDQ15	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
E27	NC	-		
E28	NC	-		
E29	NC	-		
E3	NC	-		
E30	NC	-		
E4	NC	-		
E5	NC	-		
E6	NC	-		
F25	NC	-		
F5	NC	-		
F6	NC	-		
G6	NC	-		
G7	NC	-		
K10	NC	-		
K9	NC	-		
N27	NC	-		
N4	NC	-		
R1	NC	-		
R2	NC	-		
V27	NC	-		
V4	NC	-		
P22	VCCPLL	-		
P8	VCCPLL	-		
T22	VCCPLL	-		
Y7	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO0	-			GNDIO0	-			
F7	PT9B	0		C	PT9B	0		C	
G7	PT9A	0		T	PT9A	0		T	
C3	PT8B	0		C	PT8B	0		C	
D4	PT8A	0		T	PT8A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F6	PT7B	0		C	PT7B	0		C	
E6	PT7A	0		T	PT7A	0		T	
E5	PT6B	0		C	PT6B	0		C	
D6	PT6A	0		T	PT6A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
D3	PT5B	0		C	PT5B	0		C	
E3	PT5A	0		T	PT5A	0		T	
D5	PT4B	0		C	PT4B	0		C	
E4	PT4A	0		T	PT4A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
C2	PT3B	0		C	PT3B	0		C	
B2	PT3A	0		T	PT3A	0		T	
B1	PT2B	0		C	PT2B	0		C	
C1	PT2A	0		T	PT2A	0		T	
R8	VCCPLL	-			VCCPLL	-			
H15	VCCPLL	-			VCCPLL	-			
H8	VCCPLL	-			VCCPLL	-			
R15	VCCPLL	-			VCCPLL	-			
J10	VCC	-			VCC	-			
J11	VCC	-			VCC	-			
J12	VCC	-			VCC	-			
J13	VCC	-			VCC	-			
K14	VCC	-			VCC	-			
K9	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L9	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M9	VCC	-			VCC	-			
N14	VCC	-			VCC	-			
N9	VCC	-			VCC	-			
P10	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P13	VCC	-			VCC	-			
B5	VCCIO0	0			VCCIO0	0			
B9	VCCIO0	0			VCCIO0	0			
E7	VCCIO0	0			VCCIO0	0			
H9	VCCIO0	0			VCCIO0	0			
D13	VCCIO1	1			VCCIO1	1			
E16	VCCIO1	1			VCCIO1	1			
H14	VCCIO1	1			VCCIO1	1			
E21	VCCIO2	2			VCCIO2	2			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U21	CS1N***	8		
U17	CSN***	8		
U16	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8		
T16	D1***	8		
T17	D2***	8		
T22	D3***	8		
GNDIO	GNDIO8	-		
R22	D4***	8		
T15	D5***	8		
R17	D6***	8		
T20	D7/SPID0***	8		
VCCIO	VCCIO8	8		
T21	DI/CSSPI0N***	8		
R21	DOUT/CSON/CSSPI1N***	8		
R20	BUSY/SISPI***	8		
R16	RLM0_PLLCAP	3		
R18	PR65B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	-		
R19	PR65A	3	RLM0_GDLLT_FB_A	T
P22	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
P21	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
P16	PR63B	3	RLM0_GPLL_C_IN_A**	C
VCCIO	VCCIO3	3		
P17	PR63A	3	RLM0_GPLLT_IN_A**	T
P20	PR62B	3	RLM0_GPLL_C_FB_A	C (LVDS)*
P19	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*
GNDIO	GNDIO3	-		
VCCIO	VCCIO3	3		
P18	PR55B	3	RDQ52	C
N16	PR55A	3	RDQ52	T
GNDIO	GNDIO3	-		
N22	PR54B	3	RDQ52	C (LVDS)*
N21	PR54A	3	RDQ52	T (LVDS)*
N17	PR53B	3	RDQ52	C
N18	PR53A	3	RDQ52	T
VCCIO	VCCIO3	3		
M22	PR52B	3	RDQ52	C (LVDS)*
M21	PR52A	3	RDQS52	T (LVDS)*
M16	PR51B	3	RDQ52	C
GNDIO	GNDIO3	-		
M17	PR51A	3	RDQ52	T
M20	PR50B	3	RDQ52	C (LVDS)*

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K19	PR16A	2	RDQ15	T	PR19A	2		T	
G24	PR15B	2	RDQ15	C (LVDS)*	PR18B	2		C*	
G23	PR15A	2	RDQS15	T (LVDS)*	PR18A	2		T*	
GNDIO	GNDIO2	-			GNDIO2	-			
J18	PR14B	2	RDQ15	C	PR14B	2		C	
F22	PR14A	2	RDQ15	T	PR14A	2		T	
-	-	-			VCCIO2	2			
F23	PR13B	2	RDQ15	C (LVDS)*	PR13B	2		C*	
F24	PR13A	2	RDQ15	T (LVDS)*	PR13A	2		T*	
VCCIO	VCCIO2	2			-	-			
H20	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	PR12B	2	RUM0_SPLLC_FB_A	C	
-	-	-			GNDIO2	-			
F21	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	PR12A	2	RUM0_SPLLT_FB_A	T	
G26	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A	C*	
F26	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A	T*	
-	-	-			VCCIO2	2			
E24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
GNDIO	GNDIO2	-			GNDIO2	-			
E23	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO4	4			VCCIO2	2			
H19	XRES	-			XRES	-			
C25	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A24	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B25	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B24	URC_SQ_HDIN_N0	12		C	URC_SQ_HDIN_N0	12		C	
C22	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A21	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A22	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B21	URC_SQ_HDOUT_N0	12		C	URC_SQ_HDOUT_N0	12		C	
C21	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B20	URC_SQ_HDOUT_N1	12		C	URC_SQ_HDOUT_N1	12		C	
C20	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A20	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C24	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B23	URC_SQ_HDIN_N1	12		C	URC_SQ_HDIN_N1	12		C	
C23	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A23	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B19	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E19	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D19	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C19	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A15	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L5	PL23A	7	LDQ27	T (LVDS)*	PL33A	7	LDQ37	T (LVDS)*	
L4	PL23B	7	LDQ27	C (LVDS)*	PL33B	7	LDQ37	C (LVDS)*	
N9	PL24A	7	LDQ27	T	PL34A	7	LDQ37	T	
N7	PL24B	7	LDQ27	C	PL34B	7	LDQ37	C	
K2	PL25A	7	LDQ27	T (LVDS)*	PL35A	7	LDQ37	T (LVDS)*	
K1	PL25B	7	LDQ27	C (LVDS)*	PL35B	7	LDQ37	C (LVDS)*	
P9	PL26A	7	LDQ27	T	PL36A	7	LDQ37	T	
P7	PL26B	7	LDQ27	C	PL36B	7	LDQ37	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M6	PL27A	7	LDQS27	T (LVDS)*	PL37A	7	LDQS37	T (LVDS)*	
M5	PL27B	7	LDQ27	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
N5	PL28A	7	LDQ27	T	PL38A	7	LDQ37	T	
N6	PL28B	7	LDQ27	C	PL38B	7	LDQ37	C	
M4	PL29A	7	LDQ27	T (LVDS)*	PL39A	7	LDQ37	T (LVDS)*	
M3	PL29B	7	LDQ27	C (LVDS)*	PL39B	7	LDQ37	C (LVDS)*	
P6	PL30A	7	LDQ27	T	PL40A	7	LDQ37	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P8	PL30B	7	LDQ27	C	PL40B	7	LDQ37	C	
L3	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	
L2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	
P5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	
P4	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	
L1	PL34A	7	LDQ36	T (LVDS)*	PL44A	7	LDQ46	T (LVDS)*	
M2	PL34B	7	LDQ36	C (LVDS)*	PL44B	7	LDQ46	C (LVDS)*	
R5	PL35A	7	LDQ36	T	PL45A	7	LDQ46	T	
R4	PL35B	7	LDQ36	C	PL45B	7	LDQ46	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M1	PL36A	7	LDQS36	T (LVDS)*	PL46A	7	LDQS46	T (LVDS)*	
N2	PL36B	7	LDQ36	C (LVDS)*	PL46B	7	LDQ46	C (LVDS)*	
R8	PL37A	7	LDQ36	T	PL47A	7	LDQ46	T	
T9	PL37B	7	LDQ36	C	PL47B	7	LDQ46	C	
P3	PL38A	7	LDQ36	T (LVDS)*	PL48A	7	LDQ46	T (LVDS)*	
P2	PL38B	7	LDQ36	C (LVDS)*	PL48B	7	LDQ46	C (LVDS)*	
N1	PL39A	7	PCLKT7_0/LDQ36	T	PL49A	7	PCLKT7_0/LDQ46	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P1	PL39B	7	PCLKC7_0/LDQ36	C	PL49B	7	PCLKC7_0/LDQ46	C	
T5	PL41A	6	PCLKT6_0	T (LVDS)*	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	
T4	PL41B	6	PCLKC6_0	C (LVDS)*	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	
U7	PL42A	6	VREF2_6	T	PL52A	6	VREF2_6/LDQ55	T	
T8	PL42B	6	VREF1_6	C	PL52B	6	VREF1_6/LDQ55	C	
R3	PL43A	6		T (LVDS)*	PL53A	6	LDQ55	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
R2	PL43B	6		C (LVDS)*	PL53B	6	LDQ55	C (LVDS)*	
R1	PL44A	6		T	PL54A	6	LDQ55	T	
T1	PL44B	6		C	PL54B	6	LDQ55	C	
GNDIO	GNDIO6	-			GNDIO6	-			
-	-	-			VCCIO6	6			
T3	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	

Date	Version	Section	Change Summary
August 2007 (cont.)	02.8 (cont.)	DC and Switching (cont.)	sysCLOCK GPLL timing has been updated.
		Pinout Information	Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information.
		Ordering Information	1156-fpBGA package option has been removed from the LatticeECP2M family.
September 2007	02.9	Pinout Information	Added Thermal Management text section.
February 2008	03.0	Architecture	Added LVC MOS33D description.
		DC and Switching	LatticeECP2M Supply Current has been updated.
			Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11).
			Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated.
			Table 3-8. Channel output Jitter (Max) has been updated.
		Pinout Information	Signal description has been updated.
April 2008	03.1	Pinout Information	Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100.
June 2008	03.2	Pinout Information	Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated.
		Introduction	Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
August 2008	03.3	DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
		Pinout Information	Added information for [LOC]DQ[num] to Signal Descriptions table.
January 2009	03.4	DC and Switching Characteristics	Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode.
			Added Channel Output Jitter table for x20 mode.
November 2009	03.5	DC and Switching Characteristics	Updated SPI/SPI _m Configuration Waveforms diagram.
			Updated footnotes in LatticeECP2 Initialization Supply Current table.
			Updated footnotes in LatticeECP2M Initialization Supply Current table.
			Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table.
			Updated max. value for t _{DINIT} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.
			Updated Serial Output Timing and Levels table.
			Updated Figure 3-5 MLVDS
			Updated Table 3-7 Serial Output Timing and Levels
			Updated Table 3-15 Power Down/Power Up Specification
		Pinout Information	Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5.