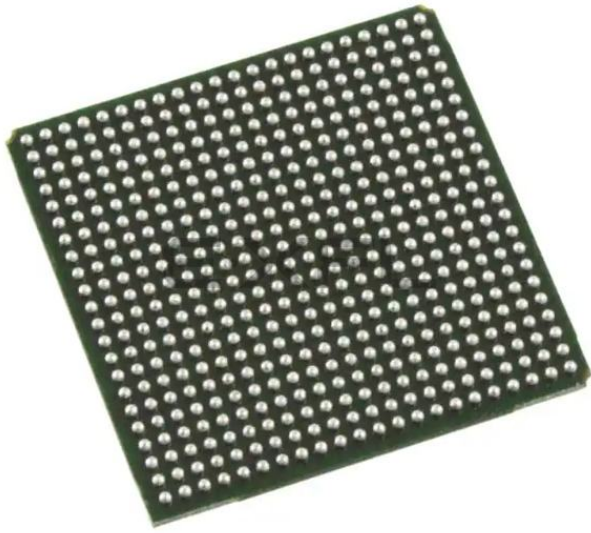




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

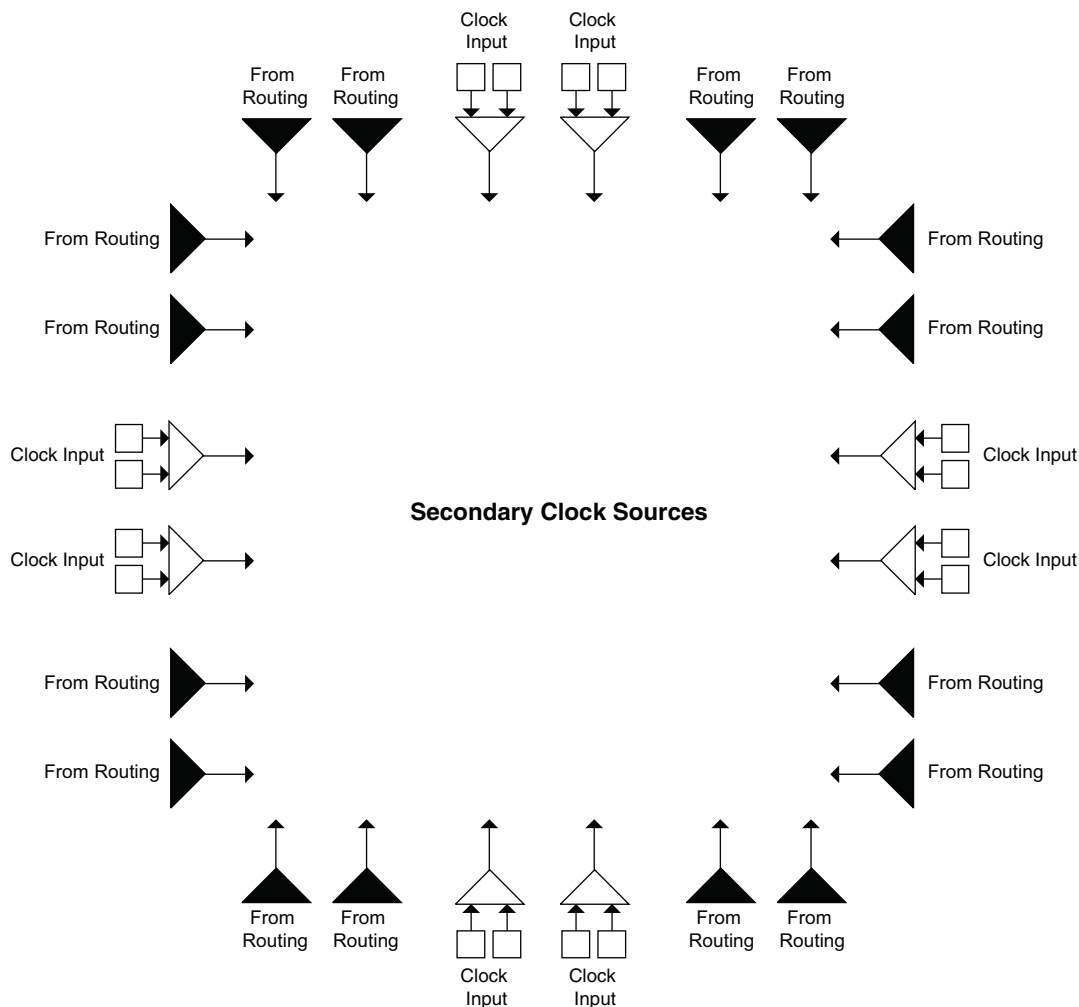
Details

Product Status	Active
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	331
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20e-5fn484c

Secondary Clock/Control Sources

LatticeECP2/M devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-11 shows the secondary clock sources.

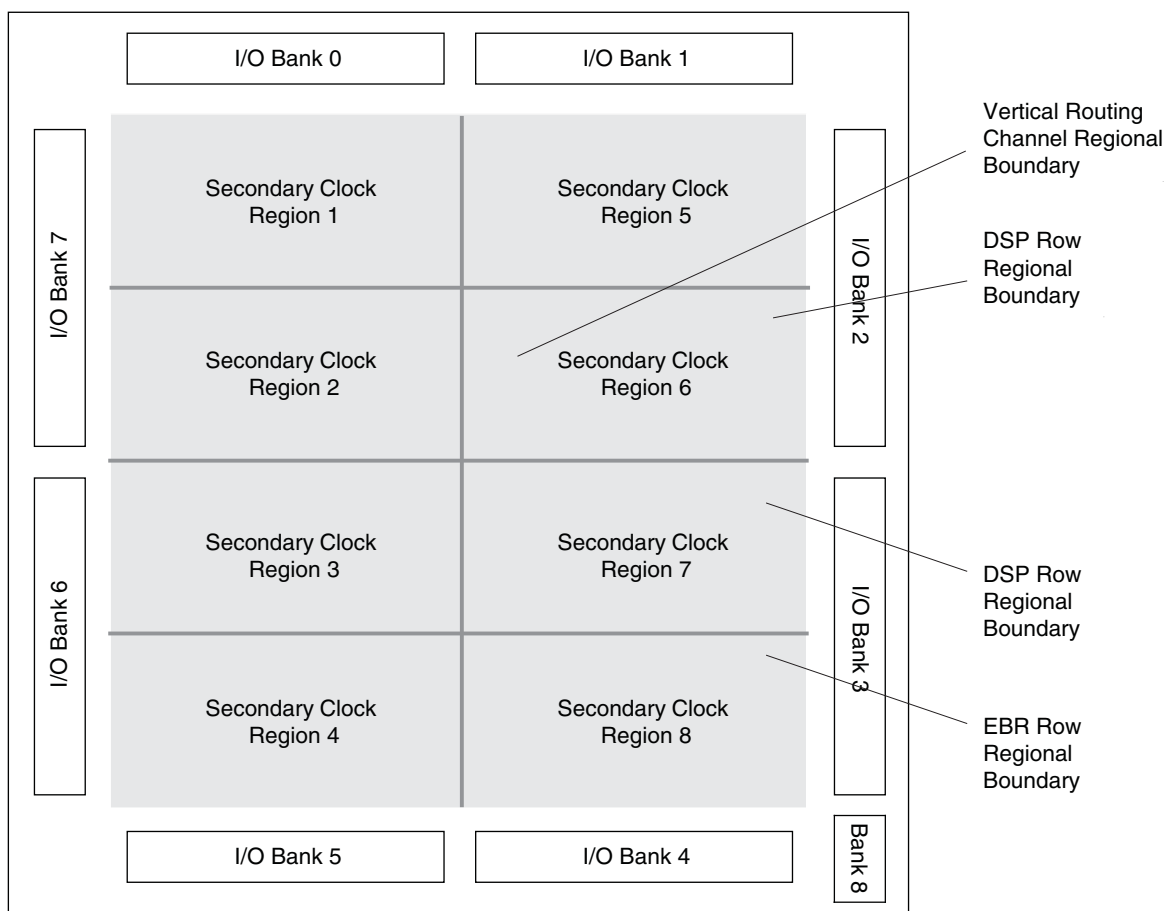
Figure 2-11. Secondary Clock Sources



this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

Figure 2-15. Secondary Clock Regions ECP2-50



IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

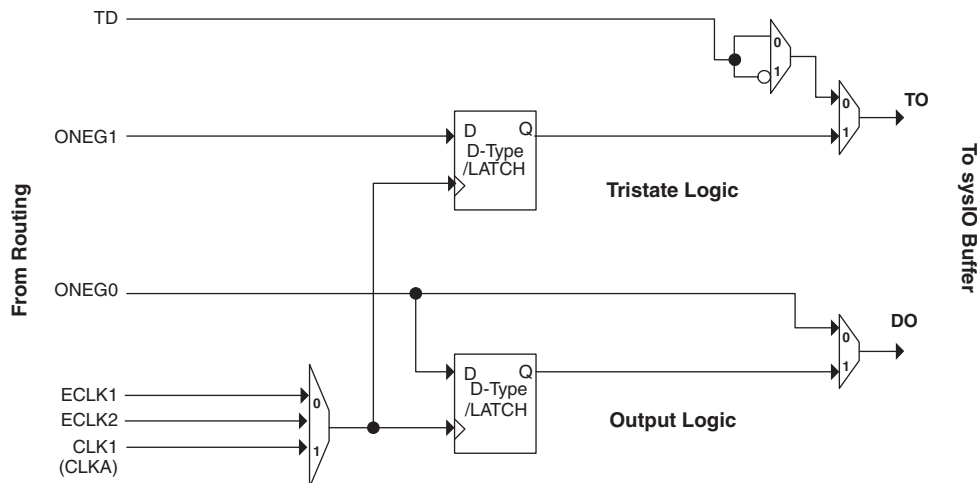
Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

Figure 2-32. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (DO).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

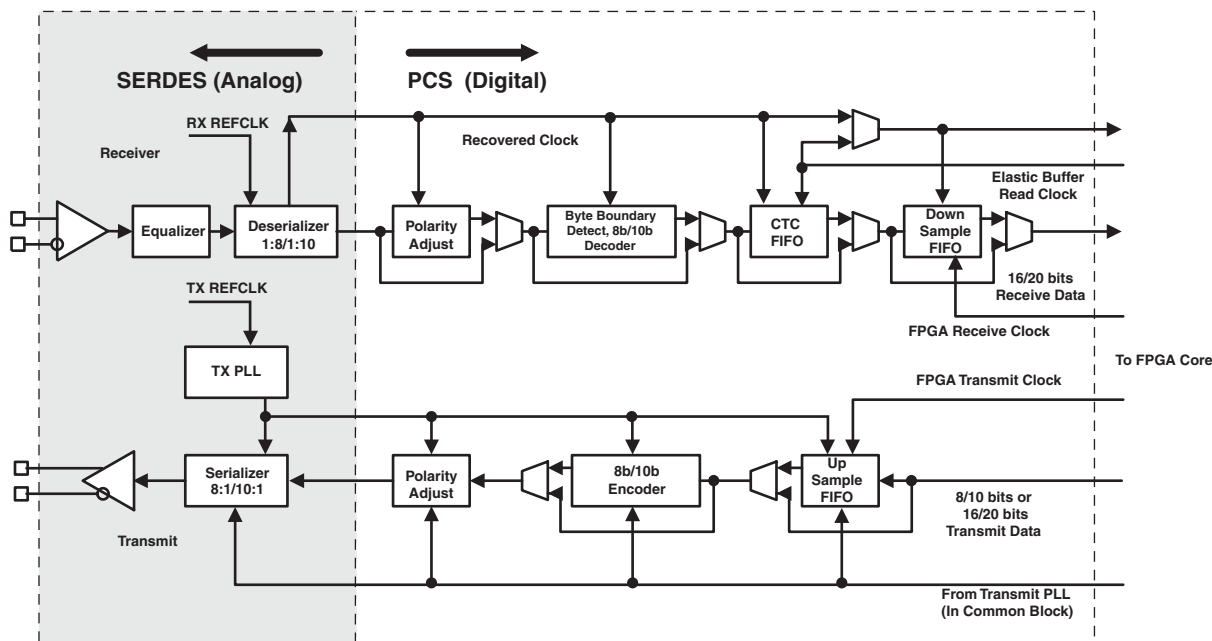
PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

Bottom Edge

PICs on the bottom edge have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel also have their own independent power supplies. In addition, there are separate power supplies for PLL, terminating resistor per quad.

Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS



PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With Diamond, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information about SERDES, please see the list of additional technical documentation at the end of this data sheet.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

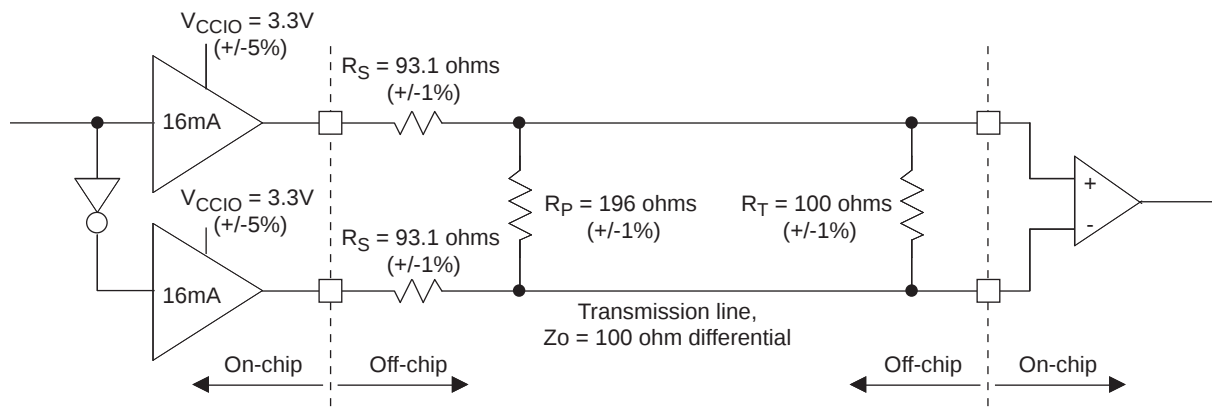


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	3.8	ns
32-bit Decoder	4.5	ns
64-bit Decoder	5.0	ns
4:1 MUX	3.2	ns
8:1 MUX	3.4	ns
16:1 MUX	3.5	ns
32:1 MUX	4.0	ns

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	599	MHz
32-bit Decoder	542	MHz
64-bit Decoder	417	MHz
4:1 MUX	847	MHz
8:1 MUX	803	MHz
16:1 MUX	660	MHz
32:1 MUX	577	MHz
8-bit Adder	591	MHz
16-bit Adder	500	MHz
64-bit Adder	306	MHz
16-bit Counter	488	MHz
32-bit Counter	378	MHz
64-bit Counter	260	MHz
64-bit Accumulator	253	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	280	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	819	MHz
32x4 Pseudo-Dual Port RAM	521	MHz
64x8 Pseudo-Dual Port RAM	435	MHz
DSP Functions		
18x18 Multiplier (All Registers)	420	MHz
9x9 Multiplier (All Registers)	420	MHz

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	420	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	20	—	420	MHz
		With external capacitor ⁵	5	—	50	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.156	—	210	MHz
		With external capacitor ⁵	0.039	—	25	MHz
f _{VCO}	PLL VCO Frequency		640	—	1280	MHz
f _{PFD}	Phase Detector Input Frequency	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	50	MHz
AC Characteristics						
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{PH} ⁴	Output Phase Accuracy		—	—	±0.05	UI
t _{OPJIT} ¹	Output Clock Period Jitter	f _{OUT} ≥ 100 MHz	—	—	±125	ps
		50 ≤ f _{OUT} < 100 MHz	—	—	0.025	UIPP
		f _{OUT} < 50 MHz	—	—	0.04	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t _W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t _{LOCK} ²	PLL Lock-in Time	Without external capacitor	—	—	150	μs
		With external capacitor ⁵	—	—	500	μs
t _{PA}	Programmable Delay Unit		85	130	360	ps
t _{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t _{FBKDLY}	External Feedback Delay		—	—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t _{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor ⁵	20	—	—	μs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.

6. $f_{OUT} (max) = f_{IN} * 10$ for $f_{IN} < 5$ MHz.

LatticeECP2 Power Supply and NC

Signals	144 TQFP ³	208 PQFP ³	256 fpBGA ⁴	484 fpBGA ⁴
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	LFE2-6: G7, G9, G10, H7, J10, K10, K8 LFE2-12/LFE2-20: G7, G9, G10, H7, J10, K10, K8	LFE2-12/LFE2-20: N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 LFE2-35/LFE2-50: J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	LFE2-12/LFE2-20: None LFE2-35: N6, N18 LFE2-50: N6, N18, K6, J16
GND ¹	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC ²	LFE2-6: 45, 46, 124, 127 LFE2-12: 127	None	LFE2-6: K6, R3, P4 LFE2-12/LFE2-20: None	LFE2-12: E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-20/LFE2-35: K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-50: None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J13	J13	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
J12	J12	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
H12	H12	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GND	GND	GNDIO3	-		
H13	H13	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
H15	H15	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO	VCCIO3	3		
H16	H16	PR22A	3	VREF1_3/RDQ25	T
H11	H11	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J11	J11	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
G16	G16	PR19B	2	PCLKC2_0/RDQ16	C
GND	GND	GNDIO2	-		
G15	G15	PR19A	2	PCLKT2_0/RDQ16	T
F15	F15	PR17B	2	RDQ16	C
G11	G11	PR18B	2	RDQ16	C (LVDS)*
F14	F14	PR17A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
F12	F12	PR18A	2	RDQ16	T (LVDS)*
G14	G14	PR16B	2	RDQ16	C (LVDS)*
G13	G13	PR16A	2	RDQS16	T (LVDS)*
GND	GND	GNDIO2	-		
F16	F16	PR14B	2	RDQ16	C (LVDS)*
F9	F9	PR15B	2	RDQ16	C
E16	E16	PR14A	2	RDQ16	T (LVDS)*
F10	F10	PR15A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
D16	D16	PR13B	2	RDQ16	C
D15	D15	PR13A	2	RDQ16	T
C15	C15	PR6B	2	RDQ8	C (LVDS)*
C16	C16	PR7B	2	RDQ8	C
GND	GND	GNDIO2	-		
D14	D14	PR6A	2	RDQ8	T (LVDS)*
B16	B16	PR7A	2	RDQ8	T
F13	F13	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO	VCCIO2	2		
E13	E13	PR2A	2	VREF1_2	T (LVDS)*
F11	F11	PT64B	1	VREF2_1	C
E11	E11	PT64A	1	VREF1_1	T
GND	GND	GNDIO1	-		
A15	A15	PT63B	1		C
E12	E12	PT62B	1		C
B15	B15	PT63A	1		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO1	-			GNDIO1	-		
C15	PT45B	1		C	PT45B	1		C
A15	PT45A	1		T	PT45A	1		T
A13	PT44B	1		C	PT44B	1		C
B13	PT44A	1		T	PT44A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
H17	PT43B	1		C	PT43B	1		C
H15	PT43A	1		T	PT43A	1		T
D13	PT42B	1		C	PT42B	1		C
C14	PT42A	1		T	PT42A	1		T
GND	GNDIO1	-			GNDIO1	-		
G14	PT41B	1		C	PT41B	1		C
E14	PT41A	1		T	PT41A	1		T
A12	PT40B	1		C	PT40B	1		C
B12	PT40A	1		T	PT40A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
F14	PT39B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C
D14	PT39A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T
H16	XRES	1			XRES	1		
H14	PT37B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GND	GNDIO0	-			GNDIO0	-		
H13	PT37A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
A11	PT36B	0		C	PT36B	0		C
B11	PT36A	0		T	PT36A	0		T
C13	PT35B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
E13	PT35A	0		T	PT35A	0		T
D12	PT34B	0		C	PT34B	0		C
F13	PT34A	0		T	PT34A	0		T
A10	PT33B	0		C	PT33B	0		C
B10	PT33A	0		T	PT33A	0		T
C12	PT32B	0		C	PT32B	0		C
GND	GNDIO0	-			GNDIO0	-		
C10	PT32A	0		T	PT32A	0		T
G13	PT31B	0		C	PT31B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
H12	PT31A	0		T	PT31A	0		T
A9	PT30B	0		C	PT30B	0		C
B9	PT30A	0		T	PT30A	0		T
E12	PT29B	0		C	PT29B	0		C
G12	PT29A	0		T	PT29A	0		T
A8	PT28B	0		C	PT28B	0		C
B8	PT28A	0		T	PT28A	0		T
GND	GNDIO0	-			GNDIO0	-		
E11	PT27B	0		C	PT27B	0		C
C9	PT27A	0		T	PT27A	0		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D4	PT7B	0		C	PT7B	0		C	
D3	PT7A	0		T	PT7A	0		T	
C2	PT6B	0		C	PT6B	0		C	
C1	PT6A	0		T	PT6A	0		T	
G8	PT5B	0		C	PT5B	0		C	
GND	GNDIO0	-			GNDIO0	-			
G7	PT5A	0		T	PT5A	0		T	
E7	PT4B	0		C	PT4B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT4A	0		T	PT4A	0		T	
E6	PT3B	0		C	PT3B	0		C	
E5	PT3A	0		T	PT3A	0		T	
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	
L12	VCC	-			VCC	-			
L13	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L15	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N16	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P16	VCC	-			VCC	-			
R11	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R15	VCC	-			VCC	-			
R16	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T13	VCC	-			VCC	-			
T14	VCC	-			VCC	-			
T15	VCC	-			VCC	-			
D11	VCCIO0	0			VCCIO0	0			
D6	VCCIO0	0			VCCIO0	0			
G9	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			
J12	VCCIO0	0			VCCIO0	0			
D16	VCCIO1	1			VCCIO1	1			
D21	VCCIO1	1			VCCIO1	1			
G18	VCCIO1	1			VCCIO1	1			
J15	VCCIO1	1			VCCIO1	1			
K15	VCCIO1	1			VCCIO1	1			
F23	VCCIO2	2			VCCIO2	2			
J20	VCCIO2	2			VCCIO2	2			

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
E21	PT76A	1		T
VCCIO	VCCIO1	1		
B22	PT75B	1		C
A22	PT75A	1		T
H20	PT74B	1		C
F21	PT74A	1		T
F20	PT73B	1		C
GND	GNDIO1	-		
H19	PT73A	1		T
D21	PT72B	1		C
C21	PT72A	1		T
E20	PT71B	1		C
VCCIO	VCCIO1	1		
G21	PT71A	1		T
B21	PT70B	1		C
A21	PT70A	1		T
F19	PT69B	1		C
G20	PT69A	1		T
E19	PT68B	1		C
GND	GNDIO1	-		
G19	PT68A	1		T
D20	PT67B	1		C
VCCIO	VCCIO1	1		
C20	PT67A	1		T
B20	PT66B	1		C
A20	PT66A	1		T
F18	PT65B	1		C
H18	PT65A	1		T
D19	PT64B	1		C
C19	PT64A	1		T
GND	GNDIO1	-		
G18	PT63B	1		C
E18	PT63A	1		T
H17	PT62B	1		C
F17	PT62A	1		T
VCCIO	VCCIO1	1		
G17	PT61B	1		C
E17	PT61A	1		T
B19	PT60B	1		C
A19	PT60A	1		T
GND	GNDIO1	-		
D17	PT59B	1		C
B18	PT59A	1		T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K26	PR26A	2	RDQ23	T
K23	PR25B	2	RDQ23	C (LVDS)*
K22	PR25A	2	RDQ23	T (LVDS)*
J22	PR24B	2	RDQ23	C
VCCIO	VCCIO2	2		
J23	PR24A	2	RDQ23	T
GNDIO	GNDIO2	-		
VCCIO	VCCIO2	2		
J26	PR17B	2	RDQ15	C (LVDS)*
H26	PR17A	2	RDQ15	T (LVDS)*
H27	PR16B	2	RDQ15	C
G26	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2		
H23	PR15B	2	RDQ15	C (LVDS)*
H24	PR15A	2	RDQS15	T (LVDS)*
D28	PR14B	2	RDQ15	C
GNDIO	GNDIO2	-		
E28	PR14A	2	RDQ15	T
G24	PR13B	2	RDQ15	C (LVDS)*
H25	PR13A	2	RDQ15	T (LVDS)*
D27	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
VCCIO	VCCIO2	2		
E27	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
F26	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*
G25	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
F24	PR9B	2	VREF2_2	C
-	-	-		
GNDIO	GNDIO2	-		
F25	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
G23	XRES	1		
C30	URC_SQ_VCCR0	12		
A29	URC_SQ_HDINP0	12		T
B30	URC_SQ_VCCIB0	12		
B29	URC_SQ_HDINN0	12		C
C27	URC_SQ_VCCTX0	12		
A26	URC_SQ_HDOUTP0	12		T
A27	URC_SQ_VCCOB0	12		
B26	URC_SQ_HDOUTN0	12		C
C26	URC_SQ_VCCTX1	12		
B25	URC_SQ_HDOUTN1	12		C
C25	URC_SQ_VCCOB1	12		
A25	URC_SQ_HDOUTP1	12		T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL} , I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT} .
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.