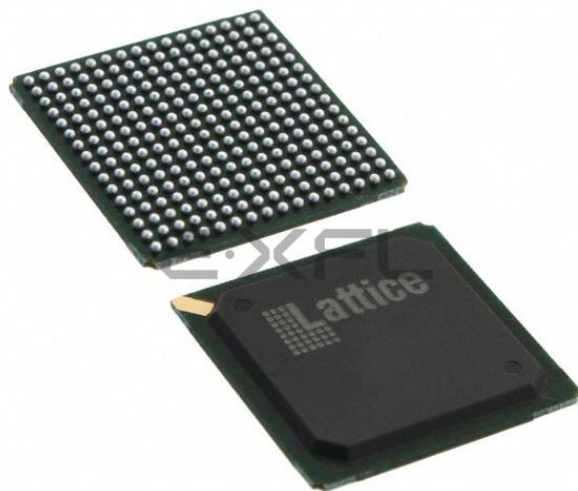




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

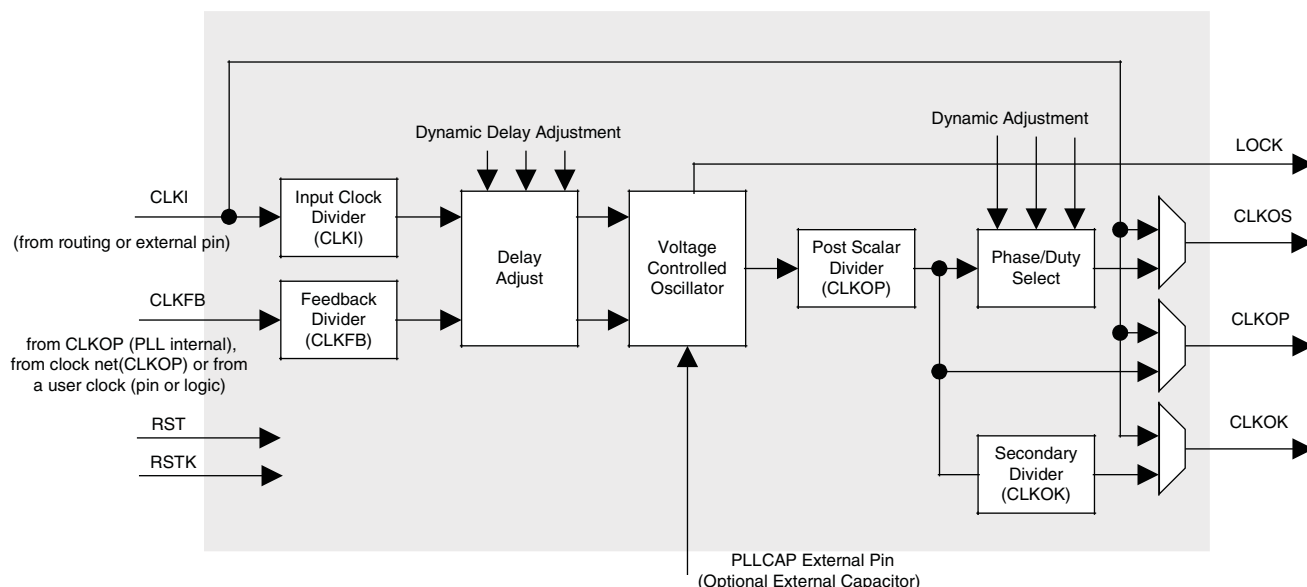
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20e-6f256c

Figure 2-5. General Purpose PLL (GPLL) Diagram



Standard PLL (SPLL)

Some of the larger devices have two to six Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see the list of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

Table 2-4. GPLL and SPLL Blocks Signal Descriptions

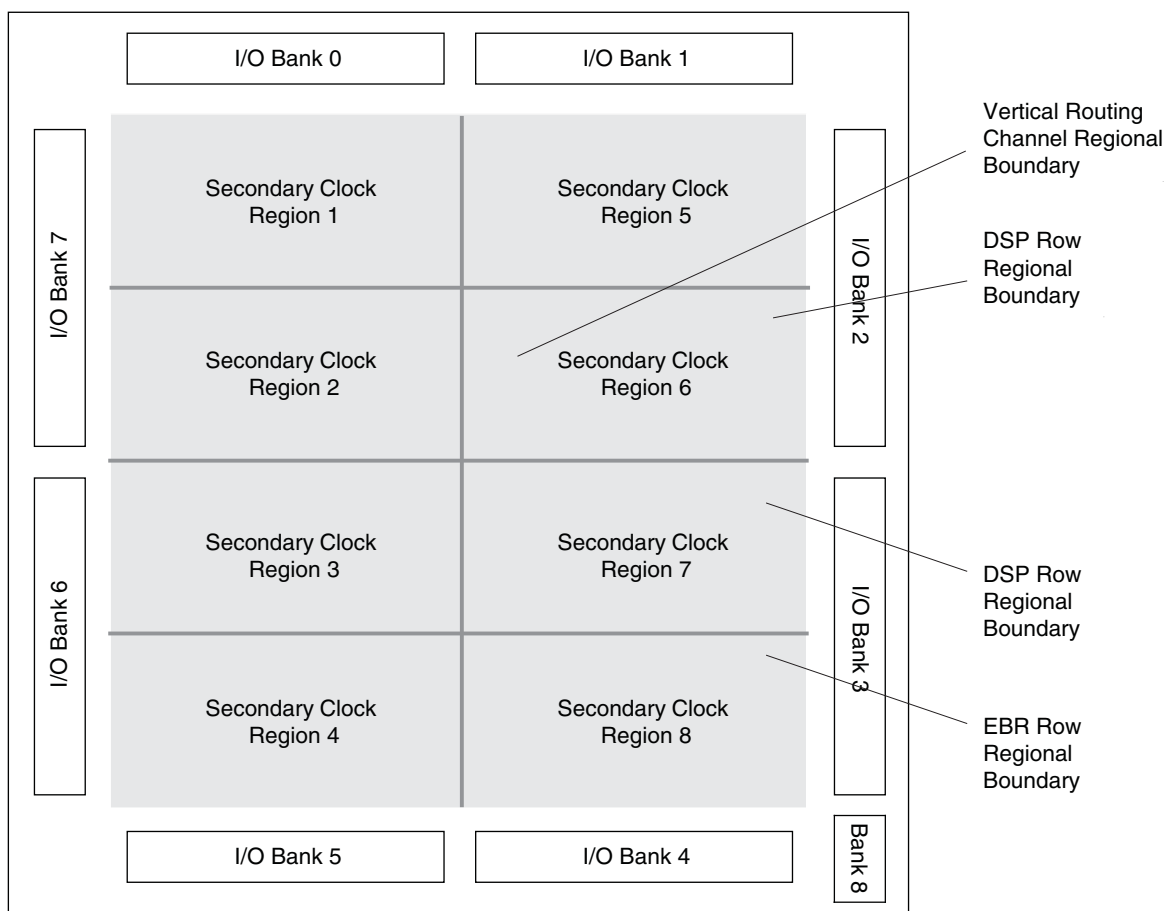
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE ¹	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR ¹	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG ¹	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0] ¹	I	Dynamic Delay Input
DPA MODES	I	DPA (Dynamic Phase Adjust/Duty Cycle Select) mode
DPHASE [3:0]	I	DPA Phase Adjust inputs
DDDUTY [3:0]	—	DPA Duty Cycle Select inputs

1. These signals are not available in SPLL.

this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

Figure 2-15. Secondary Clock Regions ECP2-50



By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

Figure 2-29. Input Register Block for Left, Right and Bottom Edges

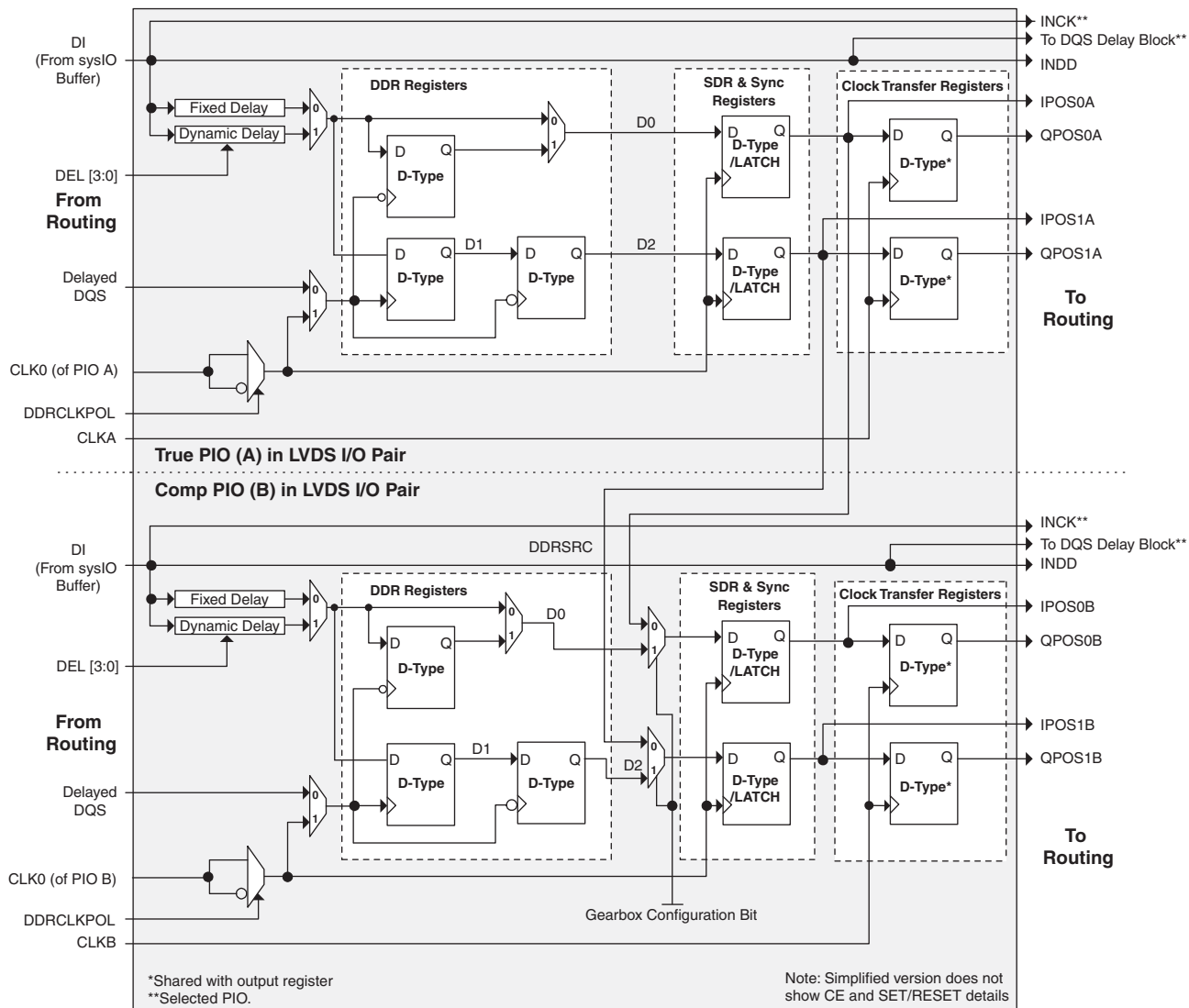
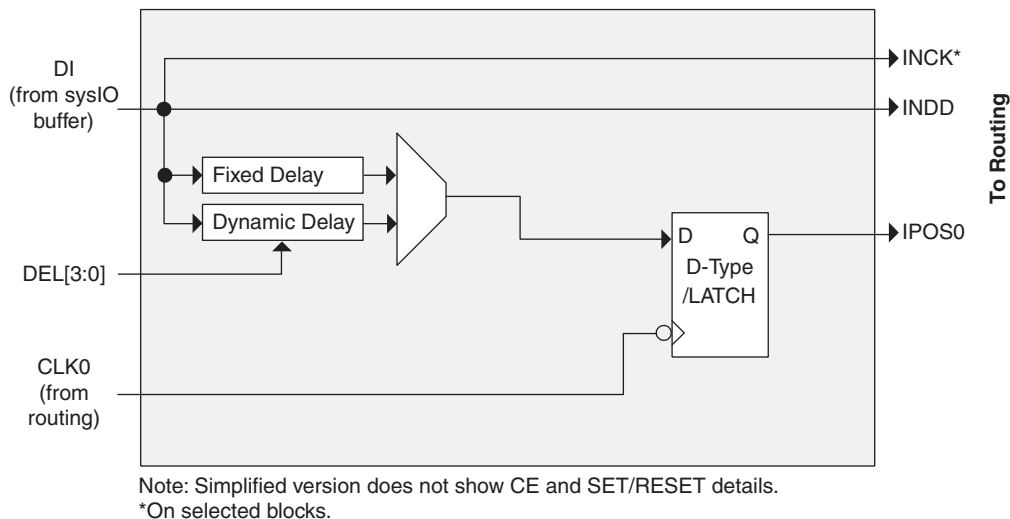


Figure 2-30. Input Register Block Top Edge



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the PIOs on the left, right and bottom contain a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-31 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-32 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining the output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams: ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-32 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{CLKOP}^1	Output clock frequency, CLKOP	100	—	500	MHz
f_{CLKOS}^2	Output clock frequency, CLKOS	25	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)		—	250	ps p-p
t_{CYJIT}	Output clock cycle to cycle jitter (clean input)			250	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	35		65	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	40		60	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode)	40		60	%
t_{SKEW}^3	Output clock to clock skew between two outputs with the same phase setting	—	—	100	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)	750	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)	750	—	—	ps
t_{INSTB}	Input clock period jitter	—	—	+/-250	ps
t_{LOCK}	DLL lock time	18,500	—	—	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)	3	—	—	ns
t_{PA}	Delay step size	16.5	42	59.4	ps
t_{RANGE1}	Max. delay setting for single delay block (144 taps)	2.376	6	8.553	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks	9.504	24	34.214	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
92	PB44A	4	BDQ42	T	PB54A	4	BDQ51	T	
93	VCCIO4	4			VCCIO4	4			
94	PB44B	4	BDQ42	C	PB54B	4	BDQ51	C	
95	PB48A	4	BDQ51	T	PB58A	4	BDQ60	T	
96	PB48B	4	BDQ51	C	PB58B	4	BDQ60	C	
97	VCC	-			VCC	-			
98	PB52A	4	BDQ51	T	PB60A	4	BDQS60	T	
99	PB52B	4	BDQ51	C	PB60B	4	BDQ60	C	
100	VCCIO4	4			VCCIO4	4			
101	PB54A	4	BDQ51		PB63A	4	BDQ60		
102	GND	-			GND	-			
103	PB55A	4	VREF2_4/BDQ51	T	PB64A	4	VREF2_4/BDQ60	T	
104	PB55B	4	VREF1_4/BDQ51	C	PB64B	4	VREF1_4/BDQ60	C	
105	CFG1	8			CFG1	8			
106	PROGRAMN	8			PROGRAMN	8			
107	CFG2	8			CFG2	8			
108	INITN	8			INITN	8			
109	CFG0	8			CFG0	8			
110	CCLK	8			CCLK	8			
111	DONE	8			DONE	8			
112	PR29A	8	D0/SPIFASTN		PR43A	8	D0/SPIFASTN		
113	VCCIO8	8			VCCIO8	8			
114	PR26A	8	D6		PR40A	8	D6		
115	GND	-			GND	-			
116	VCC	-			VCC	-			
117	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C	
118	VCCIO8	8			VCCIO8	8			
119	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T	
120	PR24B	8	DOU/CSON	C	PR38B	8	DOU/CSON	C	
121	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T	
122	GND	-			GND	-			
123	VCCIO3	3			VCCIO3	3			
124	PR21A	3	RLM0_GPLLT_FB_A		PR31A	3	RLM0_GPLLT_FB_A/RDQ34		
125	VCCAUX	-			VCCAUX	-			
126	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*	
127	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLL_T_IN_A**/RDQ34	T (LVDS)*	
128	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
129	VCC	-			VCC	-			
130	PR18B	3	RLM0_GDLL_C_FB_A	C	PR28B	3	RLM0_GDLL_C_FB_A/RDQ25	C	
131	PR18A	3	RLM0_GDLL_T_FB_A	T	PR28A	3	RLM0_GDLL_T_FB_A/RDQ25	T	
132	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLL_C_IN_A**/RDQ25	C (LVDS)*	
133	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLL_T_IN_A**/RDQ25	T (LVDS)*	
134	PR16B	3	VREF2_3	C	PR22B	3	VREF2_3/RDQ25	C	
135	VCCIO3	3			VCCIO3	3			
136	PR16A	3	VREF1_3	T	PR22A	3	VREF1_3/RDQ25	T	
137	PR15B	3	PCLKC3_0	C (LVDS)*	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*	

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C2	PT3A	0		T	PT3A	0		T	
J10	VCC	-			VCC	-			
J11	VCC	-			VCC	-			
J12	VCC	-			VCC	-			
J13	VCC	-			VCC	-			
K14	VCC	-			VCC	-			
K9	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L9	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M9	VCC	-			VCC	-			
N14	VCC	-			VCC	-			
N9	VCC	-			VCC	-			
P10	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P13	VCC	-			VCC	-			
G10	VCCIO0	0			VCCIO0	0			
G9	VCCIO0	0			VCCIO0	0			
H9	VCCIO0	0			VCCIO0	0			
H8	VCCIO0	0			VCCIO0	0			
G11	VCCIO1	1			VCCIO1	1			
G12	VCCIO1	1			VCCIO1	1			
G13	VCCIO1	1			VCCIO1	1			
G14	VCCIO1	1			VCCIO1	1			
H14	VCCIO2	2			VCCIO2	2			
H15	VCCIO2	2			VCCIO2	2			
J15	VCCIO2	2			VCCIO2	2			
K16	VCCIO2	2			VCCIO2	2			
L16	VCCIO3	3			VCCIO3	3			
M16	VCCIO3	3			VCCIO3	3			
N16	VCCIO3	3			VCCIO3	3			
P16	VCCIO3	3			VCCIO3	3			
R14	VCCIO4	4			VCCIO4	4			
T12	VCCIO4	4			VCCIO4	4			
T13	VCCIO4	4			VCCIO4	4			
T14	VCCIO4	4			VCCIO4	4			
R9	VCCIO5	5			VCCIO5	5			
T10	VCCIO5	5			VCCIO5	5			
T11	VCCIO5	5			VCCIO5	5			
T9	VCCIO5	5			VCCIO5	5			
N7	VCCIO6	6			VCCIO6	6			
P7	VCCIO6	6			VCCIO6	6			
P8	VCCIO6	6			VCCIO6	6			

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C	
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T	
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C	
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T	
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T	
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C	
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T	
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	NC	-			PB56A	4	BDQ60	T	
W17	NC	-			PB56B	4	BDQ60	C	
Y19	NC	-			PB57A	4	BDQ60	T	
Y17	NC	-			PB57B	4	BDQ60	C	
AF20	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	NC	-			NC	-			
AA20	NC	-			NC	-			
W18	NC	-			NC	-			
AD20	NC	-			NC	-			
GND	GNDIO4	-			GNDIO4	-			
AE21	NC	-			NC	-			
AF21	NC	-			NC	-			
AF22	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	GND	-			GND	-		
A25	GND	-			GND	-		
AA18	GND	-			GND	-		
AA24	GND	-			GND	-		
AA3	GND	-			GND	-		
AA9	GND	-			GND	-		
AD11	GND	-			GND	-		
AD16	GND	-			GND	-		
AD21	GND	-			GND	-		
AD6	GND	-			GND	-		
AE1	GND	-			GND	-		
AE26	GND	-			GND	-		
AF2	GND	-			GND	-		
AF25	GND	-			GND	-		
B1	GND	-			GND	-		
B26	GND	-			GND	-		
C11	GND	-			GND	-		
C16	GND	-			GND	-		
C21	GND	-			GND	-		
C6	GND	-			GND	-		
F18	GND	-			GND	-		
F24	GND	-			GND	-		
F3	GND	-			GND	-		
F9	GND	-			GND	-		
J13	GND	-			GND	-		
J14	GND	-			GND	-		
J21	GND	-			GND	-		
J6	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K13	GND	-			GND	-		
K14	GND	-			GND	-		
K16	GND	-			GND	-		
K17	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L24	GND	-			GND	-		
L3	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
G10	VCCPLL	-			VCCPLL	-		
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
E7	VCCIO0	0			VCCIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
E10	VCCIO1	1			VCCIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
VCCIO	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
VCCIO	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
VCCIO	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
VCCIO	VCCIO8	8			VCCIO8	8		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A15	GND	-			GND	-		
A16	GND	-			GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	NC	-			NC	-		
F14	NC	-			NC	-		
F13	NC	-			NC	-		
G12	NC	-			NC	-		
G13	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C6	PT12B	0		C	PT12B	0		C	
F10	PT12A	0		T	PT12A	0		T	
D7	PT11B	0		C	PT11B	0		C	
H11	PT11A	0		T	PT11A	0		T	
D5	PT10B	0		C	PT10B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E6	PT10A	0		T	PT10A	0		T	
G10	PT9B	0		C	PT9B	0		C	
F9	PT9A	0		T	PT9A	0		T	
H10	PT8B	0		C	PT8B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
E7	PT8A	0		T	PT8A	0		T	
B3	PT7B	0		C	PT7B	0		C	
C5	PT7A	0		T	PT7A	0		T	
B2	PT6B	0		C	PT6B	0		C	
C4	PT6A	0		T	PT6A	0		T	
G9	PT5B	0		C	PT5B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F7	PT5A	0		T	PT5A	0		T	
C3	PT4B	0		C	PT4B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
D4	PT4A	0		T	PT4A	0		T	
J10	PT3B	0		C	PT3B	0		C	
F8	PT3A	0		T	PT3A	0		T	
G8	PT2B	0		C	PT2B	0		C	
G7	PT2A	0		T	PT2A	0		T	
L12	VCC	-			VCC	-			
L13	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L15	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N16	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P16	VCC	-			VCC	-			
R11	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R15	VCC	-			VCC	-			
R16	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T13	VCC	-			VCC	-			
T14	VCC	-			VCC	-			
T15	VCC	-			VCC	-			
B12	VCCIO0	0			VCCIO0	0			
B7	VCCIO0	0			VCCIO0	0			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
VCCIO	VCCIO7	7			VCCIO7	7		
T6	PL44A	7	LDQ46	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*
R6	PL44B	7	LDQ46	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*
U9	PL45A	7	LDQ46	T	PL53A	7	LDQ54	T
T7	PL45B	7	LDQ46	C	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-			GNDIO7	-		
U5	PL46A	7	LDQS46	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*
U6	PL46B	7	LDQ46	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*
U7	PL47A	7	LDQ46	T	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7			VCCIO7	7		
V9	PL47B	7	LDQ46	C	PL55B	7	LDQ54	C
V11	PL48A	7	LDQ46	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*
V10	PL48B	7	LDQ46	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*
U4	PL49A	7	PCLKT7_0/LDQ46	T	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-			GNDIO7	-		
U3	PL49B	7	PCLKC7_0/LDQ46	C	PL57B	7	PCLKC7_0/LDQ54	C
U2	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
U1	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
V5	PL52A	6	VREF2_6/LDQ55	T	PL60A	6	VREF2_6/LDQ63	T
V6	PL52B	6	VREF1_6/LDQ55	C	PL60B	6	VREF1_6/LDQ63	C
V7	PL53A	6	LDQ55	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V8	PL53B	6	LDQ55	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*
V4	PL54A	6	LDQ55	T	PL62A	6	LDQ63	T
V3	PL54B	6	LDQ55	C	PL62B	6	LDQ63	C
V2	PL55A	6	LDQS55	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
V1	PL55B	6	LDQ55	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*
W7	PL56A	6	LDQ55	T	PL64A	6	LDQ63	T
W5	PL56B	6	LDQ55	C	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6			VCCIO6	6		
W2	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	PL65A	6	LLM4_SPLLT_IN_A/LDQ63	T (LVDS)*
W1	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*	PL65B	6	LLM4_SPLLC_IN_A/LDQ63	C (LVDS)*
Y6	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T	PL66A	6	LLM4_SPLLT_FB_A/LDQ63	T
W6	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C	PL66B	6	LLM4_SPLLC_FB_A/LDQ63	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL60A	6	LDQ64	T (LVDS)*	PL68A	6	LDQ72	T (LVDS)*
Y2	PL60B	6	LDQ64	C (LVDS)*	PL68B	6	LDQ72	C (LVDS)*
Y7	PL61A	6	LDQ64	T	PL69A	6	LDQ72	T
Y5	PL61B	6	LDQ64	C	PL69B	6	LDQ72	C
VCCIO	VCCIO6	6			VCCIO6	6		
W10	PL62A	6	LDQ64	T (LVDS)*	PL70A	6	LDQ72	T (LVDS)*
Y8	PL62B	6	LDQ64	C (LVDS)*	PL70B	6	LDQ72	C (LVDS)*
Y4	PL63A	6	LDQ64	T	PL71A	6	LDQ72	T
Y3	PL63B	6	LDQ64	C	PL71B	6	LDQ72	C
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL64A	6	LDQS64	T (LVDS)*	PL72A	6	LDQS72	T (LVDS)*
AA2	PL64B	6	LDQ64	C (LVDS)*	PL72B	6	LDQ72	C (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF27	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
AF28	PR85B	3	RLM0_GDLLC_FB_A	C	PR102B	3	RLM0_GDLLC_FB_A/RDQ99	C
GNDIO	GNDIO3	-			GNDIO3	-		
AD26	PR85A	3	RLM0_GDLLT_FB_A	T	PR102A	3	RLM0_GDLLT_FB_A/RDQ99	T
AJ32	PR84B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR101B	3	RLM0_GDLLC_IN_A**/ RDQ99	C (LVDS)*
AJ33	PR84A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR101A	3	RLM0_GDLLT_IN_A**/ RDQ99	T (LVDS)*
AJ34	PR83B	3	RLM0_GPLLC_IN_A**	C	PR100B	3	RLM0_GPLLC_IN_A**/ RDQ99	C
VCCIO	VCCIO3	3			VCCIO3	3		
AK34	PR83A	3	RLM0_GPLLT_IN_A**	T	PR100A	3	RLM0_GPLLT_IN_A**/ RDQ99	T
AH33	PR82B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR99B	3	RLM0_GPLLC_FB_A/RDQ99	C (LVDS)*
AH34	PR82A	3	RLM0_GPLLT_FB_A/RDQS82****	T (LVDS)*	PR99A	3	RLM0_GPLLT_FB_A/ RDQS99	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
AF29	PR81B	3	RDQ82	C	PR98B	3	RDQ99	C
AF31	PR81A	3	RDQ82	T	PR98A	3	RDQ99	T
AG33	PR80B	3	RDQ82	C (LVDS)*	PR97B	3	RDQ99	C (LVDS)*
AG34	PR80A	3	RDQ82	T (LVDS)*	PR97A	3	RDQ99	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
AF30	PR79B	3	RDQ82	C	PR96B	3	RDQ99	C
AF32	PR79A	3	RDQ82	T	PR96A	3	RDQ99	T
AE29	PR78B	3	RDQ82	C (LVDS)*	PR95B	3	RDQ99	C (LVDS)*
AE30	PR78A	3	RDQ82	T (LVDS)*	PR95A	3	RDQ99	T (LVDS)*
AF33	NC	-			PR93B	3	RDQ90	C
AF34	NC	-			PR93A	3	RDQ90	T
-	-	-			GNDIO3	-		
AC27	NC	-			PR92B	3	RDQ90	C (LVDS)*
AC28	NC	-			PR92A	3	RDQ90	T (LVDS)*
AD29	NC	-			PR91B	3	RDQ90	C
AD30	NC	-			PR91A	3	RDQ90	T
-	-	-			VCCIO3	3		
AE33	NC	-			PR90B	3	RDQ90	C (LVDS)*
AE34	NC	-			PR90A	3	RDQS90	T (LVDS)*
AD32	NC	-			PR89B	3	RDQ90	C
-	-	-			GNDIO3	-		
AD31	NC	-			PR89A	3	RDQ90	T
AB25	NC	-			PR88B	3	RDQ90	C (LVDS)*
AC25	NC	-			PR88A	3	RDQ90	T (LVDS)*
AB28	NC	-			PR87B	3	RDQ90	C
-	-	-			VCCIO3	3		
AA26	NC	-			PR87A	3	RDQ90	T
AD33	NC	-			PR86B	3	RDQ90	C (LVDS)*
AD34	NC	-			PR86A	3	RDQ90	T (LVDS)*
AC29	PR76B	3	RDQ73	C	PR84B	3	RDQ81	C
GNDIO	GNDIO3	-			GNDIO3	-		
AA27	PR76A	3	RDQ73	T	PR84A	3	RDQ81	T
AC32	PR75B	3	RDQ73	C (LVDS)*	PR83B	3	RDQ81	C (LVDS)*
AC31	PR75A	3	RDQ73	T (LVDS)*	PR83A	3	RDQ81	T (LVDS)*

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484I	304	1.2V	-5	fpBGA	484	Ind	20
LFE2M20SE-6F484I	304	1.2V	-6	fpBGA	484	Ind	20
LFE2M20SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	20
LFE2M20SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672I	410	1.2V	-5	fpBGA	672	Ind	35
LFE2M35SE-6F672I	410	1.2V	-6	fpBGA	672	Ind	35
LFE2M35SE-5F484I	303	1.2V	-5	fpBGA	484	Ind	35
LFE2M35SE-6F484I	303	1.2V	-6	fpBGA	484	Ind	35
LFE2M35SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	35
LFE2M35SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900I	410	1.2V	-5	fpBGA	900	Ind	50
LFE2M50SE-6F900I	410	1.2V	-6	fpBGA	900	Ind	50
LFE2M50SE-5F672I	372	1.2V	-5	fpBGA	672	Ind	50
LFE2M50SE-6F672I	372	1.2V	-6	fpBGA	672	Ind	50
LFE2M50SE-5F484I	270	1.2V	-5	fpBGA	484	Ind	50
LFE2M50SE-6F484I	270	1.2V	-6	fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152I	436	1.2V	-5	fpBGA	1152	Ind	70
LFE2M70SE-6F1152I	436	1.2V	-6	fpBGA	1152	Ind	70
LFE2M70SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	70
LFE2M70SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152I	520	1.2V	-5	fpBGA	1152	Ind	100
LFE2M100SE-6F1152I	520	1.2V	-6	fpBGA	1152	Ind	100
LFE2M100SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	100
LFE2M100SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	100