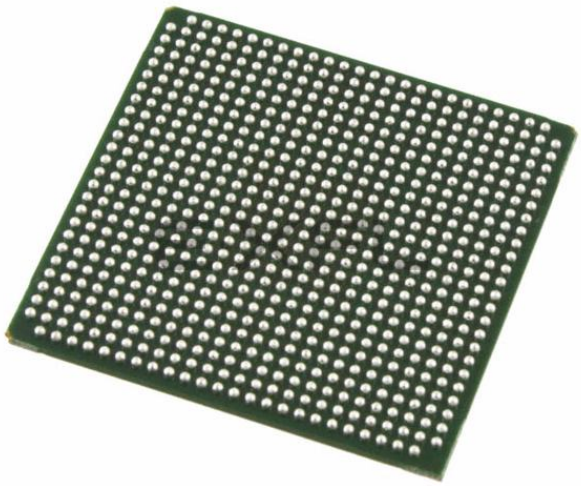
# Lattice Semiconductor Corporation - LFE2-20E-6FN672C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

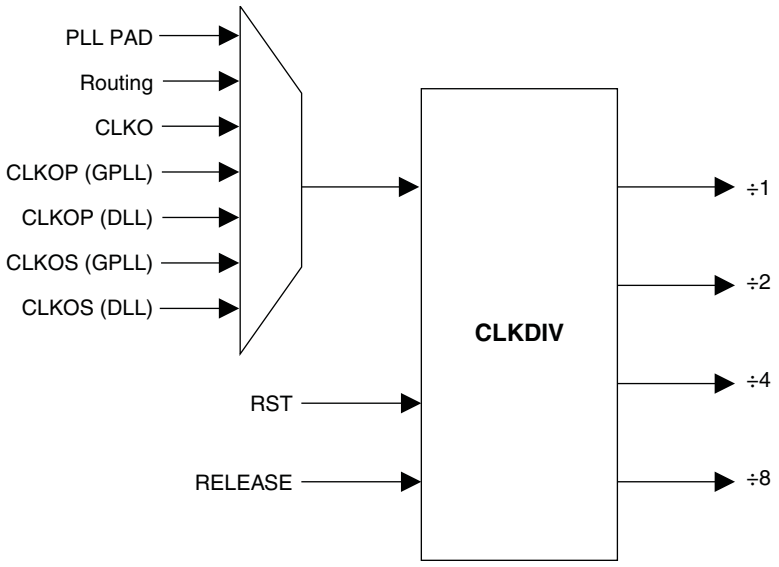
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2625 |
| Number of Logic Elements/Cells | 21000 |
| Total RAM Bits | 282624 |
| Number of I/O | 402 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20e-6fn672c |

*Figure 2-9. Clock Divider Connections*




## Clock Distribution Network

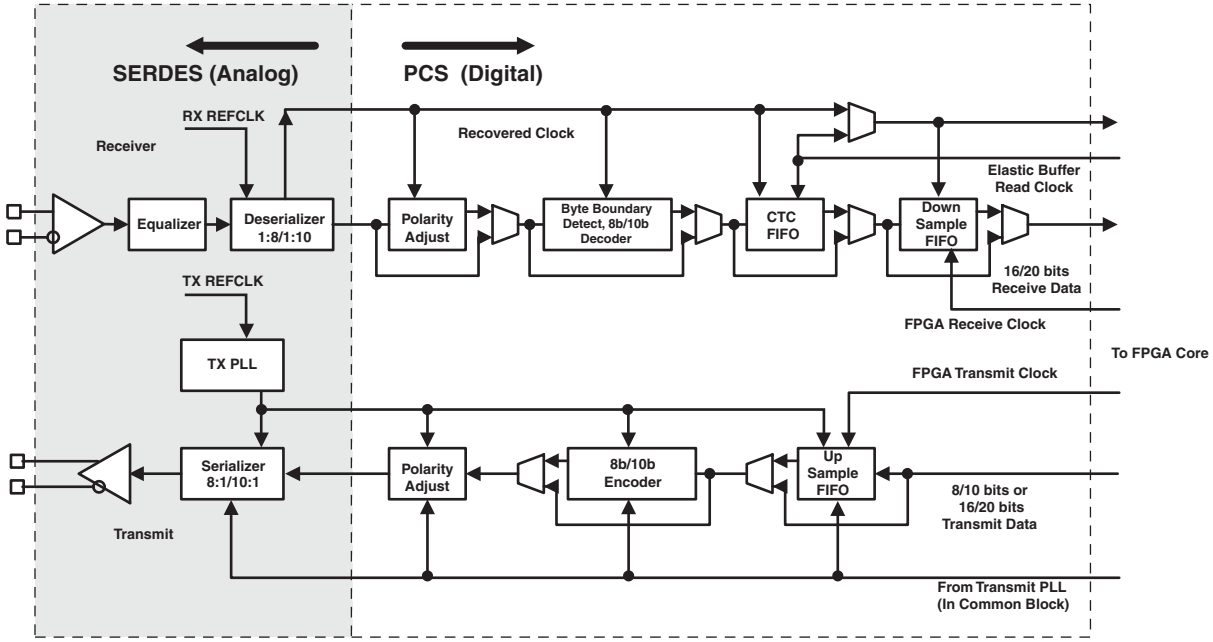
LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

### Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

Each Transmit and Receive channel has its independent power supplies. The Output and Input buffers of each channel also have their own independent power supplies. In addition, there are separate power supplies for PLL, terminating resistor per quad.

***Figure 2-40. Simplified Channel Block Diagram for SERDES and PCS***




## PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer receivers and adjusts the polarity, detects, byte boundary, decodes (8b/10b) and provides Clock Tolerance Compensation (CTC) FIFO for changing the clock domain from receiver clock to the FPGA Clock.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, adjusts the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

## SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is a soft IP interface that allow the SERDES/PCS Quad block to be controlled by registers as opposed to the configuration memory cells. It is a simple register configuration interface.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With Diamond, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet and x4 PCI-Express and 4x Serial RapidIO can be implemented using IP (provided by Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

For further information about SERDES, please see the list of additional technical documentation at the end of this data sheet.

## sysI/O Recommended Operating Conditions

| Standard | $V_{CCIO}$ | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| LVCMOS 2.5[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVCMOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVCMOS 1.2[2] | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18[2] Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL2[2] Class I, II | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL3[2] Class I, II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL[2] 15 Class I | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL[2] 18 Class I, II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| LVDS[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| MLVDS25[1] | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL33[1, 2] | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS25[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS[1, 2] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL18D_I[2], II[2] | 1.71 | 1.8 | 1.89 | — | — | — |
| SSTL25D_ I[2], II[2] | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL33D_ I[2], II[2] | 3.135 | 3.3 | 3.465 | — | — | — |
| HSTL15D_ I[2] | 1.425 | 1.5 | 1.575 | — | — | — |
| HSTL18D_ I[2], II[2] | 1.71 | 1.8 | 1.89 | — | — | — |

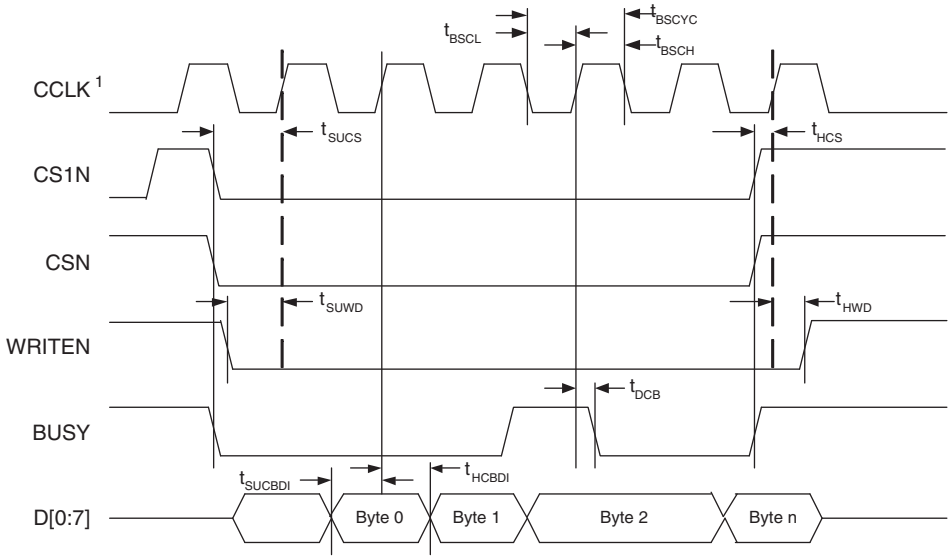
1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of $V_{CCIO}$.

*Table 3-13. Periodic Receiver Jitter Tolerance Specification[1]*

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Periodic | 3.125 Gbps | 600 mV differential eye | — | — | 0.20 | UI, p-p |
| | 2.5 Gbps | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| | 1.25 Gbps | 600 mV differential eye | — | — | 0.20 | UI, p-p |
| | 250 Mbps[2] | 600 mV differential eye | — | — | 0.08 | UI, p-p |

1. Values are measured with PRBS $2^7$-1, all channels operating.
2. Jitter specification is limited by measurement equipment capability.

*Figure 3-15. sysCONFIG Parallel Port Write Cycle*




1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

*Figure 3-16. sysCONFIG Slave Serial Port Timing*

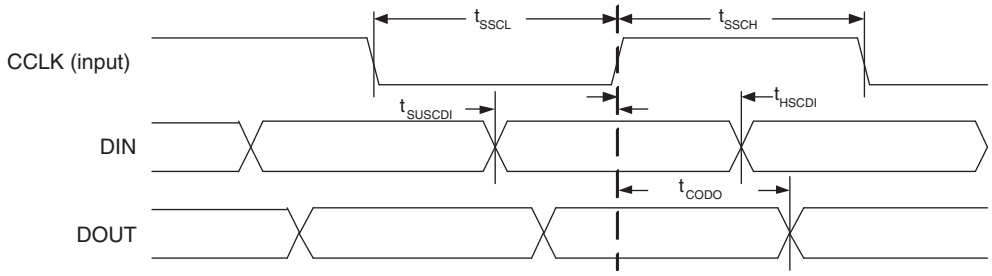
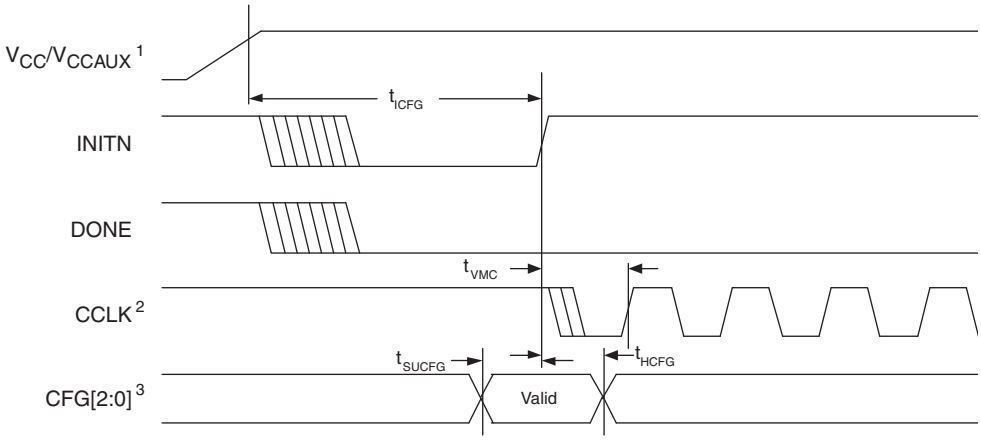



*Figure 3-17. Power-On-Reset (POR) Timing*




1. Time taken from $V_{CC}$ or $V_{CCAUX}$, whichever is the last to reach its $V_{MIN}$.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F15 | PR11B | 2 | RDQ10 | C | PR11B | 2 | RDQ10 | C |
| G11 | PR12B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ10 | C (LVDS)* |
| F14 | PR11A | 2 | RDQ10 | T | PR11A | 2 | RDQ10 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F12 | PR12A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ10 | T (LVDS)* |
| G14 | PR10B | 2 | RDQ10 | C (LVDS)* | PR10B | 2 | RDQ10 | C (LVDS)* |
| G13 | PR10A | 2 | RDQS10 | T (LVDS)* | PR10A | 2 | RDQS10 | T (LVDS)* |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| F16 | PR8B | 2 | RDQ10 | C (LVDS)* | PR8B | 2 | RDQ10 | C (LVDS)* |
| F9 | PR9B | 2 | RDQ10 | C | PR9B | 2 | RDQ10 | C |
| E16 | PR8A | 2 | RDQ10 | T (LVDS)* | PR8A | 2 | RDQ10 | T (LVDS)* |
| F10 | PR9A | 2 | RDQ10 | T | PR9A | 2 | RDQ10 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| D16 | PR7B | 2 | RDQ10 | C | PR7B | 2 | RDQ10 | C |
| D15 | PR7A | 2 | RDQ10 | T | PR7A | 2 | RDQ10 | T |
| C15 | PR4B | 2 | | C (LVDS)* | PR4B | 2 | | C (LVDS)* |
| C16 | PR5B | 2 | | C | PR5B | 2 | | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D14 | PR4A | 2 | | T (LVDS)* | PR4A | 2 | | T (LVDS)* |
| B16 | PR5A | 2 | | T | PR5A | 2 | | T |
| F13 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| E13 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| F11 | PT28B | 1 | VREF2_1 | C | PT55B | 1 | VREF2_1 | C |
| E11 | PT28A | 1 | VREF1_1 | T | PT55A | 1 | VREF1_1 | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A15 | PT27B | 1 | | C | PT54B | 1 | | C |
| E12 | PT26B | 1 | | C | PT53B | 1 | | C |
| B15 | PT27A | 1 | | T | PT54A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D12 | PT26A | 1 | | T | PT53A | 1 | | T |
| B14 | PT25B | 1 | | C | PT52B | 1 | | C |
| C14 | PT24B | 1 | | C | PT51B | 1 | | C |
| A14 | PT25A | 1 | | T | PT52A | 1 | | T |
| D13 | PT24A | 1 | | T | PT51A | 1 | | T |
| C13 | PT23B | 1 | | C | PT50B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A13 | PT22B | 1 | | C | PT49B | 1 | | C |
| B13 | PT23A | 1 | | T | PT50A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A12 | PT22A | 1 | | T | PT49A | 1 | | T |
| B11 | PT21B | 1 | | C | PT48B | 1 | | C |
| D11 | PT20B | 1 | | C | PT47B | 1 | | C |
| A11 | PT21A | 1 | | T | PT48A | 1 | | T |
| C11 | PT20A | 1 | | T | PT47A | 1 | | T |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AE17 | PB51B | 4 | BDQ51 | C | PB51B | 4 | BDQ51 | C |
| AB19 | PB52A | 4 | BDQ51 | T | PB52A | 4 | BDQ51 | T |
| AE19 | PB52B | 4 | BDQ51 | C | PB52B | 4 | BDQ51 | C |
| AF17 | PB53A | 4 | BDQ51 | T | PB53A | 4 | BDQ51 | T |
| AE18 | PB53B | 4 | BDQ51 | C | PB53B | 4 | BDQ51 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W16 | PB54A | 4 | BDQ51 | T | PB54A | 4 | BDQ51 | T |
| AA17 | PB54B | 4 | BDQ51 | C | PB54B | 4 | BDQ51 | C |
| AF18 | PB55A | 4 | BDQ51 | T | PB55A | 4 | BDQ51 | T |
| AF19 | PB55B | 4 | BDQ51 | C | PB55B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AA19 | NC | - | | | PB56A | 4 | BDQ60 | T |
| W17 | NC | - | | | PB56B | 4 | BDQ60 | C |
| Y19 | NC | - | | | PB57A | 4 | BDQ60 | T |
| Y17 | NC | - | | | PB57B | 4 | BDQ60 | C |
| AF20 | NC | - | | | NC | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AE20 | NC | - | | | NC | - | | |
| AA20 | NC | - | | | NC | - | | |
| W18 | NC | - | | | NC | - | | |
| AD20 | NC | - | | | NC | - | | |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE21 | NC | - | | | NC | - | | |
| AF21 | NC | - | | | NC | - | | |
| AF22 | NC | - | | | NC | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AE22 | PB56A | 4 | BDQ60 | T | PB65A | 4 | BDQ69 | T |
| AD22 | PB56B | 4 | BDQ60 | C | PB65B | 4 | BDQ69 | C |
| AF23 | PB57A | 4 | BDQ60 | T | PB66A | 4 | BDQ69 | T |
| AE23 | PB57B | 4 | BDQ60 | C | PB66B | 4 | BDQ69 | C |
| AD23 | PB58A | 4 | BDQ60 | T | PB67A | 4 | BDQ69 | T |
| AC23 | PB58B | 4 | BDQ60 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB20 | PB59A | 4 | BDQ60 | T | PB68A | 4 | BDQ69 | T |
| AC20 | PB59B | 4 | BDQ60 | C | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| AB21 | PB60A | 4 | BDQS60 | T | PB69A | 4 | BDQS69 | T |
| AC22 | PB60B | 4 | BDQ60 | C | PB69B | 4 | BDQ69 | C |
| W19 | PB61A | 4 | BDQ60 | T | PB70A | 4 | BDQ69 | T |
| AA21 | PB61B | 4 | BDQ60 | C | PB70B | 4 | BDQ69 | C |
| AF24 | PB62A | 4 | BDQ60 | T | PB71A | 4 | BDQ69 | T |
| AE24 | PB62B | 4 | BDQ60 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y20 | PB63A | 4 | BDQ60 | T | PB72A | 4 | BDQ69 | T |
| AB22 | PB63B | 4 | BDQ60 | C | PB72B | 4 | BDQ69 | C |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C20 | PT57B | 1 | | C | PT66B | 1 | | C |
| D20 | PT57A | 1 | | T | PT66A | 1 | | T |
| A22 | PT56B | 1 | | C | PT65B | 1 | | C |
| A21 | PT56A | 1 | | T | PT65A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E19 | NC | - | | | NC | - | | |
| C19 | NC | - | | | NC | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B21 | NC | - | | | NC | - | | |
| B20 | NC | - | | | NC | - | | |
| D19 | NC | - | | | NC | - | | |
| B19 | NC | - | | | NC | - | | |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | NC | - | | | NC | - | | |
| E18 | NC | - | | | NC | - | | |
| G19 | NC | - | | | NC | - | | |
| F17 | NC | - | | | NC | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A20 | NC | - | | | NC | - | | |
| A19 | NC | - | | | NC | - | | |
| E17 | NC | - | | | NC | - | | |
| D18 | NC | - | | | NC | - | | |
| B18 | PT55B | 1 | | C | PT55B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A18 | PT55A | 1 | | T | PT55A | 1 | | T |
| E16 | PT54B | 1 | | C | PT54B | 1 | | C |
| G16 | PT54A | 1 | | T | PT54A | 1 | | T |
| F16 | PT53B | 1 | | C | PT53B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H18 | PT53A | 1 | | T | PT53A | 1 | | T |
| A17 | PT52B | 1 | | C | PT52B | 1 | | C |
| B17 | PT52A | 1 | | T | PT52A | 1 | | T |
| C18 | PT51B | 1 | | C | PT51B | 1 | | C |
| B16 | PT51A | 1 | | T | PT51A | 1 | | T |
| C17 | PT50B | 1 | | C | PT50B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D17 | PT50A | 1 | | T | PT50A | 1 | | T |
| E15 | PT49B | 1 | | C | PT49B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G15 | PT49A | 1 | | T | PT49A | 1 | | T |
| A16 | PT48B | 1 | | C | PT48B | 1 | | C |
| B15 | PT48A | 1 | | T | PT48A | 1 | | T |
| D15 | PT47B | 1 | | C | PT47B | 1 | | C |
| F15 | PT47A | 1 | | T | PT47A | 1 | | T |
| A14 | PT46B | 1 | | C | PT46B | 1 | | C |
| B14 | PT46A | 1 | | T | PT46A | 1 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U1 | PL53A | 6 | LDQ50 | T | PL66A | 6 | LDQ63 | T |
| V1 | PL53B | 6 | LDQ50 | C | PL66B | 6 | LDQ63 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| P3 | PL54A | 6 | LDQ58 | T (LVDS)* | PL67A | 6 | LDQ71 | T (LVDS)* |
| R3 | PL54B | 6 | LDQ58 | C (LVDS)* | PL67B | 6 | LDQ71 | C (LVDS)* |
| R4 | PL55A | 6 | LDQ58 | T | PL68A | 6 | LDQ71 | T |
| U2 | PL55B | 6 | LDQ58 | C | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V2 | PL56A | 6 | LDQ58 | T (LVDS)* | PL69A | 6 | LDQ71 | T (LVDS)* |
| W2 | PL56B | 6 | LDQ58 | C (LVDS)* | PL69B | 6 | LDQ71 | C (LVDS)* |
| T6 | PL57A | 6 | LDQ58 | T | PL70A | 6 | LDQ71 | T |
| R5 | PL57B | 6 | LDQ58 | C | PL70B | 6 | LDQ71 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R6 | PL58A | 6 | LDQS58 | T (LVDS)* | PL71A | 6 | LDQS71 | T (LVDS)* |
| R7 | PL58B | 6 | LDQ58 | C (LVDS)* | PL71B | 6 | LDQ71 | C (LVDS)* |
| W1 | PL59A | 6 | LDQ58 | T | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL59B | 6 | LDQ58 | C | PL72B | 6 | LDQ71 | C |
| Y1 | PL60A | 6 | LLM0_GDLLT_IN_A**/LDQ58 | T (LVDS)* | PL73A | 6 | LLM0_GDLLT_IN_A**/LDQ71 | T (LVDS)* |
| AA2 | PL60B | 6 | LLM0_GDLLC_IN_A**/LDQ58 | C (LVDS)* | PL73B | 6 | LLM0_GDLLC_IN_A**/LDQ71 | C (LVDS)* |
| T5 | PL61A | 6 | LLM0_GDLLT_FB_A/LDQ58 | T | PL74A | 6 | LLM0_GDLLT_FB_A/LDQ71 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T7 | PL61B | 6 | LLM0_GDLLC_FB_D/LDQ58 | C | PL74B | 6 | LLM0_GDLLC_FB_D/LDQ71 | C |
| R8 | VCCPLL | 6 | | | VCCPLL | - | | |
| T8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| U3 | PL63A | 6 | LLM0_GPLLT_IN_A**/LDQ67 | T (LVDS)* | PL76A | 6 | LLM0_GPLLT_IN_A**/LDQ80 | T (LVDS)* |
| U4 | PL63B | 6 | LLM0_GPLLC_IN_A**/LDQ67 | C (LVDS)* | PL76B | 6 | LLM0_GPLLC_IN_A**/LDQ80 | C (LVDS)* |
| V3 | PL64A | 6 | LLM0_GPLLT_FB_A/LDQ67 | T | PL77A | 6 | LLM0_GPLLT_FB_A/LDQ80 | T |
| U5 | PL64B | 6 | LLM0_GPLLC_FB_A/LDQ67 | C | PL77B | 6 | LLM0_GPLLC_FB_A/LDQ80 | C |
| V4 | PL65A | 6 | LDQ67 | T (LVDS)* | PL78A | 6 | LDQ80 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V5 | PL65B | 6 | LDQ67 | C (LVDS)* | PL78B | 6 | LDQ80 | C (LVDS)* |
| Y3 | PL66A | 6 | LDQ67 | T | PL79A | 6 | LDQ80 | T |
| Y4 | PL66B | 6 | LDQ67 | C | PL79B | 6 | LDQ80 | C |
| W3 | PL67A | 6 | LDQS67 | T (LVDS)* | PL80A | 6 | LDQS80 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W4 | PL67B | 6 | LDQ67 | C (LVDS)* | PL80B | 6 | LDQ80 | C (LVDS)* |
| AA1 | PL68A | 6 | LDQ67 | T | PL81A | 6 | LDQ80 | T |
| AB1 | PL68B | 6 | LDQ67 | C | PL81B | 6 | LDQ80 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U8 | PL69A | 6 | LDQ67 | T (LVDS)* | PL82A | 6 | LDQ80 | T (LVDS)* |
| U7 | PL69B | 6 | LDQ67 | C (LVDS)* | PL82B | 6 | LDQ80 | C (LVDS)* |
| V8 | PL70A | 6 | LDQ67 | T | PL83A | 6 | LDQ80 | T |
| U6 | PL70B | 6 | LDQ67 | C | PL83B | 6 | LDQ80 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL71A | 6 | LDQ75 | T (LVDS)* | PL84A | 6 | LDQ88 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| W7 | PL72B | 6 | LDQ71 | C |
| W4 | PL73A | 6 | LLM0_GDLLT_IN_A**/LDQ71 | T (LVDS)* |
| W3 | PL73B | 6 | LLM0_GDLLC_IN_A**/LDQ71 | C (LVDS)* |
| W6 | PL74A | 6 | LLM0_GDLLT_FB_A/LDQ71 | T |
| GND | GNDIO6 | - | | |
| W8 | PL74B | 6 | LLM0_GDLLC_FB_D/LDQ71 | C |
| Y8 | LLM0_PLLCAP | 6 | | |
| Y1 | PL76A | 6 | LLM0_GPLLT_IN_A**/LDQ80 | T (LVDS)* |
| Y2 | PL76B | 6 | LLM0_GPLLC_IN_A**/LDQ80 | C (LVDS)* |
| Y5 | PL77A | 6 | LLM0_GPLLT_FB_A/LDQ80 | T |
| Y6 | PL77B | 6 | LLM0_GPLLC_FB_A/LDQ80 | C |
| Y4 | PL78A | 6 | LDQ80 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| Y3 | PL78B | 6 | LDQ80 | C (LVDS)* |
| AA6 | PL79A | 6 | LDQ80 | T |
| AA8 | PL79B | 6 | LDQ80 | C |
| AA2 | PL80A | 6 | LDQS80 | T (LVDS)* |
| GND | GNDIO6 | - | | |
| AA1 | PL80B | 6 | LDQ80 | C (LVDS)* |
| AA7 | PL81A | 6 | LDQ80 | T |
| AA5 | PL81B | 6 | LDQ80 | C |
| VCCIO | VCCIO6 | 6 | | |
| AA4 | PL82A | 6 | LDQ80 | T (LVDS)* |
| AA3 | PL82B | 6 | LDQ80 | C (LVDS)* |
| AB7 | PL83A | 6 | LDQ80 | T |
| AB5 | PL83B | 6 | LDQ80 | C |
| GND | GNDIO6 | - | | |
| AB2 | PL84A | 6 | LDQ88 | T (LVDS)* |
| AB1 | PL84B | 6 | LDQ88 | C (LVDS)* |
| AB8 | PL85A | 6 | LDQ88 | T |
| AB6 | PL85B | 6 | LDQ88 | C |
| VCCIO | VCCIO6 | 6 | | |
| AB4 | PL86A | 6 | LDQ88 | T (LVDS)* |
| AB3 | PL86B | 6 | LDQ88 | C (LVDS)* |
| AC7 | PL87A | 6 | LDQ88 | T |
| AC5 | PL87B | 6 | LDQ88 | C |
| GND | GNDIO6 | - | | |
| AC2 | PL88A | 6 | LDQS88 | T (LVDS)* |
| AC1 | PL88B | 6 | LDQ88 | C (LVDS)* |
| AC6 | PL89A | 6 | LDQ88 | T |
| VCCIO | VCCIO6 | 6 | | |
| AD6 | PL89B | 6 | LDQ88 | C |
| AD1 | PL90A | 6 | LDQ88 | T (LVDS)* |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| M19 | PR50A | 3 | RDQ52 | T (LVDS)* |
| M18 | PR49B | 3 | RDQ52 | C |
| VCCIO | VCCIO3 | 3 | | |
| L16 | PR49A | 3 | RDQ52 | T |
| L22 | PR48B | 3 | RDQ52 | C (LVDS)* |
| L21 | PR48A | 3 | RDQ52 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| K22 | PR46B | 3 | RLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | |
| K21 | PR46A | 3 | RLM3_SPLLT_FB_A | T |
| L17 | PR45B | 3 | RLM3_SPLLC_IN_A | C (LVDS)* |
| L18 | PR45A | 3 | RLM3_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| L20 | PR44B | 3 | | C |
| L19 | PR44A | 3 | | T |
| K16 | PR43B | 3 | | C (LVDS)* |
| K17 | PR43A | 3 | | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| J16 | PR42B | 3 | VREF2_3 | C |
| K18 | PR42A | 3 | VREF1_3 | T |
| J22 | PR41B | 3 | PCLKC3_0 | C (LVDS)* |
| J21 | PR41A | 3 | PCLKT3_0 | T (LVDS)* |
| H22 | PR39B | 2 | PCLKC2_0/RDQ36 | C |
| H21 | PR39A | 2 | PCLKT2_0/RDQ36 | T |
| GNDIO | GNDIO2 | - | | |
| J17 | PR38B | 2 | RDQ36 | C (LVDS)* |
| J18 | PR38A | 2 | RDQ36 | T (LVDS)* |
| J20 | PR37B | 2 | RDQ36 | C |
| J19 | PR37A | 2 | RDQ36 | T |
| VCCIO | VCCIO2 | 2 | | |
| H16 | PR36B | 2 | RDQ36 | C (LVDS)* |
| H17 | PR36A | 2 | RDQS36 | T (LVDS)* |
| G22 | PR35B | 2 | RDQ36 | C |
| GNDIO | GNDIO2 | - | | |
| G21 | PR35A | 2 | RDQ36 | T |
| H20 | PR34B | 2 | RDQ36 | C (LVDS)* |
| H19 | PR34A | 2 | RDQ36 | T (LVDS)* |
| G16 | PR33B | 2 | RUM3_SPLLC_FB_A/RDQ36 | C |
| VCCIO | VCCIO2 | 2 | | |
| H18 | PR33A | 2 | RUM3_SPLLT_FB_A/RDQ36 | T |
| F22 | PR32B | 2 | RUM3_SPLLC_IN_A/RDQ36 | C (LVDS)* |
| F21 | PR32A | 2 | RUM3_SPLLT_IN_A/RDQ36 | T (LVDS)* |
| G20 | PR30B | 2 | RDQ27 | C |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L5 | PL23A | 7 | LDQ27 | T (LVDS)* | PL33A | 7 | LDQ37 | T (LVDS)* |
| L4 | PL23B | 7 | LDQ27 | C (LVDS)* | PL33B | 7 | LDQ37 | C (LVDS)* |
| N9 | PL24A | 7 | LDQ27 | T | PL34A | 7 | LDQ37 | T |
| N7 | PL24B | 7 | LDQ27 | C | PL34B | 7 | LDQ37 | C |
| K2 | PL25A | 7 | LDQ27 | T (LVDS)* | PL35A | 7 | LDQ37 | T (LVDS)* |
| K1 | PL25B | 7 | LDQ27 | C (LVDS)* | PL35B | 7 | LDQ37 | C (LVDS)* |
| P9 | PL26A | 7 | LDQ27 | T | PL36A | 7 | LDQ37 | T |
| P7 | PL26B | 7 | LDQ27 | C | PL36B | 7 | LDQ37 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M6 | PL27A | 7 | LDQS27 | T (LVDS)* | PL37A | 7 | LDQS37 | T (LVDS)* |
| M5 | PL27B | 7 | LDQ27 | C (LVDS)* | PL37B | 7 | LDQ37 | C (LVDS)* |
| N5 | PL28A | 7 | LDQ27 | T | PL38A | 7 | LDQ37 | T |
| N6 | PL28B | 7 | LDQ27 | C | PL38B | 7 | LDQ37 | C |
| M4 | PL29A | 7 | LDQ27 | T (LVDS)* | PL39A | 7 | LDQ37 | T (LVDS)* |
| M3 | PL29B | 7 | LDQ27 | C (LVDS)* | PL39B | 7 | LDQ37 | C (LVDS)* |
| P6 | PL30A | 7 | LDQ27 | T | PL40A | 7 | LDQ37 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P8 | PL30B | 7 | LDQ27 | C | PL40B | 7 | LDQ37 | C |
| L3 | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T (LVDS)* | PL42A | 7 | LUM3_SPLLT_IN_A/LDQ46 | T (LVDS)* |
| L2 | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C (LVDS)* | PL42B | 7 | LUM3_SPLLC_IN_A/LDQ46 | C (LVDS)* |
| P5 | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T | PL43A | 7 | LUM3_SPLLT_FB_A/LDQ46 | T |
| P4 | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C | PL43B | 7 | LUM3_SPLLC_FB_A/LDQ46 | C |
| L1 | PL34A | 7 | LDQ36 | T (LVDS)* | PL44A | 7 | LDQ46 | T (LVDS)* |
| M2 | PL34B | 7 | LDQ36 | C (LVDS)* | PL44B | 7 | LDQ46 | C (LVDS)* |
| R5 | PL35A | 7 | LDQ36 | T | PL45A | 7 | LDQ46 | T |
| R4 | PL35B | 7 | LDQ36 | C | PL45B | 7 | LDQ46 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M1 | PL36A | 7 | LDQS36 | T (LVDS)* | PL46A | 7 | LDQS46 | T (LVDS)* |
| N2 | PL36B | 7 | LDQ36 | C (LVDS)* | PL46B | 7 | LDQ46 | C (LVDS)* |
| R8 | PL37A | 7 | LDQ36 | T | PL47A | 7 | LDQ46 | T |
| T9 | PL37B | 7 | LDQ36 | C | PL47B | 7 | LDQ46 | C |
| P3 | PL38A | 7 | LDQ36 | T (LVDS)* | PL48A | 7 | LDQ46 | T (LVDS)* |
| P2 | PL38B | 7 | LDQ36 | C (LVDS)* | PL48B | 7 | LDQ46 | C (LVDS)* |
| N1 | PL39A | 7 | PCLKT7_0/LDQ36 | T | PL49A | 7 | PCLKT7_0/LDQ46 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P1 | PL39B | 7 | PCLKC7_0/LDQ36 | C | PL49B | 7 | PCLKC7_0/LDQ46 | C |
| T5 | PL41A | 6 | PCLKT6_0 | T (LVDS)* | PL51A | 6 | PCLKT6_0/LDQ55 | T (LVDS)* |
| T4 | PL41B | 6 | PCLKC6_0 | C (LVDS)* | PL51B | 6 | PCLKC6_0/LDQ55 | C (LVDS)* |
| U7 | PL42A | 6 | VREF2_6 | T | PL52A | 6 | VREF2_6/LDQ55 | T |
| T8 | PL42B | 6 | VREF1_6 | C | PL52B | 6 | VREF1_6/LDQ55 | C |
| R3 | PL43A | 6 | | T (LVDS)* | PL53A | 6 | LDQ55 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | PL43B | 6 | | C (LVDS)* | PL53B | 6 | LDQ55 | C (LVDS)* |
| R1 | PL44A | 6 | | T | PL54A | 6 | LDQ55 | T |
| T1 | PL44B | 6 | | C | PL54B | 6 | LDQ55 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| - | - | - | | | VCCIO6 | 6 | | |
| T3 | PL45A | 6 | LLM3_SPLLT_IN_A | T (LVDS)* | PL57A | 6 | LLM3_SPLLT_IN_A/LDQ55 | T (LVDS)* |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| - | - | - | | | VCCIO2 | 2 | | |
| H23 | NC | - | | | PR15B | 2 | RDQ15 | C (LVDS)* |
| H24 | NC | - | | | PR15A | 2 | RDQS15 | T (LVDS)* |
| D28 | NC | - | | | PR14B | 2 | RDQ15 | C |
| - | - | - | | | GNDIO2 | - | | |
| E28 | NC | - | | | PR14A | 2 | RDQ15 | T |
| G24 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C (LVDS)* |
| H25 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| D27 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| GNDIO | GNDIO2 | - | | | VCCIO2 | 2 | | |
| E27 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| F26 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C (LVDS)* |
| G25 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| F24 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| VCCIO | VCCIO2 | - | | | - | - | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F25 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G23 | XRES | - | | | XRES | 1 | | |
| C30 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A29 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B30 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B29 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C27 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A26 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A27 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B26 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C26 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B25 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C25 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A25 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C29 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B28 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C28 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A28 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B24 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| E24 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D24 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C24 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A20 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C20 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B20 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C19 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A23 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C23 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B23 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C22 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B22 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G7 | PL8A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| G8 | PL6A | 7 | LDQS6**** | T (LVDS)* | NC | - | | |
| G9 | PL5A | 7 | LDQ6 | T | NC | - | | |
| H19 | NC | - | | | NC | - | | |
| H20 | NC | - | | | NC | - | | |
| H21 | NC | - | | | NC | - | | |
| H22 | NC | - | | | NC | - | | |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| H8 | PL5B | 7 | LDQ6 | C | NC | - | | |
| H9 | PL2A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| J10 | PL2B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| J20 | NC | - | | | NC | - | | |
| J21 | NC | - | | | NC | - | | |
| J9 | PL4A | 7 | LDQ6 | T (LVDS)* | NC | - | | |
| K9 | PL4B | 7 | LDQ6 | C (LVDS)* | NC | - | | |
| R9 | NC | - | | | NC | - | | |
| U22 | NC | - | | | NC | - | | |
| W9 | NC | - | | | NC | - | | |
| N13 | VCCPLL | - | | | VCCPLL | - | | |
| N18 | VCCPLL | - | | | VCCPLL | - | | |
| V13 | VCCPLL | - | | | VCCPLL | - | | |
| V18 | VCCPLL | - | | | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AK12 | NC | - | | | NC | - | | |
| AK24 | NC | - | | | NC | - | | |
| AK25 | NC | - | | | NC | - | | |
| AK26 | NC | - | | | NC | - | | |
| AK4 | NC | - | | | NC | - | | |
| AK9 | NC | - | | | NC | - | | |
| AL11 | NC | - | | | NC | - | | |
| AL12 | NC | - | | | NC | - | | |
| AL34 | NC | - | | | NC | - | | |
| AM10 | NC | - | | | NC | - | | |
| AM11 | NC | - | | | NC | - | | |
| AM13 | NC | - | | | NC | - | | |
| AM25 | NC | - | | | NC | - | | |
| AN10 | NC | - | | | NC | - | | |
| AN11 | NC | - | | | NC | - | | |
| AN12 | NC | - | | | NC | - | | |
| AN13 | NC | - | | | NC | - | | |
| AN24 | NC | - | | | NC | - | | |
| AN25 | NC | - | | | NC | - | | |
| AP11 | NC | - | | | NC | - | | |
| AP12 | NC | - | | | NC | - | | |
| AP24 | NC | - | | | NC | - | | |
| B10 | NC | - | | | NC | - | | |
| B11 | NC | - | | | NC | - | | |
| B12 | NC | - | | | NC | - | | |
| B13 | NC | - | | | NC | - | | |
| B22 | NC | - | | | NC | - | | |
| B23 | NC | - | | | NC | - | | |
| B24 | NC | - | | | NC | - | | |
| B25 | NC | - | | | NC | - | | |
| C10 | NC | - | | | NC | - | | |
| C11 | NC | - | | | NC | - | | |
| C13 | NC | - | | | NC | - | | |
| C22 | NC | - | | | NC | - | | |
| C24 | NC | - | | | NC | - | | |
| C25 | NC | - | | | NC | - | | |
| D1 | NC | - | | | NC | - | | |
| D15 | NC | - | | | NC | - | | |
| D24 | NC | - | | | NC | - | | |
| D34 | NC | - | | | NC | - | | |
| E10 | NC | - | | | NC | - | | |
| E24 | NC | - | | | NC | - | | |
| E25 | NC | - | | | NC | - | | |
| E26 | NC | - | | | NC | - | | |
| E3 | NC | - | | | NC | - | | |
| E31 | NC | - | | | NC | - | | |
| E32 | NC | - | | | NC | - | | |
| E33 | NC | - | | | NC | - | | |
| E34 | NC | - | | | NC | - | | |

# LatticeECP2/M Family Data Sheet Ordering Information

July 2012 Data Sheet DS1006

## LatticeECP2 Part Number Description

LFE2 – XX XE – X XXXXXX X

**Device Family**
ECP2 (LatticeECP2 FPGA)

**Logic Capacity**
6 = 6K LUTs
12 = 12K LUTs
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs

**Encryption**
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

**Supply Voltage**
E = 1.2V

**Grade**
C = Commercial
I = Industrial

**Package**
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FN256 = 256-ball Lead-Free fpBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN900 = 900-ball Lead-Free fpBGA

**Speed**
5 = Slowest
6
7 = Fastest

## Ordering Information

Note:þLatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:


## LatticeECP2 Standard Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5TN144C | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-6TN144C | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-7TN144C | 90 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-5FN256C | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-6FN256C | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-7FN256C | 190 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5TN144C | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-6TN144C | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-7TN144C | 93 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-5FN484C | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-6FN484C | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-7FN484C | 297 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-5FN672C | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-6FN672C | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-7FN672C | 402 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 20 |

## LatticeECP2M Part Number Description

LFE2M XXX XE – X XXXXXX X

**Device Family**
ECP2M (LatticeECP2 FPGA + SERDES)

**Logic Capacity**
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs
100 = 100K LUTs

**Encryption**
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

**Supply Voltage**
E = 1.2V

**Grade**
C = Commercial
I = Industrial

**Package**
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
F1152 = 1152-ball fpBGA

FN256 = 256-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA
FN672 = 672-ball Lead-free fpBGA
FN900 = 900-ball Lead-free fpBGA
FN1152 = 1152-ball Lead-free fpBGA

**Speed**
5 = Slowest
6
7 = Fastest

## Ordering Information

Note:þLatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:


| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5FN1152C | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-6FN1152C | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-7FN1152C | 520 | 1.2V | -7 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 100 |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2007 (cont.) | 02.8 (cont.) | DC and Switching (cont.) | sysCLOCK GPLL timing has been updated. |
| | | Pinout Information | Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information. |
| | | Ordering Information | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| September 2007 | 02.9 | Pinout Information | Added Thermal Management text section. |
| February 2008 | 03.0 | Architecture | Added LVCMOS33D description. |
| | | DC and Switching | LatticeECP2M Supply Current has been updated. |
| | | | Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11). |
| | | | Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated. |
| | | | Table 3-8. Channel output Jitter (Max) has been updated. |
| | | Pinout Information | Signal description has been updated. |
| | | | Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100. |
| April 2008 | 03.1 | Pinout Information | Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated. |
| June 2008 | 03.2 | Introduction | Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device. |
| | | Architecture | Removed Read-Before-Write sysMEM EBR mode. |
| | | | Clarification of the operation of the secondary clock regions. |
| | | DC and Switching Characteristics | Removed Read-Before-Write sysMEM EBR mode. |
| August 2008 | 03.3 | Architecture | Clarification of the operation of the secondary clock regions. |
| | | Pinout Information | Added information for [LOC]DQ[num] to Signal Descriptions table. |
| January 2009 | 03.4 | DC and Switching Characteristics | Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode. |
| | | | Added Channel Output Jitter table for x20 mode. |
| November 2009 | 03.5 | DC and Switching Characteristics | Updated SPI/SPIm Configuration Waveforms diagram. |
| | | | Updated footnotes in LatticeECP2 Initialization Supply Current table. |
| | | | Updated footnotes in LatticeECP2M Initialization Supply Current table. |
| | | | Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table. |
| | | | Updated max. value for $t_{DINIT}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Updated Figure 3-5 MLVDS |
| | | | Updated Table 3-7 Serial Output Timing and Levels |
| | | | Updated Table 3-15 Power Down/Power Up Specification |
| | | Pinout Information | Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5. |