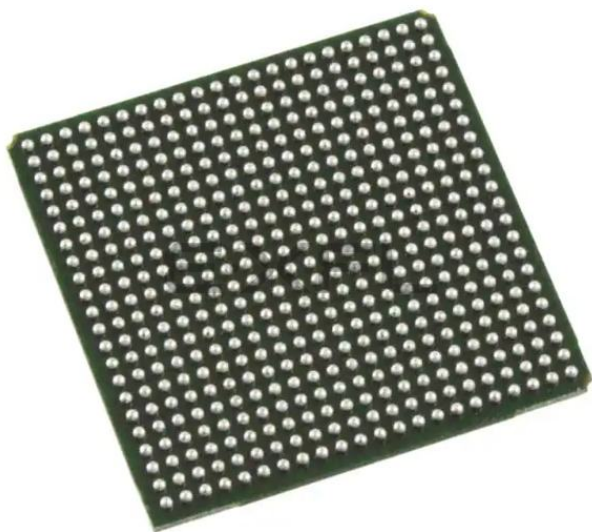




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	331
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20e-7f484c

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI or SPI _m mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. sysCONFIG Port Data I/O for SPI or SPI _m . When using the SPI or SPI _m mode, this pin should either be tied high or low, must not be left floating.
D[1:6]	I/O	sysCONFIG Port Data I/O for Parallel
D[7]/SPID0	I/O	sysCONFIG Port Data I/O for Parallel, SPI, SPI _m
DOUT/CSN	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPI0N	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPI _m modes.
Dedicated SERDES Signals^{1, 2, 3}		
[LOC]_SQ_VCCAUX33	—	Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused.
[LOC]_SQ_REFCLKN	I	Negative Reference Clock Input
[LOC]_SQ_REFCLKP	I	Positive Reference Clock Input
[LOC]_SQ_VCCP	—	PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused.

LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

Available Device Resources by Package, LatticeECP2

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA
PLL/DLL	ECP2-6	4	—	—	—
	ECP2-12	4	4	—	—
	ECP2-20	4	4	4	—
	ECP2-35	—	4	4	—
	ECP2-50	—	6	6	—
	ECP2-70	—	—	8	8

Available Device Resources by Package, LatticeECP2M

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA	1152 fpBGA
PLL/DLL	ECP2M20	10	10	—	—	—
	ECP2M35	10	10	10	—	—
	ECP2M50	—	10	10	10	—
	ECP2M70	—	—	—	10	10
	ECP2M100	—	—	—	10	10

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
46	NC	5			PB16B	5	BDQ15	C
47	GND	-			GND	-		
48	VCC				VCC	-		
49	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
50	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
51	GND	-			GND	-		
52	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
53	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
54	VCC	-			VCC	-		
55	PB14A	4	BDQ15	T	PB34A	4	BDQ33	T
56	PB14B	4	BDQ15	C	PB34B	4	BDQ33	C
57	PB16A	4	BDQ15	T	PB40A	4	BDQ42	T
58	PB16B	4	BDQ15	C	PB40B	4	BDQ42	C
59	PB18A	4	BDQ15	T	PB44A	4	BDQ42	T
60	PB18B	4	BDQ15	C	PB44B	4	BDQ42	C
61	GND	-			GND	-		
62	PB20A	4	BDQ24	T	PB48A	4	BDQ51	T
63	PB20B	4	BDQ24	C	PB48B	4	BDQ51	C
64	VCCIO4	4			VCCIO4	4		
65	PB22A	4	BDQ24	T	PB50A	4	BDQ51	T
66	PB22B	4	BDQ24	C	PB50B	4	BDQ51	C
67	PB24A	4	BDQS24	T	PB52A	4	BDQ51	T
68	PB24B	4	BDQ24	C	PB52B	4	BDQ51	C
69	PB26A	4	BDQ24	T	PB54A	4	BDQ51	T
70	PB26B	4	BDQ24	C	PB54B	4	BDQ51	C
71	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
72	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
73	CFG1	8			CFG1	8		
74	CFG2	8			CFG2	8		
75	PROGRAMN	8			PROGRAMN	8		
76	INITN	8			INITN	8		
77	CFG0	8			CFG0	8		
78	CCLK	8			CCLK	8		
79	DONE	8			DONE	8		
80	PR29A	8	D0/SPIFASTN		PR29A	8	D0/SPIFASTN	
81	GND	-			GND	-		
82	PR26A	8	D6		PR26A	8	D6	
83	VCC	-			VCC	-		
84	PR25B	8	D7/SPID0	C	PR25B	8	D7/SPID0	C
85	VCCIO8	8			VCCIO8	8		
86	PR25A	8	DI/CSSPI0N	T	PR25A	8	DI/CSSPI0N	T
87	PR24B	8	DOUT/CSON	C	PR24B	8	DOUT/CSON	C
88	PR24A	8	BUSY/SISPI	T	PR24A	8	BUSY/SISPI	T
89	VCCIO3	3			VCCIO3	3		
90	VCCAUX	-			VCCAUX	-		

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
136	PT6B	0		C	PT16B	0		C
137	PT6A	0		T	PT16A	0		T
138	GND	-			GND	-		
139	VCCIO0	0			VCCIO0	0		
140	PT4B	0		C	PT6B	0		C
141	PT4A	0		T	PT6A	0		T
142	VCCAUX	-			VCCAUX	-		
143	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
144	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one-to-one connection with a package ball or pin.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T
GNDIO	GNDIO4	-			GNDIO4	-		
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO	4		
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W20	CFG0	8			CFG0	8		
V20	PROGRAMN	8			PROGRAMN	8		
W22	CCLK	8			CCLK	8		
V22	INITN	8			INITN	8		
V21	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
R16	PR58B	8	WRITEN	C	PR77B	8	WRITEN	C
R17	PR58A	8	CS1N	T	PR77A	8	CS1N	T
U19	PR57B	8	CSN	C	PR76B	8	CSN	C
U20	PR57A	8	D0/SPIFASTN	T	PR76A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO	8		
U22	PR56B	8	D1	C	PR75B	8	D1	C
U21	PR56A	8	D2	T	PR75A	8	D2	T
T20	PR55B	8	D3	C	PR74B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
T19	PR55A	8	D4	T	PR74A	8	D4	T
T17	PR54B	8	D5	C	PR73B	8	D5	C
T18	PR54A	8	D6	T	PR73A	8	D6	T
T21	PR53B	8	D7/SPID0	C	PR72B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO	8		
T22	PR53A	8	DI/CSSPION	T	PR72A	8	DI/CSSPION	T
R18	PR52B	8	DOUT/CSON	C	PR71B	8	DOUT/CSON	C
R19	PR52A	8	BUSY/SISPI	T	PR71A	8	BUSY/SISPI	T
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO	3		
R22	PR47B	3	RDQ48	C	PR66B	3	RDQ67	C
R21	PR47A	3	RDQ48	T	PR66A	3	RDQ67	T
P18	PR46B	3	RDQ48	C (LVDS)*	PR65B	3	RDQ67	C (LVDS)*
P19	PR46A	3	RDQ48	T (LVDS)*	PR65A	3	RDQ67	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
R20	PR45B	3	RLM0_GPLL_C_FB_A/RDQ48	C	PR64B	3	RLM0_GPLL_C_FB_A/RDQ67	C
P22	PR45A	3	RLM0_GPLL_T_FB_A/RDQ48	T	PR64A	3	RLM0_GPLL_T_FB_A/RDQ67	T
P21	PR44B	3	RLM0_GPLL_C_IN_A**/RDQ48	C (LVDS)*	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*
N21	PR44A	3	RLM0_GPLL_T_IN_A**/RDQ48	T (LVDS)*	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR42B	3	RLM0_GDLL_C_FB_A/RDQ39	C	PR61B	3	RLM0_GDLL_C_FB_A/RDQ58	C
N20	PR42A	3	RLM0_GDLL_T_FB_A/RDQ39	T	PR61A	3	RLM0_GDLL_T_FB_A/RDQ58	T
GNDIO	GNDIO3	-			GNDIO3	-		
M22	PR41B	3	RLM0_GDLL_C_IN_A**/RDQ39	C (LVDS)*	PR60B	3	RLM0_GDLL_C_IN_A**/RDQ58	C (LVDS)*
M21	PR41A	3	RLM0_GDLL_T_IN_A**/RDQ39	T (LVDS)*	PR60A	3	RLM0_GDLL_T_IN_A**/RDQ58	T (LVDS)*
N19	PR40B	3	RDQ39	C	PR59B	3	RDQ58	C
M19	PR40A	3	RDQ39	T	PR59A	3	RDQ58	T
VCCIO	VCCIO3	3			VCCIO	3		
GNDIO	GNDIO3	-			GNDIO3	-		
L22	PR30B	3	RDQ31	C	PR49B	3	RDQ50	C
K22	PR30A	3	RDQ31	T	PR49A	3	RDQ50	T

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D15	PT52A	1		T	PT61A	1		T
E15	PT51B	1		C	PT60B	1		C
F15	PT51A	1		T	PT60A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
B15	PT49B	1		C	PT58B	1		C
VCCIO	VCCIO1	1			VCCIO	1		
A15	PT49A	1		T	PT58A	1		T
B14	PT48B	1		C	PT57B	1		C
A14	PT48A	1		T	PT57A	1		T
D14	PT46B	1		C	PT55B	1		C
C13	PT46A	1		T	PT55A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
E14	PT45B	1		C	PT54B	1		C
F14	PT45A	1		T	PT54A	1		T
A13	PT44B	1		C	PT53B	1		C
B13	PT44A	1		T	PT53A	1		T
VCCIO	VCCIO1	1			VCCIO	1		
E13	PT43B	1		C	PT52B	1		C
D13	PT43A	1		T	PT52A	1		T
E12	PT42B	1		C	PT51B	1		C
D12	PT42A	1		T	PT51A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A12	PT40B	1		C	PT49B	1		C
A11	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO	1		
B12	PT39B	1	PCLKC1_0	C	PT48B	1	PCLKC1_0	C
C12	PT39A	1	PCLKT1_0	T	PT48A	1	PCLKT1_0	T
F12	XRES	1			XRES	1		
B10	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	0		
B11	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T
A10	PT36B	0		C	PT45B	0		C
A9	PT36A	0		T	PT45A	0		T
C11	PT35B	0		C	PT44B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
C10	PT35A	0		T	PT44A	0		T
E11	PT34B	0		C	PT43B	0		C
F11	PT34A	0		T	PT43A	0		T
A8	PT33B	0		C	PT42B	0		C
A7	PT33A	0		T	PT42A	0		T
B8	PT32B	0		C	PT41B	0		C
GNDIO	GNDIO0	-			GNDIO0	0		
B9	PT32A	0		T	PT41A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B7	PT30B	0		C	PT39B	0		C
A6	PT30A	0		T	PT39A	0		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L2	NC	-			NC	-		
L1	NC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
M2	NC	-			NC	-		
M1	NC	-			NC	-		
N2	NC	-			NC	-		
GND	GNDIO7	-			GNDIO7	-		
M8	VCC	-			NC	-		
VCCIO	VCCIO7	7			VCCIO7	7		
GND	GNDIO7	-			GNDIO7	-		
N1	PL12A	7	LDQ16		PL18A	7	LDQ22	
L8	PL13A	7	LDQ16	T	PL19A	7	LDQ22	T
K8	PL13B	7	LDQ16	C	PL19B	7	LDQ22	C
VCCIO	VCCIO7	7			VCCIO7	7		
L6	PL14A	7	LDQ16	T (LVDS)*	PL20A	7	LDQ22	T (LVDS)*
K5	PL14B	7	LDQ16	C (LVDS)*	PL20B	7	LDQ22	C (LVDS)*
L7	PL15A	7	LDQ16	T	PL21A	7	LDQ22	T
L5	PL15B	7	LDQ16	C	PL21B	7	LDQ22	C
GND	GNDIO7	-			GNDIO7	-		
P1	PL16A	7	LDQS16	T (LVDS)*	PL22A	7	LDQS22	T (LVDS)*
P2	PL16B	7	LDQ16	C (LVDS)*	PL22B	7	LDQ22	C (LVDS)*
M6	PL17A	7	LDQ16	T	PL23A	7	LDQ22	T
VCCIO	VCCIO7	7			VCCIO7	7		
N8	PL17B	7	LDQ16	C	PL23B	7	LDQ22	C
R1	PL18A	7	LDQ16	T (LVDS)*	PL24A	7	LDQ22	T (LVDS)*
R2	PL18B	7	LDQ16	C (LVDS)*	PL24B	7	LDQ22	C (LVDS)*
M7	PL19A	7	PCLKT7_0/LDQ16	T	PL25A	7	PCLKT7_0/LDQ22	T
GND	GNDIO7	-			GNDIO7	-		
N9	PL19B	7	PCLKC7_0/LDQ16	C	PL25B	7	PCLKC7_0/LDQ22	C
M4	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	PL27A	6	PCLKT6_0/LDQ31	T (LVDS)*
M5	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*	PL27B	6	PCLKC6_0/LDQ31	C (LVDS)*
N7	PL22A	6	VREF2_6/LDQ25	T	PL28A	6	VREF2_6/LDQ31	T
P9	PL22B	6	VREF1_6/LDQ25	C	PL28B	6	VREF1_6/LDQ31	C
N3	PL23A	6	LDQ25	T (LVDS)*	PL29A	6	LDQ31	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
N4	PL23B	6	LDQ25	C (LVDS)*	PL29B	6	LDQ31	C (LVDS)*
N5	PL24A	6	LDQ25	T	PL30A	6	LDQ31	T
P7	PL24B	6	LDQ25	C	PL30B	6	LDQ31	C
T1	NC	-			PL31A	6	LDQS31	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
T2	NC	-			PL31B	6	LDQ31	C (LVDS)*
P8	NC	-			PL32A	6	LDQ31	T
P6	NC	-			PL32B	6	LDQ31	C
VCCIO	VCCIO6	6			VCCIO6	6		
P5	NC	-			PL33A	6	LDQ31	T (LVDS)*
P4	NC	-			PL33B	6	LDQ31	C (LVDS)*

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR18B	2	RDQ16	C (LVDS)*	PR24B	2	RDQ22	C (LVDS)*
K22	PR18A	2	RDQ16	T (LVDS)*	PR24A	2	RDQ22	T (LVDS)*
M24	PR17B	2	RDQ16	C	PR23B	2	RDQ22	C
N23	PR17A	2	RDQ16	T	PR23A	2	RDQ22	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR16B	2	RDQ16	C (LVDS)*	PR22B	2	RDQ22	C (LVDS)*
K25	PR16A	2	RDQS16	T (LVDS)*	PR22A	2	RDQS22	T (LVDS)*
M20	PR15B	2	RDQ16	C	PR21B	2	RDQ22	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR15A	2	RDQ16	T	PR21A	2	RDQ22	T
L22	PR14B	2	RDQ16	C (LVDS)*	PR20B	2	RDQ22	C (LVDS)*
M22	PR14A	2	RDQ16	T (LVDS)*	PR20A	2	RDQ22	T (LVDS)*
K21	PR13B	2	RDQ16	C	PR19B	2	RDQ22	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR13A	2	RDQ16	T	PR19A	2	RDQ22	T
K24	PR12B	2	RDQ16	C (LVDS)*	PR18B	2	RDQ22	C (LVDS)*
J24	PR12A	2	RDQ16	T (LVDS)*	PR18A	2	RDQ22	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	NC	-			NC	-		
J25	NC	-			NC	-		
J23	NC	-			NC	-		
K23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
H26	NC	-			NC	-		
H25	NC	-			NC	-		
H24	NC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
H23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR11B	2	RDQ8	C	PR17B	2	RDQ14	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR11A	2	RDQ8	T	PR17A	2	RDQ14	T
F26	PR10B	2	RDQ8	C (LVDS)*	PR16B	2	RDQ14	C (LVDS)*
F25	PR10A	2	RDQ8	T (LVDS)*	PR16A	2	RDQ14	T (LVDS)*
K20	PR9B	2	RDQ8	C	PR15B	2	RDQ14	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR9A	2	RDQ8	T	PR15A	2	RDQ14	T
E26	PR8B	2	RDQ8	C (LVDS)*	PR14B	2	RDQ14	C (LVDS)*
E25	PR8A	2	RDQS8	T (LVDS)*	PR14A	2	RDQS14	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR7B	2	RDQ8	C	PR13B	2	RDQ14	C
H22	PR7A	2	RDQ8	T	PR13A	2	RDQ14	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR43B	2	RDQ41	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
K22	PR43A	2	RDQ41	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
M24	PR42B	2	RDQ41	C	PR55B	2	RDQ54	C
N23	PR42A	2	RDQ41	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR41B	2	RDQ41	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
K25	PR41A	2	RDQS41	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
M20	PR40B	2	RDQ41	C	PR53B	2	RDQ54	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR40A	2	RDQ41	T	PR53A	2	RDQ54	T
L22	PR39B	2	RDQ41	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
M22	PR39A	2	RDQ41	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
K21	PR38B	2	RDQ41	C	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR38A	2	RDQ41	T	PR51A	2	RDQ54	T
K24	PR37B	2	RDQ41	C (LVDS)*	PR50B	2	RDQ54	C (LVDS)*
J24	PR37A	2	RDQ41	T (LVDS)*	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCCPLL	2			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
J25	PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
J23	PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
K23	PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
H26	PR24B	2	RDQ24	C (LVDS)*	PR37B	2	RDQ37	C (LVDS)*
H25	PR24A	2	RDQS24***	T (LVDS)*	PR37A	2	RDQS37***	T (LVDS)*
H24	PR23B	2	RDQ24	C	PR36B	2	RDQ37	C
GND	GNDIO2	-			GNDIO2	-		
H23	PR23A	2	RDQ24	T	PR36A	2	RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR19B	2	RDQ16	C	PR32B	2	RDQ29	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR19A	2	RDQ16	T	PR32A	2	RDQ29	T
F26	PR18B	2	RDQ16	C (LVDS)*	PR31B	2	RDQ29	C (LVDS)*
F25	PR18A	2	RDQ16	T (LVDS)*	PR31A	2	RDQ29	T (LVDS)*
K20	PR17B	2	RDQ16	C	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR17A	2	RDQ16	T	PR30A	2	RDQ29	T
E26	PR16B	2	RDQ16	C (LVDS)*	PR29B	2	RDQ29	C (LVDS)*
E25	PR16A	2	RDQS16	T (LVDS)*	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR15B	2	RDQ16	C	PR28B	2	RDQ29	C
H22	PR15A	2	RDQ16	T	PR28A	2	RDQ29	T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
-	-	-			VCCIO5	5			
-	-	-			GNDIO5	-			
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T	
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C	
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T	
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C	
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C	
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T	
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C	
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C	
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T	
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C	
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C	
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T	
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C	
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T	
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C	
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T	
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C	
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T	
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C	
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T	
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C	
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T	
GNDIO	GNDIO4	-			GNDIO4	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AH25	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13			
AJ25	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C	
AH26	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13			
AJ26	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C	
AK27	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13			
AK26	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T	
AH27	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13			
AJ29	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C	
AJ30	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13			
AK29	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T	
AH30	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13			
AG27	CFG2	8			CFG2	8			
AD25	CFG1	8			CFG1	8			
AG28	CFG0	8			CFG0	8			
AG30	PROGRAMN	8			PROGRAMN	8			
AG29	CCLK	8			CCLK	8			
AC24	INITN	8			INITN	8			
AF27	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
AF28	WRITEN***	8			WRITEN***	8			
AE26	CS1N***	8			CS1N***	8			
AB23	CSN***	8			CSN***	8			
AF29	D0/SPIFASTN***	8			D0/SPIFASTN***	8			
VCCIO	VCCIO8	8			VCCIO8	8			
AF30	D1***	8			D1***	8			
AD26	D2***	8			D2***	8			
AE29	D3***	8			D3***	8			
GNDIO	GNDIO8	-			GNDIO8	-			
AE30	D4***	8			D4***	8			
AD29	D5***	8			D5***	8			
AC25	D6***	8			D6***	8			
AD30	D7/SPID0***	8			D7/SPID0***	8			
VCCIO	VCCIO8	8			VCCIO8	8			
AA22	DI/CSSPI0N***	8			DI/CSSPI0N***	8			
AC26	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8			
AA23	BUSY/SISPI***	8			BUSY/SISPI***	8			
AB22	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
AC27	PR65B	3	RLM0_GDLLC_FB_A	C	PR85B	3	RLM0_GDLLC_FB_A/RDQ82	C	
GNDIO	GNDIO3	-			GNDIO3	-			
AC28	PR65A	3	RLM0_GDLLT_FB_A	T	PR85A	3	RLM0_GDLLT_FB_A/RDQ82	T	
AC29	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR84B	3	RLM0_GDLLC_IN_A**/RDQ82	C (LVDS)*	
AC30	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR84A	3	RLM0_GDLLT_IN_A**/RDQ82	T (LVDS)*	
AB30	PR63B	3	RLM0_GPLL_C_IN_A**	C	PR83B	3	RLM0_GPLL_C_IN_A**/RDQ82	C	
VCCIO	VCCIO3	3			VCCIO3	3			
AA30	PR63A	3	RLM0_GPLLT_IN_A**	T	PR83A	3	RLM0_GPLLT_IN_A**/RDQ82	T	
AB29	PR62B	3	RLM0_GPLL_C_FB_A	C (LVDS)*	PR82B	3	RLM0_GPLL_C_FB_A/RDQ82	C (LVDS)*	
AB28	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR82A	3	RLM0_GPLLT_FB_A/RDQ82	T (LVDS)*	
GNDIO	GNDIO3	-			GNDIO3	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			VCCIO2	2			
H23	NC	-			PR15B	2	RDQ15	C (LVDS)*	
H24	NC	-			PR15A	2	RDQS15	T (LVDS)*	
D28	NC	-			PR14B	2	RDQ15	C	
-	-	-			GNDIO2	-			
E28	NC	-			PR14A	2	RDQ15	T	
G24	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
H25	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
D27	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
GNDIO	GNDIO2	-			VCCIO2	2			
E27	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	
G25	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
F24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
VCCIO	VCCIO2	-			-	-			
GNDIO	GNDIO2	-			GNDIO2	-			
F25	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G23	XRES	-			XRES	1			
C30	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A29	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B30	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B29	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C27	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A26	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A27	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B26	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C26	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B25	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C25	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A25	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C29	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B28	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C28	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A28	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B24	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E24	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D24	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C24	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A20	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	
C20	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B20	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C19	URC_SQ_VCCR_X2	12			URC_SQ_VCCR_X2	12			
A23	URC_SQ_HDOUT_P2	12		T	URC_SQ_HDOUT_P2	12		T	
C23	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B23	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C22	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B22	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K13	VCCIO0	0			VCCIO0	0			
D17	VCCIO1	1			VCCIO1	1			
E22	VCCIO1	1			VCCIO1	1			
E25	VCCIO1	1			VCCIO1	1			
F19	VCCIO1	1			VCCIO1	1			
K18	VCCIO1	1			VCCIO1	1			
K19	VCCIO1	1			VCCIO1	1			
F28	VCCIO2	2			VCCIO2	2			
J25	VCCIO2	2			VCCIO2	2			
K28	VCCIO2	2			VCCIO2	2			
M21	VCCIO2	2			VCCIO2	2			
M24	VCCIO2	2			VCCIO2	2			
N21	VCCIO2	2			VCCIO2	2			
N28	VCCIO2	2			VCCIO2	2			
P21	VCCIO2	2			VCCIO2	2			
R25	VCCIO2	2			VCCIO2	2			
AA28	VCCIO3	3			VCCIO3	3			
AB25	VCCIO3	3			VCCIO3	3			
AE28	VCCIO3	3			VCCIO3	3			
T25	VCCIO3	3			VCCIO3	3			
U21	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
V28	VCCIO3	3			VCCIO3	3			
W21	VCCIO3	3			VCCIO3	3			
W24	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
AA19	VCCIO4	4			VCCIO4	4			
AE19	VCCIO4	4			VCCIO4	4			
AF22	VCCIO4	4			VCCIO4	4			
AG17	VCCIO4	4			VCCIO4	4			
AG25	VCCIO4	4			VCCIO4	4			
AA12	VCCIO5	5			VCCIO5	5			
AA13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AF9	VCCIO5	5			VCCIO5	5			
AG14	VCCIO5	5			VCCIO5	5			
AG6	VCCIO5	5			VCCIO5	5			
AA3	VCCIO6	6			VCCIO6	6			
AB6	VCCIO6	6			VCCIO6	6			
AE3	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
U10	VCCIO6	6			VCCIO6	6			
V10	VCCIO6	6			VCCIO6	6			
V3	VCCIO6	6			VCCIO6	6			
W10	VCCIO6	6			VCCIO6	6			
W7	VCCIO6	6			VCCIO6	6			
F3	VCCIO7	7			VCCIO7	7			
J6	VCCIO7	7			VCCIO7	7			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AJ2	LLC_SQ_HDINN3	14		C
AH4	LLC_SQ_VCCTX3	14		
AK5	LLC_SQ_HDOUTP3	14		T
AK4	LLC_SQ_VCCOB3	14		
AJ5	LLC_SQ_HDOUTN3	14		C
AH5	LLC_SQ_VCCTX2	14		
AJ6	LLC_SQ_HDOUTN2	14		C
AH6	LLC_SQ_VCCOB2	14		
AK6	LLC_SQ_HDOUTP2	14		T
AH2	LLC_SQ_VCCR2	14		
AJ3	LLC_SQ_HDINN2	14		C
AH3	LLC_SQ_VCCIB2	14		
AK3	LLC_SQ_HDINP2	14		T
AH7	LLC_SQ_VCCP	14		
AG7	LLC_SQ_REFCLKP	14		T
AF7	LLC_SQ_REFCLKN	14		C
AJ7	LLC_SQ_VCCAUX33	14		
AK11	LLC_SQ_HDINP1	14		T
AH11	LLC_SQ_VCCIB1	14		
AJ11	LLC_SQ_HDINN1	14		C
AH12	LLC_SQ_VCCR1	14		
AK8	LLC_SQ_HDOUTP1	14		T
AH8	LLC_SQ_VCCOB1	14		
AJ8	LLC_SQ_HDOUTN1	14		C
AH9	LLC_SQ_VCCTX1	14		
AJ9	LLC_SQ_HDOUTN0	14		C
AK10	LLC_SQ_VCCOB0	14		
AK9	LLC_SQ_HDOUTP0	14		T
AH10	LLC_SQ_VCCTX0	14		
AJ12	LLC_SQ_HDINN0	14		C
AJ13	LLC_SQ_VCCIB0	14		
AK12	LLC_SQ_HDINP0	14		T
AH13	LLC_SQ_VCCR0	14		
AF10	PB30A	5	BDQ33	T
AE8	PB30B	5	BDQ33	C
AE11	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5		
AD9	PB31B	5	BDQ33	C
AE10	PB32A	5	BDQ33	T
AD10	PB32B	5	BDQ33	C
AE13	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-		
AC12	PB33B	5	BDQ33	C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K26	PR26A	2	RDQ23	T
K23	PR25B	2	RDQ23	C (LVDS)*
K22	PR25A	2	RDQ23	T (LVDS)*
J22	PR24B	2	RDQ23	C
VCCIO	VCCIO2	2		
J23	PR24A	2	RDQ23	T
GNDIO	GNDIO2	-		
VCCIO	VCCIO2	2		
J26	PR17B	2	RDQ15	C (LVDS)*
H26	PR17A	2	RDQ15	T (LVDS)*
H27	PR16B	2	RDQ15	C
G26	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2		
H23	PR15B	2	RDQ15	C (LVDS)*
H24	PR15A	2	RDQS15	T (LVDS)*
D28	PR14B	2	RDQ15	C
GNDIO	GNDIO2	-		
E28	PR14A	2	RDQ15	T
G24	PR13B	2	RDQ15	C (LVDS)*
H25	PR13A	2	RDQ15	T (LVDS)*
D27	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
VCCIO	VCCIO2	2		
E27	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
F26	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*
G25	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
F24	PR9B	2	VREF2_2	C
-	-	-		
GNDIO	GNDIO2	-		
F25	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
G23	XRES	1		
C30	URC_SQ_VCCR0	12		
A29	URC_SQ_HDINP0	12		T
B30	URC_SQ_VCCIB0	12		
B29	URC_SQ_HDINN0	12		C
C27	URC_SQ_VCCTX0	12		
A26	URC_SQ_HDOUTP0	12		T
A27	URC_SQ_VCCOB0	12		
B26	URC_SQ_HDOUTN0	12		C
C26	URC_SQ_VCCTX1	12		
B25	URC_SQ_HDOUTN1	12		C
C25	URC_SQ_VCCOB1	12		
A25	URC_SQ_HDOUTP1	12		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
VCCIO	VCCIO7	7			VCCIO7	7		
T6	PL44A	7	LDQ46	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*
R6	PL44B	7	LDQ46	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*
U9	PL45A	7	LDQ46	T	PL53A	7	LDQ54	T
T7	PL45B	7	LDQ46	C	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-			GNDIO7	-		
U5	PL46A	7	LDQS46	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*
U6	PL46B	7	LDQ46	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*
U7	PL47A	7	LDQ46	T	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7			VCCIO7	7		
V9	PL47B	7	LDQ46	C	PL55B	7	LDQ54	C
V11	PL48A	7	LDQ46	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*
V10	PL48B	7	LDQ46	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*
U4	PL49A	7	PCLKT7_0/LDQ46	T	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-			GNDIO7	-		
U3	PL49B	7	PCLKC7_0/LDQ46	C	PL57B	7	PCLKC7_0/LDQ54	C
U2	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
U1	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
V5	PL52A	6	VREF2_6/LDQ55	T	PL60A	6	VREF2_6/LDQ63	T
V6	PL52B	6	VREF1_6/LDQ55	C	PL60B	6	VREF1_6/LDQ63	C
V7	PL53A	6	LDQ55	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V8	PL53B	6	LDQ55	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*
V4	PL54A	6	LDQ55	T	PL62A	6	LDQ63	T
V3	PL54B	6	LDQ55	C	PL62B	6	LDQ63	C
V2	PL55A	6	LDQS55	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
V1	PL55B	6	LDQ55	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*
W7	PL56A	6	LDQ55	T	PL64A	6	LDQ63	T
W5	PL56B	6	LDQ55	C	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6			VCCIO6	6		
W2	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	PL65A	6	LLM4_SPLLT_IN_A/LDQ63	T (LVDS)*
W1	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*	PL65B	6	LLM4_SPLLC_IN_A/LDQ63	C (LVDS)*
Y6	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T	PL66A	6	LLM4_SPLLT_FB_A/LDQ63	T
W6	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C	PL66B	6	LLM4_SPLLC_FB_A/LDQ63	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL60A	6	LDQ64	T (LVDS)*	PL68A	6	LDQ72	T (LVDS)*
Y2	PL60B	6	LDQ64	C (LVDS)*	PL68B	6	LDQ72	C (LVDS)*
Y7	PL61A	6	LDQ64	T	PL69A	6	LDQ72	T
Y5	PL61B	6	LDQ64	C	PL69B	6	LDQ72	C
VCCIO	VCCIO6	6			VCCIO6	6		
W10	PL62A	6	LDQ64	T (LVDS)*	PL70A	6	LDQ72	T (LVDS)*
Y8	PL62B	6	LDQ64	C (LVDS)*	PL70B	6	LDQ72	C (LVDS)*
Y4	PL63A	6	LDQ64	T	PL71A	6	LDQ72	T
Y3	PL63B	6	LDQ64	C	PL71B	6	LDQ72	C
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL64A	6	LDQS64	T (LVDS)*	PL72A	6	LDQS72	T (LVDS)*
AA2	PL64B	6	LDQ64	C (LVDS)*	PL72B	6	LDQ72	C (LVDS)*

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12