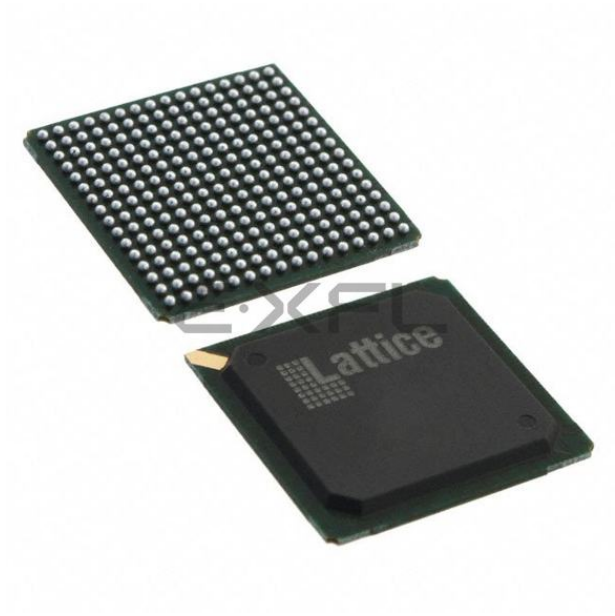

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

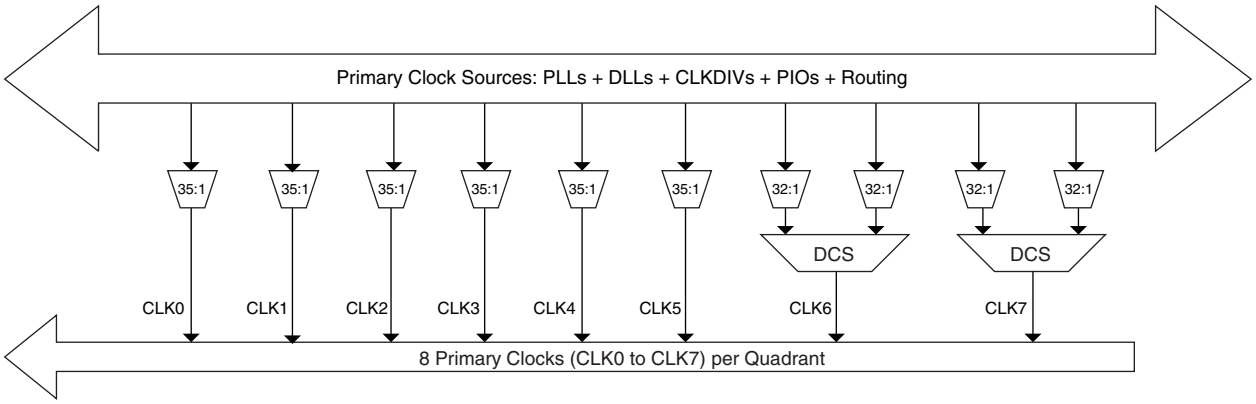
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5f256c

Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

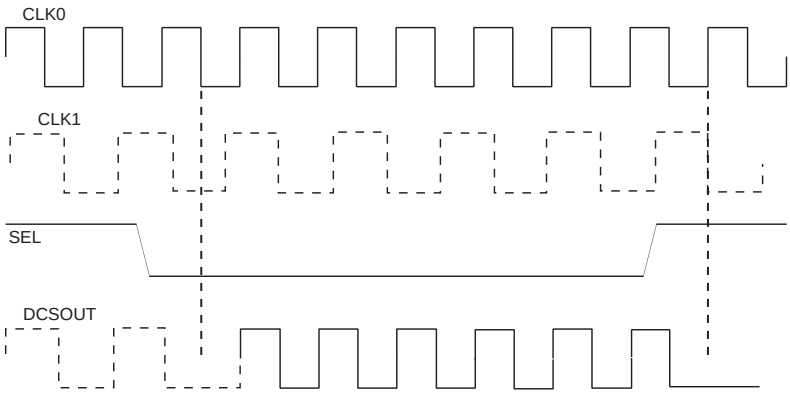


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

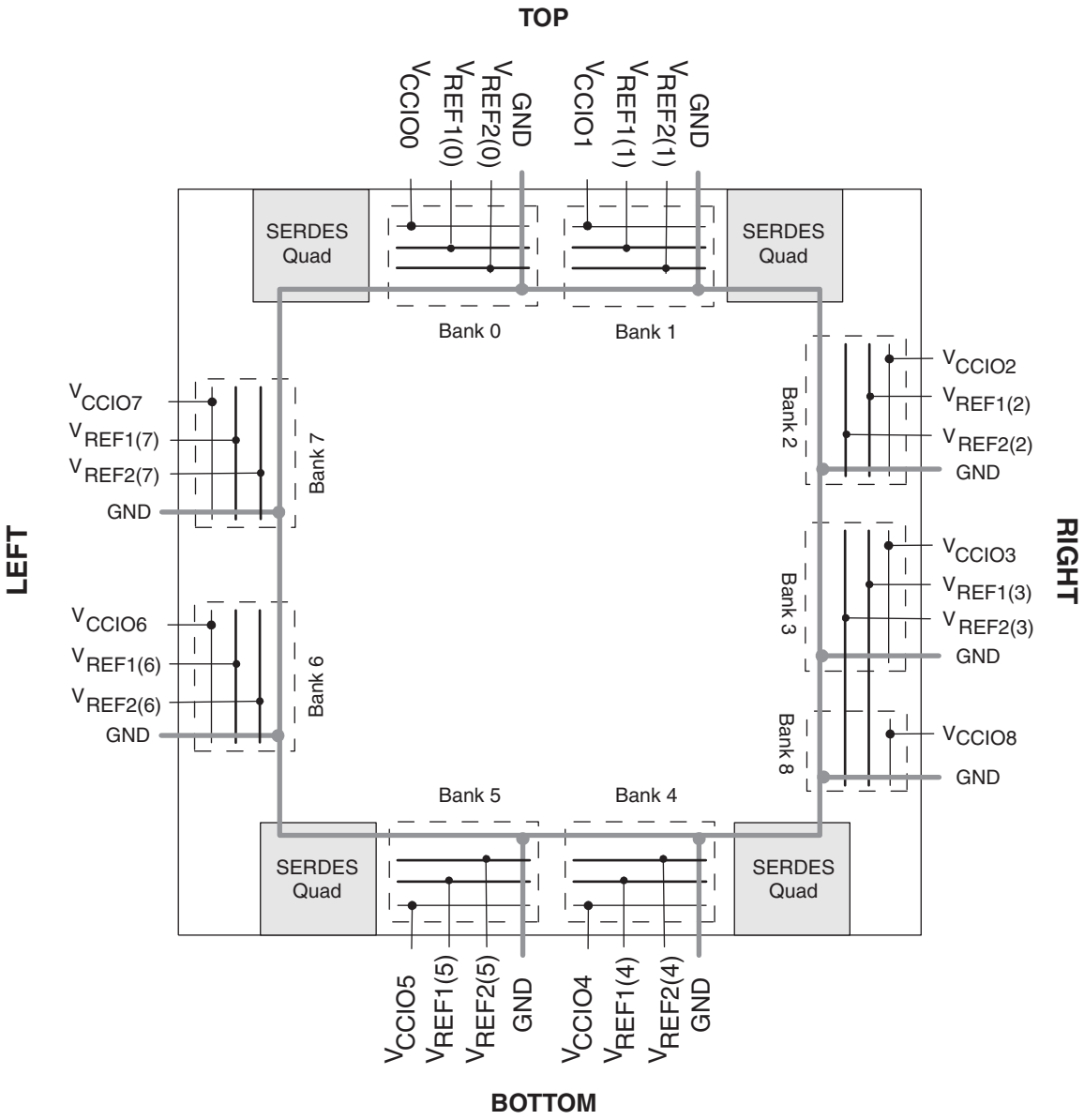
sysI/O Buffer Banks

LatticeECP2/M devices have nine sysI/O buffer banks: eight banks for user I/Os arranged two per side. The ninth sysI/O buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2}, with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-38. LatticeECP2M Banks



LatticeECP2/M devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Bottom (Bank 4 and Bank 5) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the bottom banks of the device consist of two single-ended output drivers and two

Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5
LVCMOS33D[1]	4mA, 8mA, 12mA, 16mA, 20mA	3.3

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

Hot Socketing

LatticeECP2/M devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2/M ideal for many multiple power supply and hot-swap applications.

for checking soft errors (SED) in SRAM. SED can be run on a programmed device when the user logic is not active. If a soft error occurs, during user mode (normal operation) the device can be programmed to either reload from a known good boot image or generate an error signal.

For further information about Soft Error Detect (SED) support, please see the list of additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP2/M devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP2/M device has an internal CMOS oscillator which is used to derive a Master Clock for configuration. The oscillator and the Master Clock run continuously and are available to user logic after configuration is completed. The software default value of the Master Clock is 2.5MHz. Table 2-16 lists all the available Master Configuration Clock frequencies for normal non-encrypted mode and encrypted mode. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the Master Clock frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information about the use of this oscillator for configuration or user mode, please see the list of additional technical documentation at the end of this data sheet.

Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration

Non-Encrypted Mode CCLK (MHz)			Encrypted Mode CCLK (MHz)
2.5[1]	13.0	45.0	2.5[1]
4.3	15.0	55.0	5.4
5.4	20.0	60.0	10.0
6.9	26.0	—	—
8.1	30.0	—	—
9.2	34.0	—	—
10.0	41.0	130.0	—

1. Software default frequency.

Density Shifting

The LatticeECP2/M family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. Design migration between LatticeECP2 and LatticeECP2M families is not possible. For specific requirements relating to sysCONFIG pins of the ECP2M50, M70 and M100, see the Logic Signal Connections tables.

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{HPLL}	Clock to Data Hold - PIO Input Register	LFE2-6	1.00	—	1.20	—	1.40	—	ns
		LFE2-12	1.00	—	1.20	—	1.40	—	ns
		LFE2-20	1.00	—	1.20	—	1.40	—	ns
		LFE2-35	1.00	—	1.20	—	1.40	—	ns
		LFE2-50	1.00	—	1.20	—	1.40	—	ns
		LFE2-70	1.00	—	1.20	—	1.40	—	ns
		LFE2M20	1.00	—	1.20	—	1.40	—	ns
		LFE2M35	1.00	—	1.20	—	1.40	—	ns
		LFE2M50	1.00	—	1.20	—	1.40	—	ns
		LFE2M70	1.00	—	1.20	—	1.40	—	ns
		LFE2M100	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.80	—	2.00	—	2.20	—	ns
		LFE2-12	1.80	—	2.00	—	2.20	—	ns
		LFE2-20	1.80	—	2.00	—	2.20	—	ns
		LFE2-35	1.80	—	2.00	—	2.20	—	ns
		LFE2-50	1.80	—	2.00	—	2.20	—	ns
		LFE2-70	1.80	—	2.00	—	2.20	—	ns
		LFE2M20	1.80	—	2.00	—	2.20	—	ns
		LFE2M35	1.80	—	2.00	—	2.20	—	ns
		LFE2M50	1.90	—	2.10	—	2.30	—	ns
		LFE2M70	1.90	—	2.10	—	2.30	—	ns
		LFE2M100	2.00	—	2.20	—	2.40	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR}	DDR Clock Frequency[6]	ECP2/M	95	200	95	166	95	133	MHz
DDR2 I/O Pin Parameters[3]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor[5, 6]	2	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	20	—	420	MHz
		With external capacitor[5]	5	—	50	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.156	—	210	MHz
		With external capacitor[5]	0.039	—	25	MHz
f_{VCO}	PLL VCO Frequency		640	—	1280	MHz
f_{PFD}	Phase Detector Input Frequency	Without external capacitor	20	—	420	MHz
		With external capacitor[5, 6]	2	—	50	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	±0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	—	±125	ps
		$50 \leq f_{OUT} < 100$ MHz	—		0.025	UIPP
		$f_{OUT} < 50$ MHz	—	—	0.04	UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—	150	µs
		With external capacitor[5]	—	—	500	µs
t_{PA}	Programmable Delay Unit		85	130	360	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor[5]	20	—	—	µs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. f_{OUT} (max) = f_{IN} * 10 for f_{IN} < 5MHz.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		131	193	331	402	331	450
Differential Pair User I/O		62	96	165	200	165	224
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	42	54	60	64	60	68
	Dedicated Pins	3	3	3	3	3	3
VCC		14	7	18	24	16	22
VCCAUX		8	4	16	16	16	16
VCCPLL		0	0	0	0	2	2
VCCIO	Bank0	2	2	4	5	4	5
	Bank1	2	2	4	5	4	5
	Bank2	2	2	4	5	4	5
	Bank3	2	2	4	5	4	5
	Bank4	2	2	4	5	4	5
	Bank5	2	2	4	5	4	5
	Bank6	2	2	4	5	4	5
	Bank7	2	2	4	5	4	5
	Bank8	2	1	2	2	2	2
GND, GND0 to GND7		22	20	60	72	60	72
NC		0	1	8	101	8	102
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	18/9	18/9	50/25	67/33	50/25	67/33
	Bank1	18/9	34/17	46/23	52/26	46/23	52/26
	Bank2	11/5	20/10	34/17	36/18	34/17	48/24
	Bank3	11/5	12/6	22/11	32/16	22/11	42/21
	Bank4	19/9	32/16	46/23	50/25	46/23	54/27
	Bank5	18/9	17/8	46/23	68/34	46/23	68/34
	Bank6	18/8	26/13	40/20	48/24	40/20	58/29
	Bank7	12/6	20/10	33/16	35/17	33/16	47/23
	Bank8	6/2	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	4	5	9	9	9	12
	Bank3 (Right Edge)	3	3	5	8	5	9
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	6	7	10	12	10	13
	Bank7 (Left Edge)	5	5	8	8	8	11
	Bank8 (Right Edge)	0	0	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N14	CFG1	8			CFG1	8		
N13	PROGRAMN	8			PROGRAMN	8		
N15	CFG0	8			CFG0	8		
P15	PR30B	8	WRITEN	C	PR30B	8	WRITEN	C
L12	INITN	8			INITN	8		
N16	PR29B	8	CSN	C	PR29B	8	CSN	C
GND	GNDIO8	-			GNDIO8	-		
R14	CCLK	8			CCLK	8		
P14	PR30A	8	CS1N	T	PR30A	8	CS1N	T
M13	DONE	8			DONE	8		
R16	PR28B	8	D1	C	PR28B	8	D1	C
VCCIO	VCCIO8	8			VCCIO8	8		
M16	PR29A	8	D0/SPIFASTN	T	PR29A	8	D0/SPIFASTN	T
P16	PR28A	8	D2	T	PR28A	8	D2	T
L15	PR27B	8	D3	C	PR27B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
L14	PR26A	8	D6	T	PR26A	8	D6	T
L16	PR27A	8	D4	T	PR27A	8	D4	T
L10	PR25B	8	D7/SPID0	C	PR25B	8	D7/SPID0	C
L13	PR26B	8	D5	C	PR26B	8	D5	C
VCCIO	VCCIO8	8			VCCIO8	8		
K11	PR25A	8	DI/CSSPI0N	T	PR25A	8	DI/CSSPI0N	T
K14	PR24B	8	DOUT/CSON	C	PR24B	8	DOUT/CSON	C
K13	PR24A	8	BUSY/SISPI	T	PR24A	8	BUSY/SISPI	T
GND	GNDIO8	-			GNDIO8	-		
K15	PR21B	3	RLM0_GPLLC_FB_A	C	PR21B	3	RLM0_GPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
K16	PR21A	3	RLM0_GPLLT_FB_A	T	PR21A	3	RLM0_GPLLT_FB_A	T
GND	GNDIO3	-			GNDIO3	-		
J16	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*
J15	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*
J14	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
J13	PR18B	3	RLM0_GDLLC_FB_A	C	PR18B	3	RLM0_GDLLC_FB_A	C
J12	PR18A	3	RLM0_GDLLT_FB_A	T	PR18A	3	RLM0_GDLLT_FB_A	T
H12	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
H13	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
H15	PR16B	3	VREF2_3	C	PR16B	3	VREF2_3	C
VCCIO	VCCIO3	3			VCCIO3	3		
H16	PR16A	3	VREF1_3	T	PR16A	3	VREF1_3	T
H11	PR15B	3	PCLKC3_0	C (LVDS)*	PR15B	3	PCLKC3_0	C (LVDS)*
J11	PR15A	3	PCLKT3_0	T (LVDS)*	PR15A	3	PCLKT3_0	T (LVDS)*
G16	PR13B	2	PCLKC2_0/RDQ10	C	PR13B	2	PCLKC2_0/RDQ10	C
GND	GNDIO2	-			GNDIO2	-		
G15	PR13A	2	PCLKT2_0/RDQ10	T	PR13A	2	PCLKT2_0/RDQ10	T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J1	J1	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
K3	K3	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
J2	J2	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
GND	GND	GNDIO6	-		
L2	L2	PL38A	6	LDQ42	T (LVDS)*
K2	K2	PL39A	6	LDQ42	T
L3	L3	PL38B	6	LDQ42	C (LVDS)*
K1	K1	PL39B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
L4	L4	PL40A	6	LDQ42	T (LVDS)*
L1	L1	PL41A	6	LDQ42	T
L5	L5	PL40B	6	LDQ42	C (LVDS)*
M1	M1	PL41B	6	LDQ42	C
GND	GND	GNDIO6	-		
N1	N1	PL43A	6	LDQ42	T
N2	N2	PL42A	6	LDQS42	T (LVDS)*
P1	P1	PL43B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
P2	P2	PL42B	6	LDQ42	C (LVDS)*
R1	R1	PL44A	6	LDQ42	T (LVDS)*
GND	GND	GNDIO6	-		
R2	R2	PL44B	6	LDQ42	C (LVDS)*
N4	N4	TDI	-		
M4	M4	TCK	-		
P3	P3	TDO	-		
N3	N3	TMS	-		
K7	K7	VCCJ	-		
M5	M5	PB2A	5	VREF2_5/BDQ6	T
K6	K6	PB3A	5	BDQ6	
M6	M6	PB2B	5	VREF1_5/BDQ6	C
R3	R3	PB5A	5	BDQ6	T
P4	P4	PB5B	5	BDQ6	C
-	VCC	VCCIO	5		
-	GND	GNDIO5	5		
N5	N5	PB30A	5	BDQ33	T
N6	N6	PB30B	5	BDQ33	C
T2	T2	PB31A	5	BDQ33	T
P6	P6	PB32A	5	BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
T3	T3	PB31B	5	BDQ33	C
R6	R6	PB32B	5	BDQ33	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB7	PB13B	5	BDQ15	C	PB22B	5	BDQ24	C
Y8	PB16A	5	BDQ15	T	PB25A	5	BDQ24	T
GNDIO	GNDIO5	-			GNDIO	-		
W9	PB15A	5	BDQS15	T	PB24A	5	BDQS24	T
AA8	PB16B	5	BDQ15	C	PB25B	5	BDQ24	C
V9	PB15B	5	BDQ15	C	PB24B	5	BDQ24	C
AB8	PB18A	5	BDQ15	T	PB27A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
W10	PB17A	5	BDQ15	T	PB26A	5	BDQ24	T
AA9	PB18B	5	BDQ15	C	PB27B	5	BDQ24	C
V10	PB17B	5	BDQ15	C	PB26B	5	BDQ24	C
GNDIO	GNDIO5	-			GNDIO	-		
Y10	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AB9	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AB10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
AB11	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U10	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA11	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
U11	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB12	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
Y11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AA12	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W11	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AB13	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AB14	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y12	PB32A	4	BDQ33	T	PB41A	4	BDQ42	T
W12	PB32B	4	BDQ33	C	PB41B	4	BDQ42	C
VCCIO	VCCIO4	4			VCCIO4	4		
U12	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
V12	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
U13	PB34A	4	BDQ33	T	PB43A	4	BDQ42	T
GNDIO	GNDIO4	-			GNDIO4	-		
AA13	PB33A	4	BDQS33	T	PB42A	4	BDQS42	T
U14	PB34B	4	BDQ33	C	PB43B	4	BDQ42	C
Y13	PB33B	4	BDQ33	C	PB42B	4	BDQ42	C
AB16	PB36A	4	BDQ33	T	PB45A	4	BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB15	PB35A	4	BDQ33	T	PB44A	4	BDQ42	T
AB17	PB36B	4	BDQ33	C	PB45B	4	BDQ42	C

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*
B2	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C(LVDS)*
D3	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T
C2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C
E4	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
E5	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C(LVDS)*
B1	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T
C1	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C
D2	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO7	-		
D1	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C(LVDS)*
E1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T
F1	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7			VCCIO7	7		
F3	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*
F2	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C(LVDS)*
F6	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T
F5	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-			GNDIO7	-		
G4	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
G3	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C(LVDS)*
G1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
G2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
H1	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
J1	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C(LVDS)*
H2	PL14A	7		T	PL14A	7	LDQ15	T
H3	PL14B	7		C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
VCCIO	VCCIO7	7			VCCIO7	7		
G6	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*
H6	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C(LVDS)*
J2	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
K1	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C
H4	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*
H5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C(LVDS)*
J4	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T
K4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C
VCCIO	VCCIO6	6			VCCIO6	6		
J6	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
J5	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C(LVDS)*
K3	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T
K2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO6	-			GNDIO6	-		
L1	PL42A	6	LLM0_GPLLT_IN_A	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57***	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
L2	PL42B	6	LLM0_GPLLC_IN_A	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C(LVDS)*
L3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T
L4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C
VCCIO	VCCIO6	6			VCCIO6	6		
M1	PL44A	6	LLM0_GDLLT_IN_A	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*
N1	PL44B	6	LLM0_GDLLC_IN_A	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C(LVDS)*
N2	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T
N3	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C
GNDIO	GNDIO6	-			GNDIO6	-		
M4	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	-			GNDIO6	-		
K6	TCK	-			TCK	-		
L5	TDI	-			TDI	-		
N4	TMS	-			TMS	-		
N6	TDO	-			TDO	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T
N5	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C
L6	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
M6	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
P3	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
P4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
P2	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
P1	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
R1	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	-			GNDIO5	-		
R2	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
R3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
T2	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
R4	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
T4	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
GNDIO	GNDIO5	-			GNDIO5	-		
T5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
T6	PB16A	5	VREF2_5/BDQ15	T	PB34A	5	VREF2_5/BDQ33	T
R6	PB16B	5	VREF1_5/BDQ15	C	PB34B	5	VREF1_5/BDQ33	C
P6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T
P7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
G10	VCCPLL	-			VCCPLL	-		
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
E7	VCCIO0	0			VCCIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
E10	VCCIO1	1			VCCIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
VCCIO	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
VCCIO	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
VCCIO	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
VCCIO	VCCIO8	8			VCCIO8	8		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A15	GND	-			GND	-		
A16	GND	-			GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L4	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*
M1	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
M2	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C
M6	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*
M5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*
M3	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T
M4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C
VCCIO	VCCIO6	6			VCCIO6	6		
N7	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
N6	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*
N1	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T
N2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	-			GNDIO6	-		
P6	PL38A	6	LDQS38****	T (LVDS)*	PL48A	6	LDQS48****	T (LVDS)*
N5	PL38B	6	LDQ38	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*
P1	PL39A	6	LDQ38	T	PL49A	6	LDQ48	T
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL39B	6	LDQ38	C	PL49B	6	LDQ48	C
P3	PL40A	6	LDQ38	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*
P4	PL40B	6	LDQ38	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*
P5	PL41A	6	LDQ38	T	PL51A	6	LDQ48	T
GNDIO	GNDIO6	-			GNDIO6	-		
P7	PL41B	6	LDQ38	C	PL51B	6	LDQ48	C
R1	PL42A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
R2	PL42B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*
R3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T
R4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C
VCCIO	VCCIO6	6			VCCIO6	6		
R6	PL44A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*
R5	PL44B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*
T1	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T
T2	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C
GNDIO	GNDIO6	-			GNDIO6	-		
R7	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
T6	PL47A	6	LDQ51	T (LVDS)*	PL62A	6	LDQ66	T (LVDS)*
T7	PL47B	6	LDQ51	C (LVDS)*	PL62B	6	LDQ66	C (LVDS)*
U1	PL48A	6	LDQ51	T	PL63A	6	LDQ66	T
U2	PL48B	6	LDQ51	C	PL63B	6	LDQ66	C
VCCIO	VCCIO6	6			VCCIO6	6		
T3	PL49A	6	LDQ51	T (LVDS)*	PL64A	6	LDQ66	T (LVDS)*
U3	PL49B	6	LDQ51	C (LVDS)*	PL64B	6	LDQ66	C (LVDS)*
U6	PL50A	6	LDQ51	T	NC	-		
U5	PL50B	6	LDQ51	C	PL65B	6	LDQ66	C
GNDIO	GNDIO6	-			GNDIO6	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L18	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
L20	PR30B	3		C	PR40B	3		C
L19	PR30A	3		T	PR40A	3		T
K16	PR29B	3		C (LVDS)*	PR39B	3		C (LVDS)*
K17	PR29A	3		T (LVDS)*	PR39A	3		T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
J16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
K18	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J22	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J21	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
H22	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
H21	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		
J17	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*
J18	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
J20	PR23B	2	RDQ22	C	PR33B	2	RDQ32	C
J19	PR23A	2	RDQ22	T	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2			VCCIO2	2		
H16	PR22B	2	RDQ22	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*
H17	PR22A	2	RDQS22	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-			GNDIO2	-		
G21	PR21A	2	RDQ22	T	PR31A	2	RDQ32	T
H20	PR20B	2	RDQ22	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*
H19	PR20A	2	RDQ22	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*
G16	PR19B	2	RUM1_SPLLC_FB_A/RDQ22	C	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C
VCCIO	VCCIO2	2			VCCIO2	2		
H18	PR19A	2	RUM1_SPLLT_FB_A/RDQ22	T	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T
F22	PR18B	2	RUM1_SPLLC_IN_A/RDQ22	C (LVDS)*	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*
F21	PR18A	2	RUM1_SPLLT_IN_A/RDQ22	T (LVDS)*	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*
GNDIO	GNDIO2	-			-	-		
G20	PR16B	2		C	PR26B	2	RDQ23	C
VCCIO	VCCIO2	2			-	-		
F20	PR16A	2		T	PR26A	2	RDQ23	T
-	-	-			GNDIO2	-		
G17	PR15B	2		C (LVDS)*	PR25B	2	RDQ23	C (LVDS)*
F17	PR15A	2		T (LVDS)*	PR25A	2	RDQ23	T (LVDS)*
-	-	-			VCCIO2	2		
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR14B	2		C	PR14B	2	RDQ15	C
D22	PR14A	2		T	PR14A	2	RDQ15	T
E20	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*
D20	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
D19	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
E19	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AJ2	LLC_SQ_HDINN3	14		C
AH4	LLC_SQ_VCCTX3	14		
AK5	LLC_SQ_HDOUTP3	14		T
AK4	LLC_SQ_VCCOB3	14		
AJ5	LLC_SQ_HDOUTN3	14		C
AH5	LLC_SQ_VCCTX2	14		
AJ6	LLC_SQ_HDOUTN2	14		C
AH6	LLC_SQ_VCCOB2	14		
AK6	LLC_SQ_HDOUTP2	14		T
AH2	LLC_SQ_VCCRX2	14		
AJ3	LLC_SQ_HDINN2	14		C
AH3	LLC_SQ_VCCIB2	14		
AK3	LLC_SQ_HDINP2	14		T
AH7	LLC_SQ_VCCP	14		
AG7	LLC_SQ_REFCLKP	14		T
AF7	LLC_SQ_REFCLKN	14		C
AJ7	LLC_SQ_VCCAUX33	14		
AK11	LLC_SQ_HDINP1	14		T
AH11	LLC_SQ_VCCIB1	14		
AJ11	LLC_SQ_HDINN1	14		C
AH12	LLC_SQ_VCCRX1	14		
AK8	LLC_SQ_HDOUTP1	14		T
AH8	LLC_SQ_VCCOB1	14		
AJ8	LLC_SQ_HDOUTN1	14		C
AH9	LLC_SQ_VCCTX1	14		
AJ9	LLC_SQ_HDOUTN0	14		C
AK10	LLC_SQ_VCCOB0	14		
AK9	LLC_SQ_HDOUTP0	14		T
AH10	LLC_SQ_VCCTX0	14		
AJ12	LLC_SQ_HDINN0	14		C
AJ13	LLC_SQ_VCCIB0	14		
AK12	LLC_SQ_HDINP0	14		T
AH13	LLC_SQ_VCCRX0	14		
AF10	PB30A	5	BDQ33	T
AE8	PB30B	5	BDQ33	C
AE11	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5		
AD9	PB31B	5	BDQ33	C
AE10	PB32A	5	BDQ33	T
AD10	PB32B	5	BDQ33	C
AE13	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-		
AC12	PB33B	5	BDQ33	C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK20	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
AN22	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
AL21	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AH19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
AJ20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
AD20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
AF20	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ19	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
AH20	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
AE20	PB73A	4	BDQ69	T	PB82A	4	BDQ78	T
AG20	PB73B	4	BDQ69	C	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
AH22	NC	-			PB89A	4	BDQ87	T
-	-	-			VCCIO4	4		
AH21	NC	-			PB89B	4	BDQ87	C
AG22	NC	-			PB90A	4	BDQ87	T
AG21	NC	-			PB90B	4	BDQ87	C
-	-	-			GNDIO4	-		
AM22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T
AL22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AP23	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T
AN23	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AM24	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T
AL24	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C
AK22	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T
AJ22	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C
AL23	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T
AK23	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ23	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T
AH23	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AL28	LRC_SQ_VCCRX3	13			LRC_SQ_VCCRX3	13		
AM26	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T
AN26	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13		
AM27	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C
AN27	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13		
AP26	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T
AL26	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13		
AP27	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C
AN28	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13		
AP28	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C
AK28	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13		
AP29	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W30	PR53A	3	RDQ55	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U27	PR52B	3	VREF2_3/RDQ55	C	PR60B	3	VREF2_3/RDQ63	C
V29	PR52A	3	VREF1_3/RDQ55	T	PR60A	3	VREF1_3/RDQ63	T
V31	PR51B	3	PCLKC3_0/RDQ55	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
V32	PR51A	3	PCLKT3_0/RDQ55	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
V33	PR49B	2	PCLKC2_0/RDQ46	C	PR57B	2	PCLKC2_0/RDQ54	C
V34	PR49A	2	PCLKT2_0/RDQ46	T	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-			GNDIO2	-		
U24	PR48B	2	RDQ46	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
U25	PR48A	2	RDQ46	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
V30	PR47B	2	RDQ46	C	PR55B	2	RDQ54	C
Y32	PR47A	2	RDQ46	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
U28	PR46B	2	RDQ46	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
U29	PR46A	2	RDQS46	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
U33	PR45B	2	RDQ46	C	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-			GNDIO2	-		
U34	PR45A	2	RDQ46	T	PR53A	2	RDQ54	T
T30	PR44B	2	RDQ46	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
U30	PR44A	2	RDQ46	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
T29	PR43B	2	RUM3_SPLLC_FB_A/RDQ46	C	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
T28	PR43A	2	RUM3_SPLLT_FB_A/RDQ46	T	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
U31	PR42B	2	RUM3_SPLLC_IN_A/RDQ46	C (LVDS)*	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
U32	PR42A	2	RUM3_SPLLT_IN_A/RDQ46	T (LVDS)*	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
T33	PR40B	2	RDQ37	C	PR48B	2	RDQ45	C
T34	PR40A	2	RDQ37	T	PR48A	2	RDQ45	T
GNDIO	GNDIO2	-			GNDIO2	-		
R27	PR39B	2	RDQ37	C (LVDS)*	PR47B	2	RDQ45	C (LVDS)*
R28	PR39A	2	RDQ37	T (LVDS)*	PR47A	2	RDQ45	T (LVDS)*
R29	PR38B	2	RDQ37	C	PR46B	2	RDQ45	C
R30	PR38A	2	RDQ37	T	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2			VCCIO2	2		
R33	PR37B	2	RDQ37	C (LVDS)*	PR45B	2	RDQ45	C (LVDS)*
R34	PR37A	2	RDQS37	T (LVDS)*	PR45A	2	RDQS45	T (LVDS)*
R32	PR36B	2	RDQ37	C	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-			GNDIO2	-		
R31	PR36A	2	RDQ37	T	PR44A	2	RDQ45	T
P34	PR35B	2	RDQ37	C (LVDS)*	PR43B	2	RDQ45	C (LVDS)*
P33	PR35A	2	RDQ37	T (LVDS)*	PR43A	2	RDQ45	T (LVDS)*
R26	PR34B	2	RDQ37	C	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2			VCCIO2	2		
T25	PR34A	2	RDQ37	T	PR42A	2	RDQ45	T
P28	PR33B	2	RDQ37	C (LVDS)*	PR41B	2	RDQ45	C (LVDS)*
P27	PR33A	2	RDQ37	T (LVDS)*	PR41A	2	RDQ45	T (LVDS)*
P30	NC	-			PR40B	2		C
-	-	-			GNDIO2	-		
P29	NC	-			PR40A	2		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE12	NC	-			NC	-		
AE13	NC	-			NC	-		
AE19	NC	-			NC	-		
AE21	NC	-			NC	-		
AE22	NC	-			NC	-		
AE23	NC	-			NC	-		
AF11	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
AF24	NC	-			NC	-		
AF8	NC	-			NC	-		
AF9	NC	-			NC	-		
AG10	NC	-			NC	-		
AG11	NC	-			NC	-		
AG24	NC	-			NC	-		
AG25	NC	-			NC	-		
AG26	NC	-			NC	-		
AG3	NC	-			NC	-		
AG7	NC	-			NC	-		
AG8	NC	-			NC	-		
AG9	NC	-			NC	-		
AH10	NC	-			NC	-		
AH11	NC	-			NC	-		
AH13	NC	-			NC	-		
AH24	NC	-			NC	-		
AH25	NC	-			NC	-		
AH26	NC	-			NC	-		
AH27	NC	-			NC	-		
AH5	NC	-			NC	-		
AH6	NC	-			NC	-		
AH7	NC	-			NC	-		
AH8	NC	-			NC	-		
AH9	NC	-			NC	-		
AJ10	NC	-			NC	-		
AJ11	NC	-			NC	-		
AJ13	NC	-			NC	-		
AJ24	NC	-			NC	-		
AJ25	NC	-			NC	-		
AJ26	NC	-			NC	-		
AJ27	NC	-			NC	-		
AJ3	NC	-			NC	-		
AJ4	NC	-			NC	-		
AJ5	NC	-			NC	-		
AJ6	NC	-			NC	-		
AJ7	NC	-			NC	-		
AJ8	NC	-			NC	-		
AJ9	NC	-			NC	-		
AK10	NC	-			NC	-		
AK11	NC	-			NC	-		