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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	193
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5fn256c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5fn256c</a>

## Features

- **High Logic Density for System Integration**
  - 6K to 95K LUTs
  - 90 to 583 I/Os
- **Embedded SERDES (LatticeECP2M Only)**
  - Data Rates 250 Mbps to 3.125 Gbps
  - Up to 16 channels per device  
PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.
- **sysDSP™ Block**
  - 3 to 42 blocks for high performance multiply and accumulate
  - Each block supports
    - One 36x36, four 18x18 or eight 9x9 multipliers
- **Flexible Memory Resources**
  - 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
    - 18Kbit block
    - Single, pseudo dual and true dual port
    - Byte Enable Mode support
  - 12K to 202Kbits distributed RAM
    - Single port and pseudo dual port
- **sysCLOCK Analog PLLs and DLLs**
  - Two GPLLs and up to six SPLLs per device
    - Clock multiply, divide, phase & delay adjust
    - Dynamic PLL adjustment
  - Two general purpose DLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - Source synchronous standards support
    - SPI4.2, SF14 (DDR Mode), XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR and DDR2 memory support
    - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
  - Dedicated DQS support
- **Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces**
  - LVTTTL and LVCMOS 33/25/18/15/12
  - SSTL 3/2/18 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL
- **Flexible Device Configuration**
  - 1149.1 Boundary Scan compliant
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual boot images supported
  - TransFR™ I/O for simple field updates
  - Soft Error Detect macro embedded
- **Optional Bitstream Encryption (LatticeECP2/M “S” Versions Only)**
- **System Level Support**
  - ispTRACY™ internal logic analyzer capability
  - On-chip oscillator for initialization & general use
  - 1.2V power supply

**Table 1-1. LatticeECP2 (Including “S-Series”) Family Selection**

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
<b>Packages and I/O Combinations</b>						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

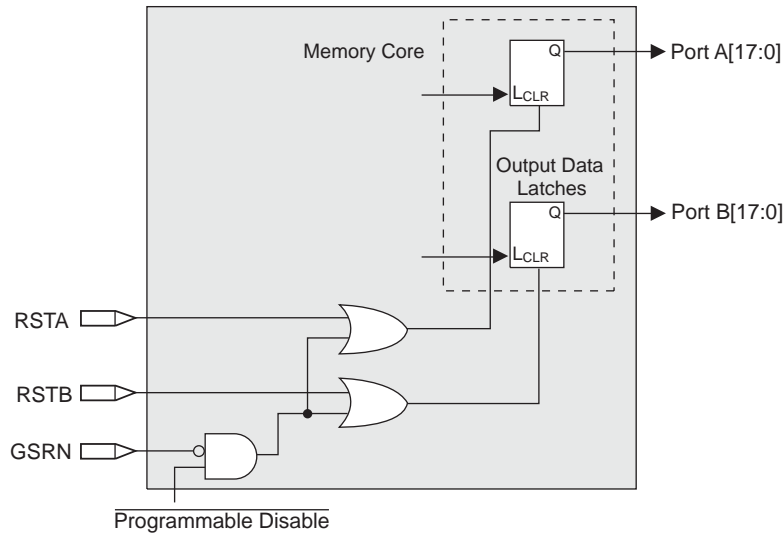
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- Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

### Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

**Figure 2-20. Memory Core Reset**

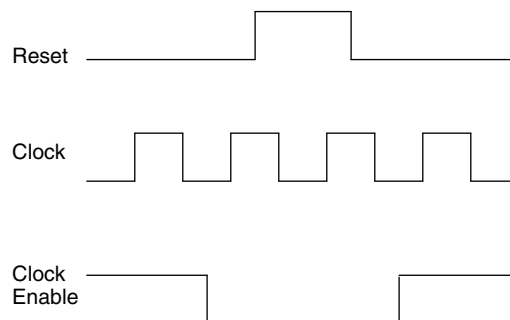


For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

### EBR Asynchronous Reset

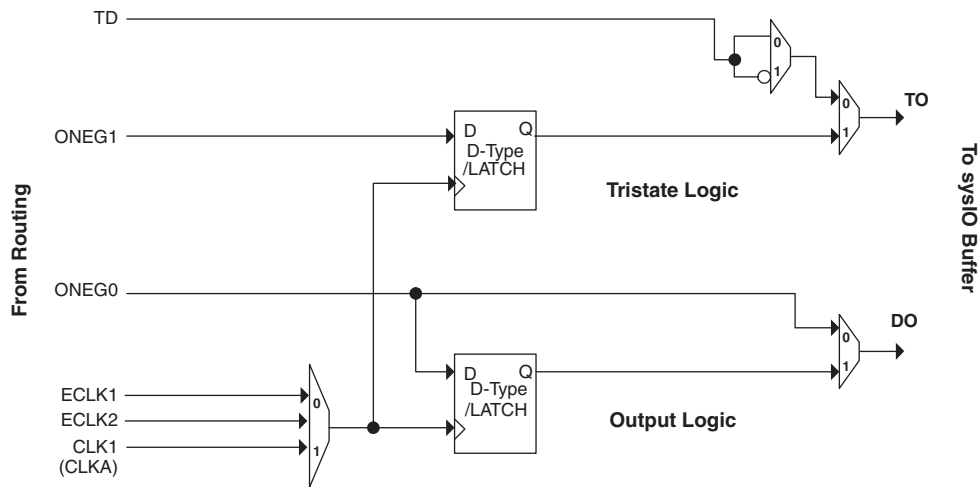
EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

**Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram**



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of  $1/f_{MAX}$  (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Figure 2-32. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

## Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sys/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (DO).

## Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

## DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by the edge of the device as detailed below.

### Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

### Bottom Edge

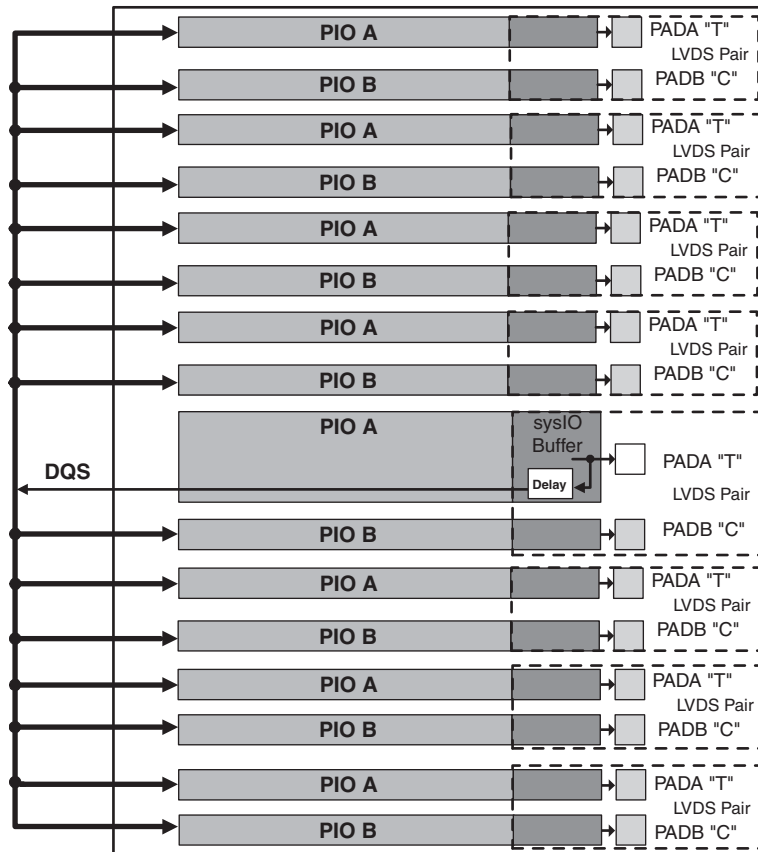
PICs on the bottom edge have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

### Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

**Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device**



**LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)**

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
138	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	
139	GND	-			GND	-			
140	VCC	-			VCC	-			
141	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C	
142	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T	
143	VCCIO2	2			VCCIO2	2			
144	PR12A	2	RDQ10		PR16A	2	RDQS16		
145	GND	-			GND	-			
146	VCC	-			VCC	-			
147	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*	
148	VCCIO2	2			VCCIO2	2			
149	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*	
150	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*	
151	VCCAUX	-			VCCAUX	-			
152	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*	
153	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*	
154	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
155	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
156	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
157	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
158	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
159	GND	-			GND	-			
160	PT54B	1		C	PT62B	1		C	
161	PT54A	1		T	PT62A	1		T	
162	VCCIO1	1			VCCIO1	1			
163	PT52B	1		C	PT60B	1		C	
164	PT52A	1		T	PT60A	1		T	
165	PT50B	1		C	PT58B	1		C	
166	PT50A	1		T	PT58A	1		T	
167	PT48B	1		C	PT56B	1		C	
168	PT48A	1		T	PT56A	1		T	
169	GND	-			GND	-			
170	VCCIO1	1			VCCIO1	1			
171	VCC	-			VCC	-			
172	PT40B	1		C	PT50B	1		C	
173	PT40A	1		T	PT50A	1		T	
174	VCCAUX	-			VCCAUX	-			
175	GND	-			GND	-			
176	PT36B	1		C	PT44B	1		C	
177	PT36A	1		T	PT44A	1		T	
178	PT34B	1		C	PT42B	1		C	
179	PT34A	1		T	PT42A	1		T	
180	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C	
181	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T	
182	XRES	1			XRES	1			
183	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C	

**LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)**

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C	
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*	
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T	
VCCIO	VCCIO2	2			VCCIO2	2			
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*	
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*	
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*	
GND	GNDIO2	-			GNDIO2	-			
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*	
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C	
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*	
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T	
VCCIO	VCCIO2	2			VCCIO2	2			
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C	
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T	
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*	
C16	PR5B	2		C	PR5B	2		C	
GND	GNDIO2	-			GNDIO2	-			
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*	
B16	PR5A	2		T	PR5A	2		T	
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C	
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T	
GND	GNDIO1	-			GNDIO1	-			
A15	PT27B	1		C	PT54B	1		C	
E12	PT26B	1		C	PT53B	1		C	
B15	PT27A	1		T	PT54A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D12	PT26A	1		T	PT53A	1		T	
B14	PT25B	1		C	PT52B	1		C	
C14	PT24B	1		C	PT51B	1		C	
A14	PT25A	1		T	PT52A	1		T	
D13	PT24A	1		T	PT51A	1		T	
C13	PT23B	1		C	PT50B	1		C	
GND	GNDIO1	-			GNDIO1	-			
A13	PT22B	1		C	PT49B	1		C	
B13	PT23A	1		T	PT50A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A12	PT22A	1		T	PT49A	1		T	
B11	PT21B	1		C	PT48B	1		C	
D11	PT20B	1		C	PT47B	1		C	
A11	PT21A	1		T	PT48A	1		T	
C11	PT20A	1		T	PT47A	1		T	

**LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA  
 (Cont.)**

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F19	PR5A	2		T	PR7A	2	RDQ8	T
D20	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*
F18	PR3B	2		C	PR5B	2	RDQ8	C
VCCIO	VCCIO2	2			VCCIO2	2		
C21	NC	-			PR4B	2	RDQ8	C (LVDS)*
F16	PR3A	2		T	PR5A	2	RDQ8	T
C22	NC	-			PR4A	2	RDQ8	T (LVDS)*
-	-	-			GNDIO	-		
D19	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
E19	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
B21	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C
B22	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T
GNDIO	GNDIO1	-			GNDIO1	-		
D18	PT53B	1		C	PT62B	1		C
C20	PT54B	1		C	PT63B	1		C
E18	PT53A	1		T	PT62A	1		T
C19	PT54A	1		T	PT63A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D17	PT51B	1		C	PT60B	1		C
B20	PT52B	1		C	PT61B	1		C
C18	PT51A	1		T	PT60A	1		T
A19	PT52A	1		T	PT61A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A18	PT49B	1		C	PT58B	1		C
A21	PT50B	1		C	PT59B	1		C
B18	PT49A	1		T	PT58A	1		T
A20	PT50A	1		T	PT59A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D16	PT47B	1		C	PT56B	1		C
G16	PT48B	1		C	PT57B	1		C
E16	PT47A	1		T	PT56A	1		T
G15	PT48A	1		T	PT57A	1		T
C17	PT46B	1		C	PT55B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
C16	PT46A	1		T	PT55A	1		T
A17	PT44B	1		C	PT53B	1		C
B17	PT45B	1		C	PT54B	1		C
A16	PT44A	1		T	PT53A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B16	PT45A	1		T	PT54A	1		T
E15	PT42B	1		C	PT51B	1		C
C15	PT43B	1		C	PT52B	1		C
F15	PT42A	1		T	PT51A	1		T
D15	PT43A	1		T	PT52A	1		T



**LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA**  
**(Cont.)**

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W20	CFG0	8			CFG0	8		
V20	PROGRAMN	8			PROGRAMN	8		
W22	CCLK	8			CCLK	8		
V22	INITN	8			INITN	8		
V21	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
R16	PR58B	8	WRITEN	C	PR77B	8	WRITEN	C
R17	PR58A	8	CS1N	T	PR77A	8	CS1N	T
U19	PR57B	8	CSN	C	PR76B	8	CSN	C
U20	PR57A	8	D0/SPIFASTN	T	PR76A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO	8		
U22	PR56B	8	D1	C	PR75B	8	D1	C
U21	PR56A	8	D2	T	PR75A	8	D2	T
T20	PR55B	8	D3	C	PR74B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
T19	PR55A	8	D4	T	PR74A	8	D4	T
T17	PR54B	8	D5	C	PR73B	8	D5	C
T18	PR54A	8	D6	T	PR73A	8	D6	T
T21	PR53B	8	D7/SPID0	C	PR72B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO	8		
T22	PR53A	8	DI/CSSPION	T	PR72A	8	DI/CSSPION	T
R18	PR52B	8	DOUT/CSON	C	PR71B	8	DOUT/CSON	C
R19	PR52A	8	BUSY/SISPI	T	PR71A	8	BUSY/SISPI	T
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO	3		
R22	PR47B	3	RDQ48	C	PR66B	3	RDQ67	C
R21	PR47A	3	RDQ48	T	PR66A	3	RDQ67	T
P18	PR46B	3	RDQ48	C (LVDS)*	PR65B	3	RDQ67	C (LVDS)*
P19	PR46A	3	RDQ48	T (LVDS)*	PR65A	3	RDQ67	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
R20	PR45B	3	RLM0_GPLL_C_FB_A/RDQ48	C	PR64B	3	RLM0_GPLL_C_FB_A/RDQ67	C
P22	PR45A	3	RLM0_GPLL_T_FB_A/RDQ48	T	PR64A	3	RLM0_GPLL_T_FB_A/RDQ67	T
P21	PR44B	3	RLM0_GPLL_C_IN_A**/RDQ48	C (LVDS)*	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*
N21	PR44A	3	RLM0_GPLL_T_IN_A**/RDQ48	T (LVDS)*	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR42B	3	RLM0_GDLL_C_FB_A/RDQ39	C	PR61B	3	RLM0_GDLL_C_FB_A/RDQ58	C
N20	PR42A	3	RLM0_GDLL_T_FB_A/RDQ39	T	PR61A	3	RLM0_GDLL_T_FB_A/RDQ58	T
GNDIO	GNDIO3	-			GNDIO3	-		
M22	PR41B	3	RLM0_GDLL_C_IN_A**/RDQ39	C (LVDS)*	PR60B	3	RLM0_GDLL_C_IN_A**/RDQ58	C (LVDS)*
M21	PR41A	3	RLM0_GDLL_T_IN_A**/RDQ39	T (LVDS)*	PR60A	3	RLM0_GDLL_T_IN_A**/RDQ58	T (LVDS)*
N19	PR40B	3	RDQ39	C	PR59B	3	RDQ58	C
M19	PR40A	3	RDQ39	T	PR59A	3	RDQ58	T
VCCIO	VCCIO3	3			VCCIO	3		
GNDIO	GNDIO3	-			GNDIO3	-		
L22	PR30B	3	RDQ31	C	PR49B	3	RDQ50	C
K22	PR30A	3	RDQ31	T	PR49A	3	RDQ50	T

**LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA  
 (Cont.)**

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C	
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T	
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C	
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T	
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T	
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C	
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T	
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	NC	-			PB56A	4	BDQ60	T	
W17	NC	-			PB56B	4	BDQ60	C	
Y19	NC	-			PB57A	4	BDQ60	T	
Y17	NC	-			PB57B	4	BDQ60	C	
AF20	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	NC	-			NC	-			
AA20	NC	-			NC	-			
W18	NC	-			NC	-			
AD20	NC	-			NC	-			
GND	GNDIO4	-			GNDIO4	-			
AE21	NC	-			NC	-			
AF21	NC	-			NC	-			
AF22	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	

**LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA**  
**(Cont.)**

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
VCCIO	VCCIO3	3			VCCIO3	3			
U20	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T	PR63A	3	RLM0_GPLLT_IN_A	T	
W24	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C (LVDS)*	PR62B	3	RLM0_GPLLC_FB_A	C*	
V24	PR57A	3	RLM0_GPLLT_FB_A/RDQS57	T (LVDS)*	PR62A	3	RLM0_GPLLT_FB_A	T*	
GNDIO	GNDIO3	-			GNDIO3	-			
U21	PR56A	3	RDQ57	T	PR60A	3		T	
W25	PR55B	3	RDQ57	C (LVDS)*	PR59B	3		C*	
W26	PR55A	3	RDQ57	T (LVDS)*	PR59A	3		T*	
VCCIO	VCCIO3	3			VCCIO3	3			
U18	PR54B	3	RDQ57	C	PR58B	3		C	
U22	PR54A	3	RDQ57	T	PR58A	3		T	
V25	PR53B	3	RDQ57	C (LVDS)*	PR57B	3		C*	
V26	PR53A	3	RDQ57	T (LVDS)*	PR57A	3		T*	
U24	PR51B	3	RDQ48	C	PR55B	3	RDQ52	C	
T24	PR51A	3	RDQ48	T	PR55A	3	RDQ52	T	
GNDIO	GNDIO3	-			GNDIO3	-			
T22	PR50B	3	RDQ48	C (LVDS)*	PR54B	3	RDQ52	C*	
T23	PR50A	3	RDQ48	T (LVDS)*	PR54A	3	RDQ52	T*	
U25	PR49B	3	RDQ48	C	PR53B	3	RDQ52	C	
U26	PR49A	3	RDQ48	T	PR53A	3	RDQ52	T	
VCCIO	VCCIO3	3			VCCIO3	3			
T19	PR48B	3	RDQ48	C (LVDS)*	PR52B	3	RDQ52	C*	
R19	PR48A	3	RDQS48	T (LVDS)*	PR52A	3	RDQS52	T*	
R21	PR47B	3	RDQ48	C	PR51B	3	RDQ52	C	
GNDIO	GNDIO3	-			GNDIO3	-			
R20	PR47A	3	RDQ48	T	PR51A	3	RDQ52	T	
T26	PR46B	3	RDQ48	C (LVDS)*	PR50B	3	RDQ52	C*	
R26	PR46A	3	RDQ48	T (LVDS)*	PR50A	3	RDQ52	T*	
P21	PR45B	3	RDQ48	C	PR49B	3	RDQ52	C	
VCCIO	VCCIO3	3			VCCIO3	3			
P19	PR45A	3	RDQ48	T	PR49A	3	RDQ52	T	
R23	PR44B	3	RDQ48	C (LVDS)*	PR48B	3	RDQ52	C*	
R24	PR44A	3	RDQ48	T (LVDS)*	PR48A	3	RDQ52	T*	
-	-	-			GNDIO3	-			
R22	PR42B	3	RLM2_SPLLC_FB_A	C	PR46B	3	RLM3_SPLLC_FB_A	C	
VCCIO	VCCIO3	3			VCCIO3	3			
N19	PR42A	3	RLM2_SPLLT_FB_A	T	PR46A	3	RLM3_SPLLT_FB_A	T	
P23	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*	PR45B	3	RLM3_SPLLC_IN_A	C*	
P24	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*	PR45A	3	RLM3_SPLLT_IN_A	T*	
GNDIO	GNDIO3	-			GNDIO3	-			
N21	PR40B	3		C	PR44B	3		C	
P22	PR40A	3		T	PR44A	3		T	
N20	PR39B	3		C (LVDS)*	PR43B	3		C*	
N22	PR39A	3		T (LVDS)*	PR43A	3		T*	
VCCIO	VCCIO3	3			VCCIO3	3			
P25	PR38B	3	VREF2_3	C	PR42B	3	VREF2_3	C	
P26	PR38A	3	VREF1_3	T	PR42A	3	VREF1_3	T	
M21	PR37B	3	PCLKC3_0	C (LVDS)*	PR41B	3	PCLKC3_0	C*	

**LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA**  
**(Cont.)**

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C15	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B15	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C14	URC_SQ_VCCR2	12			URC_SQ_VCCR2	12			
A18	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C18	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B18	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C17	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B17	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A16	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A17	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T	
C16	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B14	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B13	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A14	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C13	URC_SQ_VCCR3	12			URC_SQ_VCCR3	12			
-	-	-			GNDIO1	-			
-	-	-			VCCIO1	1			
E17	PT46B	1		C	PT55B	1		C	
D17	PT46A	1		T	PT55A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
F17	PT45B	1		C	PT54B	1		C	
D16	PT45A	1		T	PT54A	1		T	
F19	PT44B	1		C	PT53B	1		C	
F18	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
E16	PT43B	1		C	PT52B	1		C	
D15	PT43A	1		T	PT52A	1		T	
G18	PT42B	1		C	PT51B	1		C	
E15	PT42A	1		T	PT51A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
G17	PT41B	1		C	PT50B	1		C	
E14	PT41A	1		T	PT50A	1		T	
D14	PT40B	1		C	PT49B	1		C	
D13	PT40A	1		T	PT49A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
F15	PT39B	1	VREF2_1	C	PT48B	1	VREF2_1	C	
E12	PT39A	1	VREF1_1	T	PT48A	1	VREF1_1	T	
H17	PT38B	1	PCLKC1_0	C	PT47B	1	PCLKC1_0	C	
E13	PT38A	1	PCLKT1_0	T	PT47A	1	PCLKT1_0	T	
C12	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
G15	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T	
C11	PT36B	0	VREF2_0	C	PT45B	0	VREF2_0	C	
F14	PT36A	0	VREF1_0	T	PT45A	0	VREF1_0	T	

**LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA  
 (Cont.)**

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P16	GND	-			GND	-		
P17	GND	-			GND	-		
P18	GND	-			GND	-		
P20	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
R15	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R20	GND	-			GND	-		
R21	GND	-			GND	-		
R24	GND	-			GND	-		
R7	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T13	GND	-			GND	-		
T14	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T20	GND	-			GND	-		
T21	GND	-			GND	-		
T24	GND	-			GND	-		
T7	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U20	GND	-			GND	-		
V14	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V27	GND	-			GND	-		
V4	GND	-			GND	-		
W23	GND	-			GND	-		
W8	GND	-			GND	-		
Y14	GND	-			GND	-		

**LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)**

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AC19	PB96A	4	BDQS96	T
AD20	PB96B	4	BDQ96	C
AB18	PB97A	4	BDQ96	T
AC20	PB97B	4	BDQ96	C
AE20	PB98A	4	BDQ96	T
AE21	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4		
AC23	PB99A	4	BDQ96	T
AD23	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-		
AH18	LRC_SQ_VCCR3	13		
AK19	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOUTP3	13		T
AK21	LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOUTN3	13		C
AH22	LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOUTN2	13		C
AH23	LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOUTP2	13		T
AH19	LRC_SQ_VCCR2	13		
AJ20	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCR1	13		
AK25	LRC_SQ_HDOUTP1	13		T
AH25	LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOUTN1	13		C
AH26	LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOUTN0	13		C
AK27	LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOUTP0	13		T
AH27	LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C

**LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)**

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AE23	NC	-		
AE5	NC	-		
AE6	NC	-		
AE7	NC	-		
AF20	NC	-		
AF23	NC	-		
AF5	NC	-		
AG23	NC	-		
AG26	NC	-		
D10	NC	-		
E10	NC	-		
E11	NC	-		
F10	NC	-		
F20	NC	-		
F23	NC	-		
F8	NC	-		
G10	NC	-		
G20	NC	-		
G21	NC	-		
G7	NC	-		
G8	NC	-		
G9	NC	-		
H19	NC	-		
H20	NC	-		
H21	NC	-		
H22	NC	-		
H6	NC	-		
H8	NC	-		
H9	NC	-		
J10	NC	-		
J20	NC	-		
J21	NC	-		
J9	NC	-		
K9	NC	-		
R9	NC	-		
U22	NC	-		
W9	NC	-		
N13	VCCPLL	-		
N18	VCCPLL	-		
V13	VCCPLL	-		

**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		



**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF1	PL78B	6	LDQ82	C (LVDS)*	PL95B	6	LDQ99	C (LVDS)*
AE5	PL79A	6	LDQ82	T	PL96A	6	LDQ99	T
AE6	PL79B	6	LDQ82	C	PL96B	6	LDQ99	C
AF4	PL80A	6	LDQ82	T (LVDS)*	PL97A	6	LDQ99	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AF3	PL80B	6	LDQ82	C (LVDS)*	PL97B	6	LDQ99	C (LVDS)*
AF5	PL81A	6	LDQ82	T	PL98A	6	LDQ99	T
AF6	PL81B	6	LDQ82	C	PL98B	6	LDQ99	C
AG1	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	PL99A	6	LLM0_GPLLT_IN_A**/ LDQS99	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AG2	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	PL99B	6	LLM0_GPLLC_IN_A**/LDQ99	C (LVDS)*
AE9	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	PL100A	6	LLM0_GPLLT_FB_A/LDQ99	T
AF7	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	PL100B	6	LLM0_GPLLC_FB_A/LDQ99	C
VCCIO	VCCIO6	6			VCCIO6	6		
AH1	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	PL101A	6	LLM0_GDLLT_IN_A**/LDQ99	T (LVDS)*
AH2	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	PL101B	6	LLM0_GDLLC_IN_A**/ LDQ99	C (LVDS)*
AG5	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	PL102A	6	LLM0_GDLLT_FB_A/LDQ99	T
AG4	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	PL102B	6	LLM0_GDLLC_FB_A/LDQ99	C
GNDIO	GNDIO6	-			GNDIO6	-		
AG6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
AJ1	PL87A	6		T	PL104A	6		T
AJ2	PL87B	6		C	PL104B	6		C
AK2	TCK	-			TCK	-		
AK1	TDI	-			TDI	-		
AL1	TMS	-			TMS	-		
AF10	TDO	-			TDO	-		
AK3	VCCJ	-			VCCJ	-		
AN2	LLC_SQ_VCCRX3	14			LLC_SQ_VCCRX3	14		
AM2	LLC_SQ_HDINP3	14		T	LLC_SQ_HDINP3	14		T
AN1	LLC_SQ_VCCIB3	14			LLC_SQ_VCCIB3	14		
AM3	LLC_SQ_HDINN3	14		C	LLC_SQ_HDINN3	14		C
AN3	LLC_SQ_VCCTX3	14			LLC_SQ_VCCTX3	14		
AP2	LLC_SQ_HDOU3P3	14		T	LLC_SQ_HDOU3P3	14		T
AM1	LLC_SQ_VCCOB3	14			LLC_SQ_VCCOB3	14		
AP3	LLC_SQ_HDOU3N3	14		C	LLC_SQ_HDOU3N3	14		C
AN4	LLC_SQ_VCCTX2	14			LLC_SQ_VCCTX2	14		
AP4	LLC_SQ_HDOU2N2	14		C	LLC_SQ_HDOU2N2	14		C
AL3	LLC_SQ_VCCOB2	14			LLC_SQ_VCCOB2	14		
AP5	LLC_SQ_HDOU2P2	14		T	LLC_SQ_HDOU2P2	14		T
AN5	LLC_SQ_VCCRX2	14			LLC_SQ_VCCRX2	14		
AM4	LLC_SQ_HDINN2	14		C	LLC_SQ_HDINN2	14		C
AL4	LLC_SQ_VCCIB2	14			LLC_SQ_VCCIB2	14		
AM5	LLC_SQ_HDINP2	14		T	LLC_SQ_HDINP2	14		T
AL6	LLC_SQ_VCCP	14			LLC_SQ_VCCP	14		
AL5	LLC_SQ_REFCLKP	14		T	LLC_SQ_REFCLKP	14		T
AK5	LLC_SQ_REFCLKN	14		C	LLC_SQ_REFCLKN	14		C
AK6	LLC_SQ_VCCAUX33	14			LLC_SQ_VCCAUX33	14		
AM6	LLC_SQ_HDINP1	14		T	LLC_SQ_HDINP1	14		T

**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK20	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
AN22	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
AL21	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AH19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
AJ20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
AD20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
AF20	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ19	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
AH20	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
AE20	PB73A	4	BDQ69	T	PB82A	4	BDQ78	T
AG20	PB73B	4	BDQ69	C	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
AH22	NC	-			PB89A	4	BDQ87	T
-	-	-			VCCIO4	4		
AH21	NC	-			PB89B	4	BDQ87	C
AG22	NC	-			PB90A	4	BDQ87	T
AG21	NC	-			PB90B	4	BDQ87	C
-	-	-			GNDIO4	-		
AM22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T
AL22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AP23	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T
AN23	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AM24	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T
AL24	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C
AK22	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T
AJ22	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C
AL23	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T
AK23	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ23	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T
AH23	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AL28	LRC_SQ_VCCR3	13			LRC_SQ_VCCR3	13		
AM26	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T
AN26	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13		
AM27	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C
AN27	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13		
AP26	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T
AL26	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13		
AP27	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C
AN28	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13		
AP28	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C
AK28	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13		
AP29	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T

**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA**  
**(Cont.)**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P31	NC	-			PR39B	2		C (LVDS)*
P32	NC	-			PR39A	2		T (LVDS)*
R25	NC	-			PR38B	2		C
-	-	-			VCCIO2	2		
T24	NC	-			PR38A	2		T
N34	NC	-			PR37B	2		C (LVDS)*
N33	NC	-			PR37A	2		T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
M34	PR31B	2	RDQ28	C	PR35B	2	RDQ32	C
M33	PR31A	2	RDQ28	T	PR35A	2	RDQ32	T
-	-	-			GNDIO2	-		
R24	PR30B	2	RDQ28	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*
P24	PR30A	2	RDQ28	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
N30	PR29B	2	RDQ28	C	PR33B	2	RDQ32	C
M29	PR29A	2	RDQ28	T	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2			VCCIO2	2		
N28	PR28B	2	RDQ28	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*
N29	PR28A	2	RDQS28	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
N24	PR27B	2	RDQ28	C	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-			GNDIO2	-		
N25	PR27A	2	RDQ28	T	PR31A	2	RDQ32	T
M28	PR26B	2	RDQ28	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*
M27	PR26A	2	RDQ28	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*
L27	PR25B	2	RDQ28	C	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2			VCCIO2	2		
M26	PR25A	2	RDQ28	T	PR29A	2	RDQ32	T
M32	PR24B	2	RDQ28	C (LVDS)*	PR28B	2	RDQ32	C (LVDS)*
M31	PR24A	2	RDQ28	T (LVDS)*	PR28A	2	RDQ32	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
-	-	-			VCCIO2	2		
L34	PR22B	2		C	PR22B	2	RDQ23	C
L33	PR22A	2		T	PR22A	2	RDQ23	T
L32	PR21B	2		C (LVDS)*	PR21B	2	RDQ23	C (LVDS)*
L31	PR21A	2		T (LVDS)*	PR21A	2	RDQ23	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
L28	PR20B	2		C	PR20B	2	RDQ23	C
L29	PR20A	2		T	PR20A	2	RDQ23	T
M30	PR19B	2		C (LVDS)*	PR19B	2	RDQ23	C (LVDS)*
L30	PR19A	2		T (LVDS)*	PR19A	2	RDQ23	T (LVDS)*
K34	PR18B	2	RDQ15	C	PR18B	2	RDQ15	C
K33	PR18A	2	RDQ15	T	PR18A	2	RDQ15	T
GNDIO	GNDIO2	-			GNDIO2	-		
K30	PR17B	2	RDQ15	C (LVDS)*	PR17B	2	RDQ15	C (LVDS)*
K29	PR17A	2	RDQ15	T (LVDS)*	PR17A	2	RDQ15	T (LVDS)*
J34	PR16B	2	RDQ15	C	PR16B	2	RDQ15	C
J33	PR16A	2	RDQ15	T	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2			VCCIO2	2		
J32	PR15B	2	RDQ15	C (LVDS)*	PR15B	2	RDQ15	C (LVDS)*
J31	PR15A	2	RDQS15	T (LVDS)*	PR15A	2	RDQS15	T (LVDS)*

**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE12	NC	-			NC	-		
AE13	NC	-			NC	-		
AE19	NC	-			NC	-		
AE21	NC	-			NC	-		
AE22	NC	-			NC	-		
AE23	NC	-			NC	-		
AF11	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
AF24	NC	-			NC	-		
AF8	NC	-			NC	-		
AF9	NC	-			NC	-		
AG10	NC	-			NC	-		
AG11	NC	-			NC	-		
AG24	NC	-			NC	-		
AG25	NC	-			NC	-		
AG26	NC	-			NC	-		
AG3	NC	-			NC	-		
AG7	NC	-			NC	-		
AG8	NC	-			NC	-		
AG9	NC	-			NC	-		
AH10	NC	-			NC	-		
AH11	NC	-			NC	-		
AH13	NC	-			NC	-		
AH24	NC	-			NC	-		
AH25	NC	-			NC	-		
AH26	NC	-			NC	-		
AH27	NC	-			NC	-		
AH5	NC	-			NC	-		
AH6	NC	-			NC	-		
AH7	NC	-			NC	-		
AH8	NC	-			NC	-		
AH9	NC	-			NC	-		
AJ10	NC	-			NC	-		
AJ11	NC	-			NC	-		
AJ13	NC	-			NC	-		
AJ24	NC	-			NC	-		
AJ25	NC	-			NC	-		
AJ26	NC	-			NC	-		
AJ27	NC	-			NC	-		
AJ3	NC	-			NC	-		
AJ4	NC	-			NC	-		
AJ5	NC	-			NC	-		
AJ6	NC	-			NC	-		
AJ7	NC	-			NC	-		
AJ8	NC	-			NC	-		
AJ9	NC	-			NC	-		
AK10	NC	-			NC	-		
AK11	NC	-			NC	-		

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<b>Part Number</b>	<b>I/Os</b>	<b>Voltage</b>	<b>Grade</b>	<b>Package</b>	<b>Pins</b>	<b>Temp.</b>	<b>LUTs (K)</b>
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100