Lattice Semiconductor Corporation - LFE2-20SE-5Q208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

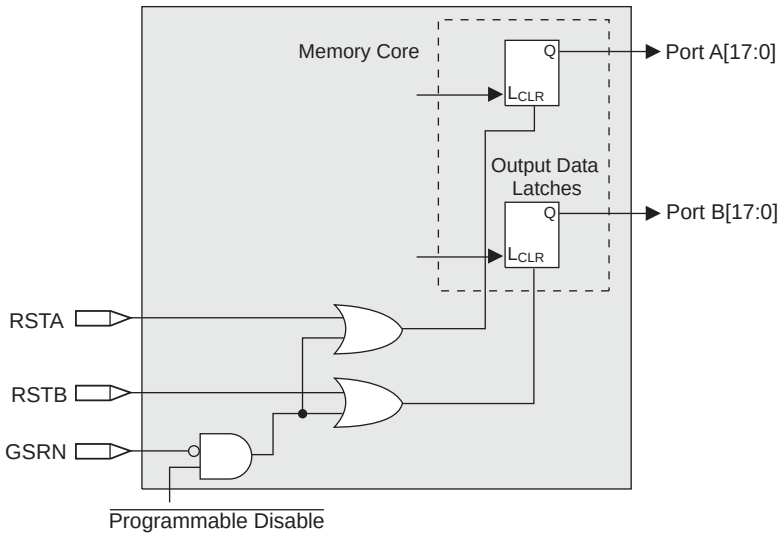
Details	
Product Status	Obsolete
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5q208c

2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

Figure 2-20. Memory Core Reset

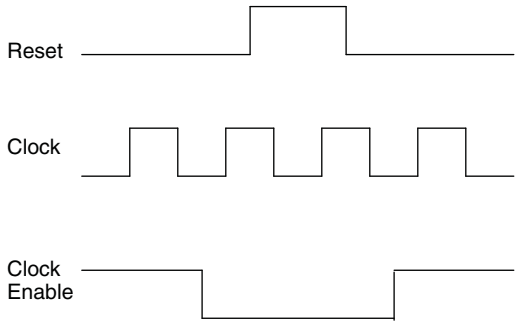


For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device

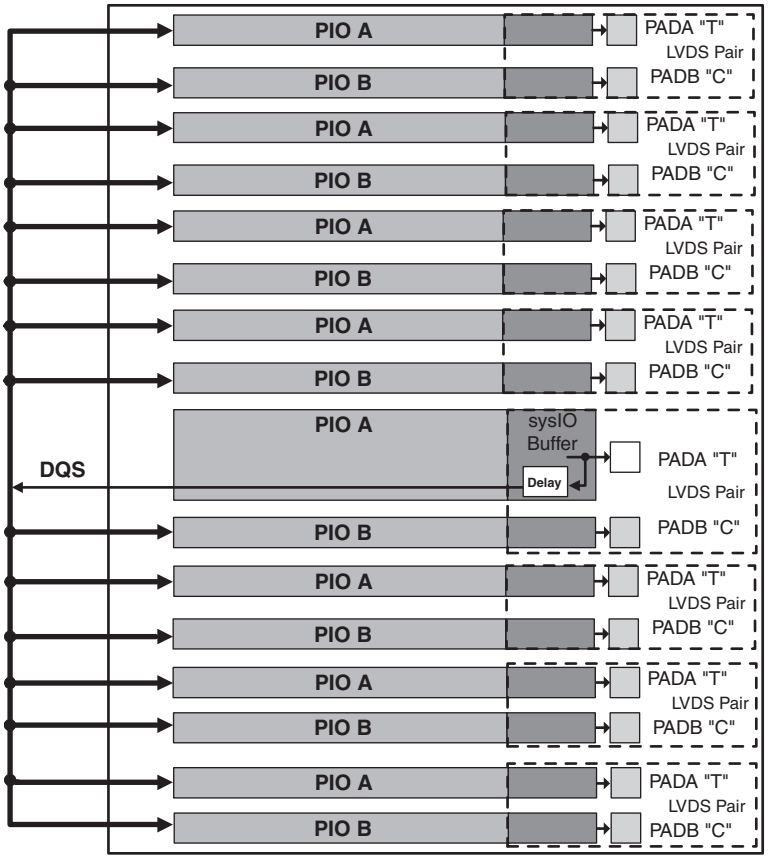
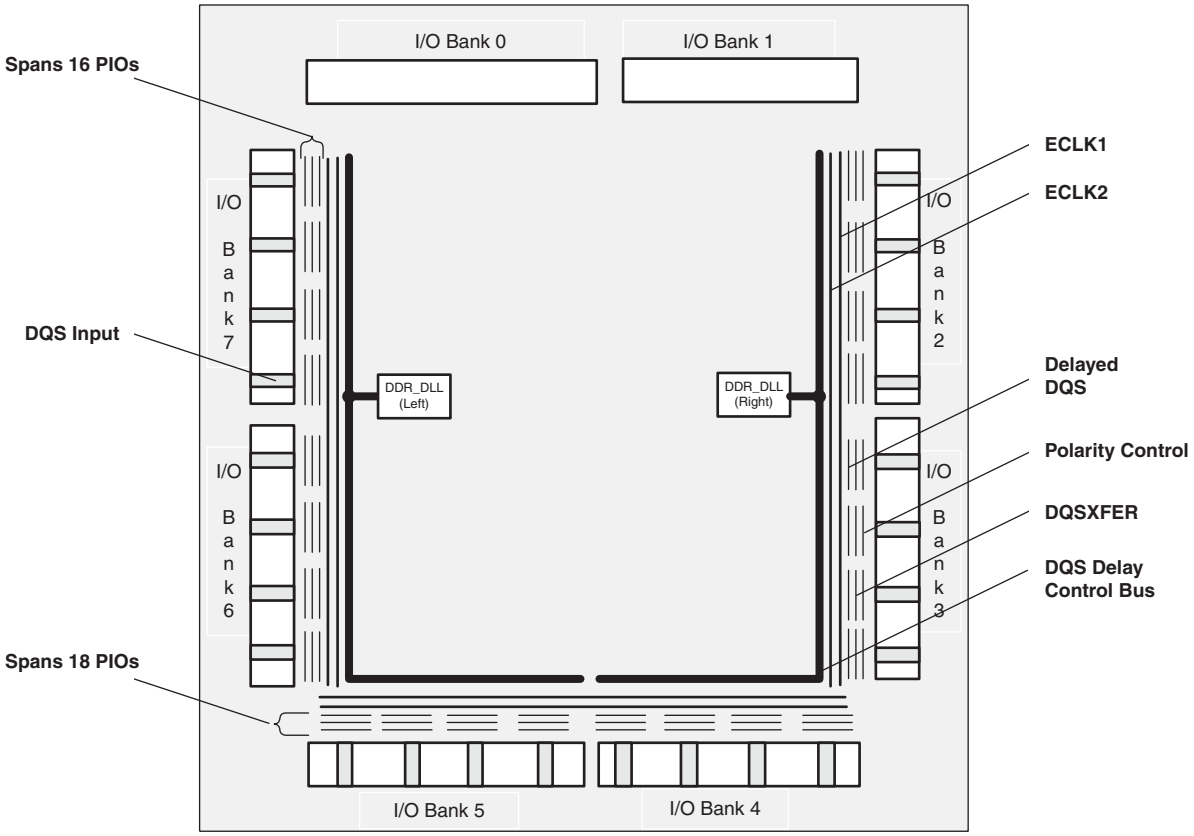


Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP2M devices feature up to 16 channels of embedded SERDES arranged in quads at the corners of the devices. Figure 2-39 shows the position of the quad blocks in relation to the PFU array for LatticeECP2M70 and LatticeECP2M100 devices. Table 2-15 shows the location of Quads for all the devices.

Each quad contains four dedicated SERDES (Ch0 to Ch3) for high-speed, full-duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains digital logic to support an array of popular data protocols. PCS also contains logic to the interface to FPGA core.

Figure 2-39. SERDES Quads (LatticeECP2M70/LatticeECP2M100)

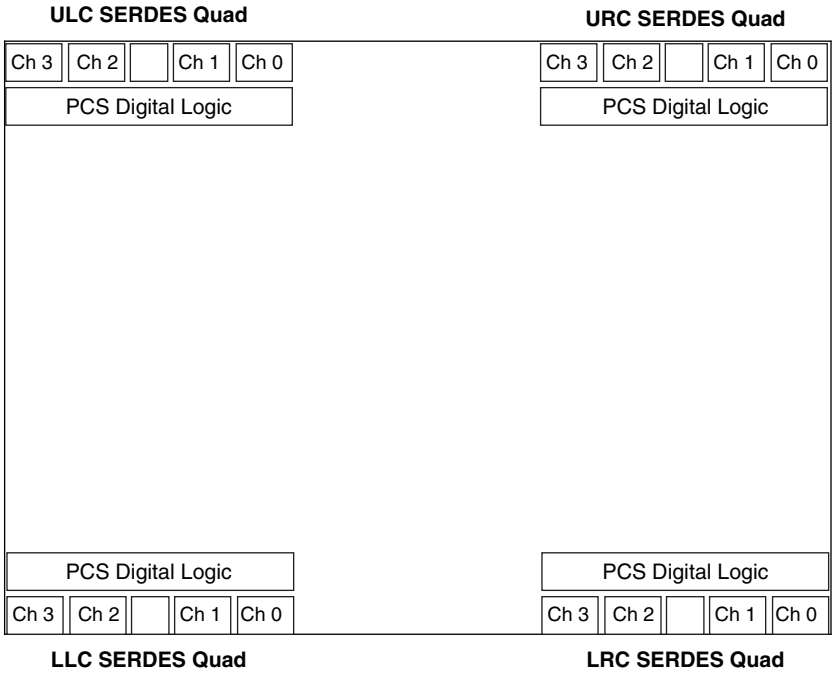


Table 2-15. Available SERDES Quads per LatticeECP2M Devices

Device	URC Quad	ULC Quad	LRC Quad	LLC Quad
ECP2M20	Available	—	—	—
ECP2M35	Available	—	—	—
ECP2M50	Available	—	Available	—
ECP2M70	Available	Available	Available	Available
ECP2M100	Available	Available	Available	Available

SERDES Block

A differential receiver receives the serial encoded data stream, equalizes the signal, extracts the buried clock and de-serializes the data-stream before passing the 8- or 10-bit data to the PCS logic. The transmit channel receives the parallel (8- or 10-bit) encoded data, serializes the data and transmits the serial bit stream through the differential buffers. There is a single transmit clock per quad. Figure 2-40 shows a single channel SERDES and its interface to the PCS logic. Each SERDES receiver channel provides a recovered clock to the PCS block and to the FPGA core logic.

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR2}	DDR Clock Frequency	ECP2/M	133	266	133	200	133	166	MHz
SPI4.2 I/O Pin Parameters Static Alignment[4, 8, 11]									
	Maximum Data Rate	ECP2-20	—	750	—	622	—	622	Mbps
		ECP2-35	—	750	—	622	—	622	Mbps
		ECP2-50	—	750	—	622	—	622	Mbps
		ECP2-70	—	750	—	622	—	622	Mbps
		ECP2M20	—	622	—	622	—	622	Mbps
		ECP2M35	—	622	—	622	—	622	Mbps
		ECP2M50	—	622	—	622	—	622	Mbps
		ECP2M70	—	622	—	622	—	622	Mbps
		ECP2M100	—	622	—	622	—	622	Mbps
$t_{DVACLKSPI}$	Data Valid After CLK (Receive)	ECP2-20	—	0.25	—	0.25	—	0.25	UI
		ECP2-35	—	0.25	—	0.25	—	0.25	UI
		ECP2-50	—	0.25	—	0.25	—	0.25	UI
		ECP2-70	—	0.25	—	0.25	—	0.25	UI
		ECP2M20	—	0.21	—	0.21	—	0.21	UI
		ECP2M35	—	0.21	—	0.21	—	0.21	UI
		ECP2M50	—	0.21	—	0.21	—	0.21	UI
		ECP2M70	—	0.21	—	0.21	—	0.21	UI
		ECP2M100	—	0.21	—	0.21	—	0.21	UI
$t_{DVECLKSPI}$	Data Hold After CLK (Receive)	ECP2-20	0.75	—	0.75	—	0.75	—	UI
		ECP2-35	0.75	—	0.75	—	0.75	—	UI
		ECP2-50	0.75	—	0.75	—	0.75	—	UI
		ECP2-70	0.75	—	0.75	—	0.75	—	UI
		ECP2M20	0.79	—	0.79	—	0.79	—	UI
		ECP2M35	0.79	—	0.79	—	0.79	—	UI
		ECP2M50	0.79	—	0.79	—	0.79	—	UI
		ECP2M70	0.79	—	0.79	—	0.79	—	UI
		ECP2M100	0.79	—	0.79	—	0.79	—	UI
t_{DIASPI}	Data Invalid After Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps

LatticeECP2/M Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	2.18	2.26	2.33	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	2.19	2.35	2.51	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.50	1.66	1.82	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.60	1.59	1.58	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.43	1.39	1.34	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	2.22	2.27	2.32	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.93	2.08	2.23	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.43	1.51	1.58	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.47	1.46	1.45	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	2.32	2.38	2.43	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	1.84	1.98	2.12	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	2.52	2.63	2.74	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	1.69	1.83	1.96	ns
PCI33	PCI33	0.04	0.04	0.04	ns

1. Timing Adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.

Timing v.A 0.11

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]_SQ_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_HDOUTNm	O	High-speed output, negative channel m
[LOC]_SQ_HDOUTPm	O	High-speed output, positive channel m
[LOC]_SQ_HDINNm	I	High-speed input, negative channel m
[LOC]_SQ_HDINPm	I	High-speed input, positive channel m
[LOC]_SQ_VCCTXm[4]	—	Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.
[LOC]_SQ_VCCRXm[4]	—	Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to TN1159, LatticeECP2/M Pin Assignment Recommendations.
5. There may be SPLLs that do not have dedicated I/Os.

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P5	P5	VCCIO5	5		
K5	K5	VCCIO6	6		
M3	M3	VCCIO6	6		
E3	E3	VCCIO7	7		
G5	G5	VCCIO7	7		
T15	T15	VCCIO8	8		
A1	A1	GND	-		
A16	A16	GND	-		
B12	B12	GND	-		
B5	B5	GND	-		
C8	C8	GND	-		
E15	E15	GND	-		
E2	E2	GND	-		
H14	H14	GND	-		
H8	H8	GND	-		
H9	H9	GND	-		
J3	J3	GND	-		
J8	J8	GND	-		
J9	J9	GND	-		
M15	M15	GND	-		
M2	M2	GND	-		
P9	P9	GND	-		
R12	R12	GND	-		
R5	R5	GND	-		
T1	T1	GND	-		
T16	T16	GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
AA19	NC	-			PB56A	4	BDQ60	T
W17	NC	-			PB56B	4	BDQ60	C
Y19	NC	-			PB57A	4	BDQ60	T
Y17	NC	-			PB57B	4	BDQ60	C
AF20	NC	-			NC	-		
VCCIO	VCCIO4	4			VCCIO4	4		
AE20	NC	-			NC	-		
AA20	NC	-			NC	-		
W18	NC	-			NC	-		
AD20	NC	-			NC	-		
GND	GNDIO4	-			GNDIO4	-		
AE21	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
VCCIO	VCCIO4	4			VCCIO4	4		
GND	GNDIO4	-			GNDIO4	-		
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	GND	-			GND	-		
A25	GND	-			GND	-		
AA18	GND	-			GND	-		
AA24	GND	-			GND	-		
AA3	GND	-			GND	-		
AA9	GND	-			GND	-		
AD11	GND	-			GND	-		
AD16	GND	-			GND	-		
AD21	GND	-			GND	-		
AD6	GND	-			GND	-		
AE1	GND	-			GND	-		
AE26	GND	-			GND	-		
AF2	GND	-			GND	-		
AF25	GND	-			GND	-		
B1	GND	-			GND	-		
B26	GND	-			GND	-		
C11	GND	-			GND	-		
C16	GND	-			GND	-		
C21	GND	-			GND	-		
C6	GND	-			GND	-		
F18	GND	-			GND	-		
F24	GND	-			GND	-		
F3	GND	-			GND	-		
F9	GND	-			GND	-		
J13	GND	-			GND	-		
J14	GND	-			GND	-		
J21	GND	-			GND	-		
J6	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K13	GND	-			GND	-		
K14	GND	-			GND	-		
K16	GND	-			GND	-		
K17	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L24	GND	-			GND	-		
L3	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB82A	4	VREF2_4/BDQ78	T	PB100A	4	VREF2_4/BDQ96	T
AB23	PB82B	4	VREF1_4/BDQ78	C	PB100B	4	VREF1_4/BDQ96	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR77B	8	WRITEN	C	PR90B	8	WRITEN	C
Y22	PR77A	8	CS1N	T	PR90A	8	CS1N	T
AC25	PR76B	8	CSN	C	PR89B	8	CSN	C
AB25	PR76A	8	D0/SPIFASTN	T	PR89A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR75B	8	D1	C	PR88B	8	D1	C
AC26	PR75A	8	D2	T	PR88A	8	D2	T
Y23	PR74B	8	D3	C	PR87B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR74A	8	D4	T	PR87A	8	D4	T
AA25	PR73B	8	D5	C	PR86B	8	D5	C
AB26	PR73A	8	D6	T	PR86A	8	D6	T
W23	PR72B	8	D7/SPID0	C	PR85B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR72A	8	DI/CSSPI0N	T	PR85A	8	DI/CSSPI0N	T
Y24	PR71B	8	DOUT/CSON	C	PR84B	8	DOUT/CSON	C
Y25	PR71A	8	BUSY/SISPI	T	PR84A	8	BUSY/SISPI	T
W24	PR70B	3	RDQ67	C	PR83B	3	RDQ80	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR70A	3	RDQ67	T	PR83A	3	RDQ80	T
AA26	PR69B	3	RDQ67	C (LVDS)*	PR82B	3	RDQ80	C (LVDS)*
Y26	PR69A	3	RDQ67	T (LVDS)*	PR82A	3	RDQ80	T (LVDS)*
U21	PR68B	3	RDQ67	C	PR81B	3	RDQ80	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR68A	3	RDQ67	T	PR81A	3	RDQ80	T
W25	PR67B	3	RDQ67	C (LVDS)*	PR80B	3	RDQ80	C (LVDS)*
W26	PR67A	3	RDQS67	T (LVDS)*	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR66B	3	RDQ67	C	PR79B	3	RDQ80	C
V25	PR66A	3	RDQ67	T	PR79A	3	RDQ80	T
V26	PR65B	3	RDQ67	C (LVDS)*	PR78B	3	RDQ80	C (LVDS)*
U26	PR65A	3	RDQ67	T (LVDS)*	PR78A	3	RDQ80	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR64B	3	RLM0_GPLLC_FB_A/RDQ67	C	PR77B	3	RLM0_GPLLC_FB_A/RDQ80	C
U23	PR64A	3	RLM0_GPLLT_FB_A/RDQ67	T	PR77A	3	RLM0_GPLLT_FB_A/RDQ80	T

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N11	CCLK	8			CCLK	8		
M11	INITN	8			INITN	8		
N13	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
M12	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
M13	PR53A	8	CS1N	T	PR68A	8	CS1N	T
N14	PR52B	8	CSN	C	PR67B	8	CSN	C
N15	PR52A	8	D0/SPIFASTN	T	PR67A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
N16	PR51B	8	D1	C	PR66B	8	D1	C
M16	PR51A	8	D2	T	PR66A	8	D2	T
L12	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
L13	PR50A	8	D4	T	PR65A	8	D4	T
L16	PR49B	8	D5	C	PR64B	8	D5	C
K16	PR49A	8	D6	T	PR64A	8	D6	T
L14	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C
VCCIO	VCCIO8	8			VCCIO8	8		
L15	PR48A	8	DI/CSSPI0N	T	PR63A	8	DI/CSSPI0N	T
K13	PR47B	8	DOUT/CSON/CSSPI1N	C	PR62B	8	DOUT/CSON/CSSPI1N	C
K14	PR47A	8	BUSY/SISPI	T	PR62A	8	BUSY/SISPI	T
K11	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
K15	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C
GNDIO	GNDIO3	-			GNDIO3	-		
J16	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T
H16	PR44B	3	RLM0_GDLLC_IN_A	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C(LVDS)*
J15	PR44A	3	RLM0_GDLLT_IN_A	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*
J14	PR43B	3	RLM0_GPLLC_IN_A	C	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C
VCCIO	VCCIO3	3			VCCIO3	3		
J13	PR43A	3	RLM0_GPLLT_IN_A	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T
H13	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C(LVDS)*
H12	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57***	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
G16	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
H15	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
E16	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C(LVDS)*
F15	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
F16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
G15	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J11	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C(LVDS)*
J12	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
G14	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
G13	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
D1	PL2A	7	LDQ6	T (LVDS)*
E1	PL2B	7	LDQ6	C (LVDS)*
F1	PL3A	7	LDQ6	T
F2	PL3B	7	LDQ6	C
F5	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7		
G6	PL4B	7	LDQ6	C (LVDS)*
F4	PL5A	7	LDQ6	T
F3	PL5B	7	LDQ6	C
G1	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-		
G2	PL6B	7	LDQ6	C (LVDS)*
H1	PL7A	7	LDQ6	T
H2	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7		
H7	PL8A	7	LDQ6	T (LVDS)*
H6	PL8B	7	LDQ6	C (LVDS)*
G3	PL9A	7	VREF2_7/LDQ6	T
H3	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C
GNDIO	GNDIO7	-		
J3	PL13A	7		T (LVDS)*
J4	PL13B	7		C (LVDS)*
J7	PL14A	7		T
VCCIO	VCCIO7	7		
J6	PL14B	7		C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
K1	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*
K2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*
J5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T
K5	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C
VCCIO	VCCIO7	7		
K7	PL34A	7	LDQ36	T (LVDS)*
K6	PL34B	7	LDQ36	C (LVDS)*
L6	PL35A	7	LDQ36	T
L7	PL35B	7	LDQ36	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J11	VCC	-		
J12	VCC	-		
J13	VCC	-		
K14	VCC	-		
K9	VCC	-		
L14	VCC	-		
L9	VCC	-		
M14	VCC	-		
M9	VCC	-		
N14	VCC	-		
N9	VCC	-		
P10	VCC	-		
P11	VCC	-		
P12	VCC	-		
P13	VCC	-		
B5	VCCIO0	0		
B9	VCCIO0	0		
E7	VCCIO0	0		
H9	VCCIO0	0		
D13	VCCIO1	1		
E16	VCCIO1	1		
H14	VCCIO1	1		
E21	VCCIO2	2		
G18	VCCIO2	2		
J15	VCCIO2	2		
K19	VCCIO2	2		
N19	VCCIO3	3		
P15	VCCIO3	3		
T18	VCCIO3	3		
V21	VCCIO3	3		
AA18	VCCIO4	4		
R14	VCCIO4	4		
V16	VCCIO4	4		
W13	VCCIO4	4		
AA5	VCCIO5	5		
R9	VCCIO5	5		
V7	VCCIO5	5		
W10	VCCIO5	5		
N4	VCCIO6	6		
P8	VCCIO6	6		
T5	VCCIO6	6		
V2	VCCIO6	6		
E2	VCCIO7	7		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C15	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B15	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C14	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A18	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C18	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B18	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C17	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B17	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A16	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A17	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C16	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B14	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B13	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A14	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C13	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
-	-	-			GNDIO1	-		
-	-	-			VCCIO1	1		
E17	PT46B	1		C	PT55B	1		C
D17	PT46A	1		T	PT55A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
F17	PT45B	1		C	PT54B	1		C
D16	PT45A	1		T	PT54A	1		T
F19	PT44B	1		C	PT53B	1		C
F18	PT44A	1		T	PT53A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
E16	PT43B	1		C	PT52B	1		C
D15	PT43A	1		T	PT52A	1		T
G18	PT42B	1		C	PT51B	1		C
E15	PT42A	1		T	PT51A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
G17	PT41B	1		C	PT50B	1		C
E14	PT41A	1		T	PT50A	1		T
D14	PT40B	1		C	PT49B	1		C
D13	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
F15	PT39B	1	VREF2_1	C	PT48B	1	VREF2_1	C
E12	PT39A	1	VREF1_1	T	PT48A	1	VREF1_1	T
H17	PT38B	1	PCLKC1_0	C	PT47B	1	PCLKC1_0	C
E13	PT38A	1	PCLKT1_0	T	PT47A	1	PCLKT1_0	T
C12	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G15	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T
C11	PT36B	0	VREF2_0	C	PT45B	0	VREF2_0	C
F14	PT36A	0	VREF1_0	T	PT45A	0	VREF1_0	T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AJ17	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AF26	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T
AE25	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
AD24	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T
AE24	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C
AD18	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AC18	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
AE18	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
AG19	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AC19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
AD20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
AB18	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
AC20	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
AE20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
AE21	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
AC23	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
AD23	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
AH18	LRC_SQ_VCCRX3	13			LRC_SQ_VCCRX3	13		
AK19	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T
AK21	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C
AH22	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C
AH23	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T
AH19	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AJ20	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AK25	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AH25	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AH26	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AK27	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AH27	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AJ30	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AK29	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AH30	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AG27	CFG2	8			CFG2	8		
AD25	CFG1	8			CFG1	8		
AG28	CFG0	8			CFG0	8		
AG30	PROGRAMN	8			PROGRAMN	8		
AG29	CCLK	8			CCLK	8		
AC24	INITN	8			INITN	8		
AF27	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF28	WRITEN***	8			WRITEN***	8		
AE26	CS1N***	8			CS1N***	8		
AB23	CSN***	8			CSN***	8		
AF29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AF30	D1***	8			D1***	8		
AD26	D2***	8			D2***	8		
AE29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE30	D4***	8			D4***	8		
AD29	D5***	8			D5***	8		
AC25	D6***	8			D6***	8		
AD30	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AA22	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AC26	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8		
AA23	BUSY/SISPI***	8			BUSY/SISPI***	8		
AB22	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
AC27	PR65B	3	RLM0_GDLLC_FB_A	C	PR85B	3	RLM0_GDLLC_FB_A/RDQ82	C
GNDIO	GNDIO3	-			GNDIO3	-		
AC28	PR65A	3	RLM0_GDLLT_FB_A	T	PR85A	3	RLM0_GDLLT_FB_A/RDQ82	T
AC29	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR84B	3	RLM0_GDLLC_IN_A**/RDQ82	C (LVDS)*
AC30	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR84A	3	RLM0_GDLLT_IN_A**/RDQ82	T (LVDS)*
AB30	PR63B	3	RLM0_GPLLC_IN_A**	C	PR83B	3	RLM0_GPLLC_IN_A**/RDQ82	C
VCCIO	VCCIO3	3			VCCIO3	3		
AA30	PR63A	3	RLM0_GPLLT_IN_A**	T	PR83A	3	RLM0_GPLLT_IN_A**/RDQ82	T
AB29	PR62B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR82B	3	RLM0_GPLLC_FB_A/RDQ82	C (LVDS)*
AB28	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR82A	3	RLM0_GPLLT_FB_A/RDQS82	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M26	PR27A	2	RDQS27	T (LVDS)*	PR37A	2	RDQS37	T (LVDS)*
L30	PR26B	2	RDQ27	C	PR36B	2	RDQ37	C
GNDIO	GNDIO2	-			GNDIO2	-		
L29	PR26A	2	RDQ27	T	PR36A	2	RDQ37	T
L28	PR25B	2	RDQ27	C (LVDS)*	PR35B	2	RDQ37	C (LVDS)*
L27	PR25A	2	RDQ27	T (LVDS)*	PR35A	2	RDQ37	T (LVDS)*
H29	PR24B	2	RDQ27	C	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2			VCCIO2	2		
G29	PR24A	2	RDQ27	T	PR34A	2	RDQ37	T
L22	PR23B	2	RDQ27	C (LVDS)*	PR33B	2	RDQ37	C (LVDS)*
M22	PR23A	2	RDQ27	T (LVDS)*	PR33A	2	RDQ37	T (LVDS)*
F30	PR21B	2		C	PR31B	2	RDQ28	C
GNDIO	GNDIO2	-			GNDIO2	-		
F29	PR21A	2		T	PR31A	2	RDQ28	T
-	-	-			-	-		
-	-	-			-	-		
E30	PR20B	2		C (LVDS)*	PR30B	2	RDQ28	C (LVDS)*
E29	PR20A	2		T (LVDS)*	PR30A	2	RDQ28	T (LVDS)*
VCCIO	VCCIO2	2			-	-		
L25	PR19B	2		C	PR29B	2	RDQ28	C
L26	PR19A	2		T	PR29A	2	RDQ28	T
-	-	-			VCCIO2	2		
H28	PR18B	2		C (LVDS)*	PR28B	2	RDQ28	C (LVDS)*
J28	PR18A	2		T (LVDS)*	PR28A	2	RDQS28	T (LVDS)*
G28	PR16B	2		C	PR27B	2	RDQ28	C
GNDIO	GNDIO2	-			GNDIO2	-		
G27	PR16A	2		T	PR27A	2	RDQ28	T
L24	NC	-			PR26B	2	RDQ28	C (LVDS)*
L23	NC	-			PR26A	2	RDQ28	T (LVDS)*
D30	NC	-			PR25B	2	RDQ28	C
-	-	-			VCCIO2	2		
D29	NC	-			PR25A	2	RDQ28	T
K24	NC	-			PR24B	2	RDQ28	C (LVDS)*
K25	NC	-			PR24A	2	RDQ28	T (LVDS)*
J27	NC	-			PR22B	2		C
-	-	-			GNDIO2	-		
K26	NC	-			PR22A	2		T
K23	PR15B	2		C (LVDS)*	PR21B	2		C (LVDS)*
K22	PR15A	2		T (LVDS)*	PR21A	2		T (LVDS)*
J22	PR14B	2		C	PR20B	2		C
VCCIO	VCCIO2	-			VCCIO2	2		
J23	PR14A	2		T	PR20A	2		T
-	-	-			GNDIO2	-		
-	-	-			-	-		
J26	NC	-			PR17B	2	RDQ15	C (LVDS)*
H26	NC	-			PR17A	2	RDQ15	T (LVDS)*
H27	NC	-			PR16B	2	RDQ15	C
G26	NC	-			PR16A	2	RDQ15	T

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2M20SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	35
LFE2M35SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50SE-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152I	436	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-6FN1152I	436	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table.
		Ordering Information	Updated ordering part number table to include ECP2-12.
			Updated topside mark drawing.
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions.
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
			Updated timing numbers to include LFE2-12E (rev A 0.08).
		Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.
		Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added “Security Series” to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	“Security Series” ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.
August 2007	02.8	Introduction	1156-fpBGA package option has been removed from the LatticeECP2M family.
		Architecture	Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated.
		DC and Switching	Supply Current (Standby) table has been updated.
			DSP Function timing has been updated.