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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

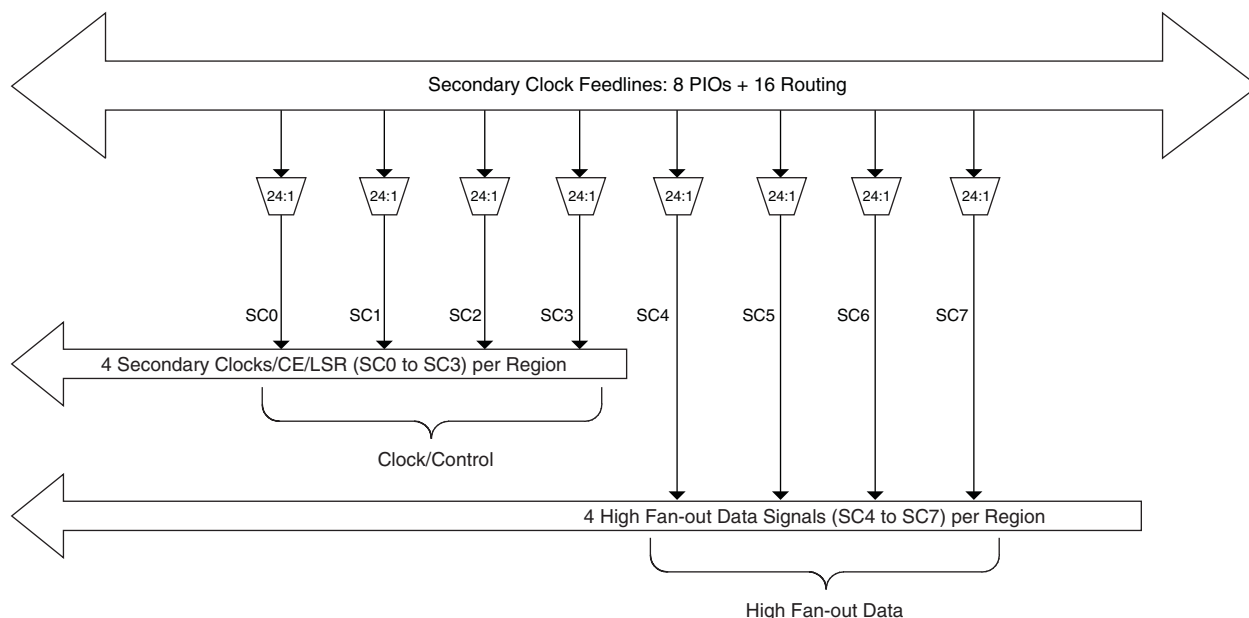
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5q208i

Figure 2-16. Secondary Clock Selection

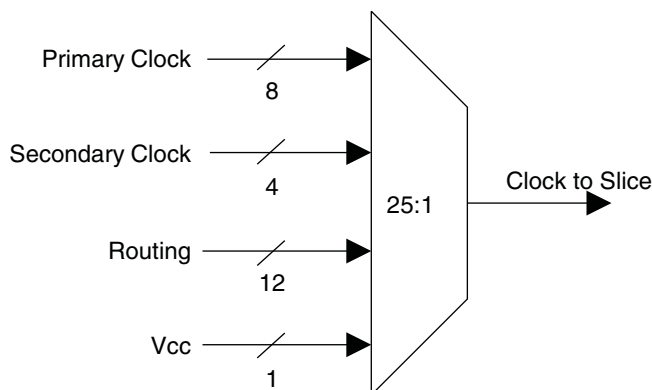


Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection



IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IOE}	Clock Frequency of I/O and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)¹									
t _{COPLL} ¹⁰	Clock to Output - PIO Output Register	LFE2-6	—	2.30	—	2.60	—	2.80	ns
		LFE2-12	—	2.30	—	2.60	—	2.80	ns
		LFE2-20	—	2.30	—	2.60	—	2.80	ns
		LFE2-35	—	2.30	—	2.60	—	2.80	ns
		LFE2-50	—	2.30	—	2.60	—	2.80	ns
		LFE2-70	—	2.30	—	2.60	—	2.80	ns
		LFE2M20	—	2.30	—	2.60	—	2.80	ns
		LFE2M35	—	2.30	—	2.60	—	2.80	ns
		LFE2M50	—	2.60	—	2.90	—	3.10	ns
		LFE2M70	—	2.60	—	2.90	—	3.10	ns
		LFE2M100	—	2.70	—	3.00	—	3.20	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	LFE2-6	0.70	—	0.80	—	0.90	—	ns
		LFE2-12	0.70	—	0.80	—	0.90	—	ns
		LFE2-20	0.70	—	0.80	—	0.90	—	ns
		LFE2-35	0.70	—	0.80	—	0.90	—	ns
		LFE2-50	0.70	—	0.80	—	0.90	—	ns
		LFE2-70	0.70	—	0.80	—	0.90	—	ns
		LFE2M20	0.70	—	0.80	—	0.90	—	ns
		LFE2M35	0.70	—	0.80	—	0.90	—	ns
		LFE2M50	0.70	—	0.80	—	0.90	—	ns
		LFE2M70	0.70	—	0.80	—	0.90	—	ns
		LFE2M100	0.80	—	0.90	—	1.00	—	ns

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, slow slew rate	2.18	2.26	2.33	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, slow slew rate	2.19	2.35	2.51	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, slow slew rate	1.50	1.66	1.82	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, slow slew rate	1.60	1.59	1.58	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, slow slew rate	1.43	1.39	1.34	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, slow slew rate	2.22	2.27	2.32	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, slow slew rate	1.93	2.08	2.23	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, slow slew rate	1.43	1.51	1.58	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, slow slew rate	1.47	1.46	1.45	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, slow slew rate	2.32	2.38	2.43	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, slow slew rate	1.84	1.98	2.12	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, slow slew rate	2.52	2.63	2.74	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, slow slew rate	1.69	1.83	1.96	ns
PCI33	PCI33	0.04	0.04	0.04	ns

1. Timing Adders are characterized but not tested on every device.
 2. LVC MOS timing measured with the load specified in Switching Test Condition table.
 3. All other standards tested according to the appropriate specifications.
 4. These timing adders are measured with the recommended resistor values.
- Timing v.A 0.11

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
138	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	
139	GND	-			GND	-			
140	VCC	-			VCC	-			
141	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C	
142	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T	
143	VCCIO2	2			VCCIO2	2			
144	PR12A	2	RDQ10		PR16A	2	RDQS16		
145	GND	-			GND	-			
146	VCC	-			VCC	-			
147	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*	
148	VCCIO2	2			VCCIO2	2			
149	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*	
150	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*	
151	VCCAUX	-			VCCAUX	-			
152	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*	
153	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*	
154	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
155	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
156	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
157	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
158	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
159	GND	-			GND	-			
160	PT54B	1		C	PT62B	1		C	
161	PT54A	1		T	PT62A	1		T	
162	VCCIO1	1			VCCIO1	1			
163	PT52B	1		C	PT60B	1		C	
164	PT52A	1		T	PT60A	1		T	
165	PT50B	1		C	PT58B	1		C	
166	PT50A	1		T	PT58A	1		T	
167	PT48B	1		C	PT56B	1		C	
168	PT48A	1		T	PT56A	1		T	
169	GND	-			GND	-			
170	VCCIO1	1			VCCIO1	1			
171	VCC	-			VCC	-			
172	PT40B	1		C	PT50B	1		C	
173	PT40A	1		T	PT50A	1		T	
174	VCCAUX	-			VCCAUX	-			
175	GND	-			GND	-			
176	PT36B	1		C	PT44B	1		C	
177	PT36A	1		T	PT44A	1		T	
178	PT34B	1		C	PT42B	1		C	
179	PT34A	1		T	PT42A	1		T	
180	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C	
181	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T	
182	XRES	1			XRES	1			
183	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C	

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO	VCCIO1	1		
D12	D12	PT62A	1		T
B14	B14	PT61B	1		C
C14	C14	PT60B	1		C
A14	A14	PT61A	1		T
D13	D13	PT60A	1		T
C13	C13	PT59B	1		C
GND	GND	GNDIO1	-		
A13	A13	PT58B	1		C
B13	B13	PT59A	1		T
VCCIO	VCCIO	VCCIO1	1		
A12	A12	PT58A	1		T
B11	B11	PT57B	1		C
D11	D11	PT56B	1		C
A11	A11	PT57A	1		T
C11	C11	PT56A	1		T
-	GND	GNDIO1	1		
-	VCC	VCCIO	1		
D10	D10	PT46B	1		C
C10	C10	PT46A	1		T
GND	GND	GNDIO1	-		
B10	B10	PT45B	1		C
A9	A9	PT44B	1		C
A10	A10	PT45A	1		T
B9	B9	PT44A	1		T
VCCIO	VCCIO	VCCIO1	1		
A8	A8	PT43B	1		C
D9	D9	PT42B	1		C
B8	B8	PT43A	1		T
C9	C9	PT42A	1		T
GND	GND	GNDIO1	-		
B7	B7	PT41B	1		C
E9	E9	PT40B	1		C
A7	A7	PT41A	1		T
D8	D8	PT40A	1		T
VCCIO	VCCIO	VCCIO1	1		
A6	A6	PT39B	1	PCLKC1_0	C
B6	B6	PT39A	1	PCLKT1_0	T
E6	E6	XRES	1		
F8	F8	PT37B	0	PCLKC0_0	C
GND	GND	GNDIO0	-		
E8	E8	PT37A	0	PCLKT0_0	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO1	-			GNDIO1	-		
C15	PT54B	1		C	PT63B	1		C
A15	PT54A	1		T	PT63A	1		T
A13	PT53B	1		C	PT62B	1		C
B13	PT53A	1		T	PT62A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
H17	PT52B	1		C	PT61B	1		C
H15	PT52A	1		T	PT61A	1		T
D13	PT51B	1		C	PT60B	1		C
C14	PT51A	1		T	PT60A	1		T
GND	GNDIO1	-			GNDIO1	-		
G14	PT50B	1		C	PT59B	1		C
E14	PT50A	1		T	PT59A	1		T
A12	PT49B	1		C	PT58B	1		C
B12	PT49A	1		T	PT58A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
F14	PT48B	1	PCLKC1_0	C	PT57B	1	PCLKC1_0	C
D14	PT48A	1	PCLKT1_0	T	PT57A	1	PCLKT1_0	T
H16	XRES	1			XRES	1		
H14	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C
GND	GNDIO0	-			GNDIO0	-		
H13	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T
A11	PT45B	0		C	PT54B	0		C
B11	PT45A	0		T	PT54A	0		T
C13	PT44B	0		C	PT53B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
E13	PT44A	0		T	PT53A	0		T
D12	PT43B	0		C	PT52B	0		C
F13	PT43A	0		T	PT52A	0		T
A10	PT42B	0		C	PT51B	0		C
B10	PT42A	0		T	PT51A	0		T
C12	PT41B	0		C	PT50B	0		C
GND	GNDIO0	-			GNDIO0	-		
C10	PT41A	0		T	PT50A	0		T
G13	PT40B	0		C	PT49B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
H12	PT40A	0		T	PT49A	0		T
A9	PT39B	0		C	PT48B	0		C
B9	PT39A	0		T	PT48A	0		T
E12	PT38B	0		C	PT47B	0		C
G12	PT38A	0		T	PT47A	0		T
A8	PT37B	0		C	PT46B	0		C
B8	PT37A	0		T	PT46A	0		T
GND	GNDIO0	-			GNDIO0	-		
E11	PT36B	0		C	PT45B	0		C
C9	PT36A	0		T	PT45A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D1	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*	
E1	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C (LVDS)*	
F1	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T	
F2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C	
F5	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
G6	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C (LVDS)*	
F4	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T	
F3	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C	
G1	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO7	-			
G2	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C (LVDS)*	
H1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T	
H2	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C	
VCCIO	VCCIO7	7			VCCIO7	7			
H7	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*	
H6	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C (LVDS)*	
G3	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T	
H3	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C	
GNDIO	GNDIO7	-			GNDIO7	-			
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	
J1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	
J2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	
J3	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
J4	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*	
J7	PL14A	7		T	PL14A	7	LDQ15	T	
J6	PL14B	7		C	PL14B	7	LDQ15	C	
GNDIO	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K1	PL18A	7	LUM1_SPLLT_IN_A/LDQ22	T (LVDS)*	PL28A	7	LUM1_SPLLT_IN_A/LDQ32	T (LVDS)*	
K2	PL18B	7	LUM1_SPLLC_IN_A/LDQ22	C (LVDS)*	PL28B	7	LUM1_SPLLC_IN_A/LDQ32	C (LVDS)*	
J5	PL19A	7	LUM1_SPLLT_FB_A/LDQ22	T	PL29A	7	LUM1_SPLLT_FB_A/LDQ32	T	
K5	PL19B	7	LUM1_SPLLC_FB_A/LDQ22	C	PL29B	7	LUM1_SPLLC_FB_A/LDQ32	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K7	PL20A	7	LDQ22	T (LVDS)*	PL30A	7	LDQ32	T (LVDS)*	
K6	PL20B	7	LDQ22	C (LVDS)*	PL30B	7	LDQ32	C (LVDS)*	
L6	PL21A	7	LDQ22	T	PL31A	7	LDQ32	T	
L7	PL21B	7	LDQ22	C	PL31B	7	LDQ32	C	
GNDIO	GNDIO7	-			GNDIO7	-			
L1	PL22A	7	LDQS22	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*	
L2	PL22B	7	LDQ22	C (LVDS)*	PL32B	7	LDQ32	C (LVDS)*	
M7	PL23A	7	LDQ22	T	PL33A	7	LDQ32	T	
VCCIO	VCCIO7	7			VCCIO7	7			
L5	PL23B	7	LDQ22	C	PL33B	7	LDQ32	C	
L3	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
V5	PL51A	6	LDQS51	T (LVDS)*	PL66A	6	LDQS66	T (LVDS)*	
U4	PL51B	6	LDQ51	C (LVDS)*	PL66B	6	LDQ66	C (LVDS)*	
V1	PL52A	6	LDQ51	T	PL67A	6	LDQ66	T	
VCCIO	VCCIO6	6			VCCIO6	6			
V3	PL52B	6	LDQ51	C	PL67B	6	LDQ66	C	
W1	PL53A	6	LDQ51	T (LVDS)*	PL68A	6	LDQ66	T (LVDS)*	
Y1	PL53B	6	LDQ51	C (LVDS)*	PL68B	6	LDQ66	C (LVDS)*	
AA1	PL54A	6	LDQ51	T	PL69A	6	LDQ66	T	
GNDIO	GNDIO6	-			GNDIO6	-			
AA2	PL54B	6	LDQ51	C	PL69B	6	LDQ66	C	
V4	TCK	-			TCK	-			
Y2	TDI	-			TDI	-			
Y3	TMS	-			TMS	-			
W3	TDO	-			TDO	-			
W4	VCCJ	-			VCCJ	-			
W5	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T	
Y4	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C	
W6	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
V6	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AA3	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AB2	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
T8	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
U7	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
U8	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
T9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
V8	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
W8	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
Y6	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
AB3	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AB4	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AB5	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AA6	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
V9	PB13A	5	BDQ15	T	PB31A	5	BDQ33	T	
U9	PB13B	5	BDQ15	C	PB31B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
-	-	-			GNDIO5	-			
U10	PB14A	5	BDQ15	T	PB32A	5	BDQ33	T	
T10	PB14B	5	BDQ15	C	PB32B	5	BDQ33	C	
GNDIO	GNDIO5	-			GNDIO5	-			
W9	PB15A	5	BDQS15****	T	PB33A	5	BDQS33****	T	
Y8	PB15B	5	BDQ15	C	PB33B	5	BDQ33	C	
AA7	PB16A	5	VREF2_5/BDQ15	T	PB34A	5	VREF2_5/BDQ33	T	
Y7	PB16B	5	VREF1_5/BDQ15	C	PB34B	5	VREF1_5/BDQ33	C	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
P8	PL45A	6	LDQ48	T	PL49A	6	LDQ52	T	
R6	PL45B	6	LDQ48	C	PL49B	6	LDQ52	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T1	PL46A	6	LDQ48	T (LVDS)*	PL50A	6	LDQ52	T*	
U1	PL46B	6	LDQ48	C (LVDS)*	PL50B	6	LDQ52	C*	
R7	PL47A	6	LDQ48	T	PL51A	6	LDQ52	T	
T5	PL47B	6	LDQ48	C	PL51B	6	LDQ52	C	
GNDIO	GNDIO6	-			GNDIO6	-			
U3	PL48A	6	LDQS48	T (LVDS)*	PL52A	6	LDQS52	T*	
U4	PL48B	6	LDQ48	C (LVDS)*	PL52B	6	LDQ52	C*	
U5	PL49A	6	LDQ48	T	PL53A	6	LDQ52	T	
VCCIO	VCCIO6	6			VCCIO6	6			
U6	PL49B	6	LDQ48	C	PL53B	6	LDQ52	C	
U2	PL50A	6	LDQ48	T (LVDS)*	PL54A	6	LDQ52	T*	
V1	PL50B	6	LDQ48	C (LVDS)*	PL54B	6	LDQ52	C*	
W2	PL51A	6	LDQ48	T	PL55A	6	LDQ52	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V2	PL51B	6	LDQ48	C	PL55B	6	LDQ52	C	
V4	PL55A	6	LDQ57	T (LVDS)*	PL59A	6		T*	
VCCIO	VCCIO6	6			VCCIO6	6			
V3	PL55B	6	LDQ57	C (LVDS)*	PL59B	6		C*	
-	-	-			GNDIO6	-			
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	PL62A	6	LLM0_GPLLT_IN_A	T*	
GNDIO	GNDIO6	-			GNDIO6	-			
W3	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	PL62B	6	LLM0_GPLLC_IN_A	C*	
W1	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	PL63A	6	LLM0_GPLLT_FB_A	T	
Y1	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	PL63B	6	LLM0_GPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AA1	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*	PL64A	6	LLM0_GDLLT_IN_A	T*	
AB1	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	PL64B	6	LLM0_GDLLC_IN_A	C*	
U7	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T	PL65A	6	LLM0_GDLLT_FB_A	T	
V6	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	PL65B	6	LLM0_GDLLC_FB_A	C	
GNDIO	GNDIO6	-			GNDIO6	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
W5	PL62A	6	LDQ66	T (LVDS)*	PL67A	6	LDQ71	T*	
Y4	PL62B	6	LDQ66	C (LVDS)*	PL67B	6	LDQ71	C*	
U8	PL63A	6	LDQ66	T	PL68A	6	LDQ71	T	
W6	PL63B	6	LDQ66	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y3	PL64A	6	LDQ66	T (LVDS)*	PL69A	6	LDQ71	T*	
AA3	PL64B	6	LDQ66	C (LVDS)*	PL69B	6	LDQ71	C*	
V7	NC	-			PL70A	6	LDQ71	T	
Y5	PL65B	6	LDQ66	C	PL70B	6	LDQ71	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB2	PL66A	6	LDQS66	T (LVDS)*	PL71A	6	LDQS71	T*	
AA4	PL66B	6	LDQ66	C (LVDS)*	PL71B	6	LDQ71	C*	
Y6	PL67A	6	LDQ66	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF23	PB64A	4	BDQ60	T	LRC_SQ_HDINP1	13		T	
AD23	NC	-			LRC_SQ_VCCIB1	13			
AE23	PB66B	4	BDQ69	C	LRC_SQ_HDINN1	13		C	
AD24	VCC	-			LRC_SQ_VCCRX1	13			
AF20	PB55A	4	BDQ51	T	LRC_SQ_HDOUTP1	13		T	
AD20	NC	-			LRC_SQ_VCCOB1	13			
AE20	PB55B	4	BDQ51	C	LRC_SQ_HDOUTN1	13		C	
AD21	VCC	-			LRC_SQ_VCCTX1	13			
AE21	PB63B	4	BDQ60	C	LRC_SQ_HDOUTN0	13		C	
AF22	NC	-			LRC_SQ_VCCOB0	13			
AF21	PB62A	4	BDQ60	T	LRC_SQ_HDOUTP0	13		T	
AD22	VCC	-			LRC_SQ_VCCTX0	13			
AE24	PB67B	4	BDQ69	C	LRC_SQ_HDINN0	13		C	
AE25	NC	-			LRC_SQ_VCCIB0	13			
AF24	PB67A	4	BDQ69	T	LRC_SQ_HDINP0	13		T	
AD25	VCC	-			LRC_SQ_VCCRX0	13			
AA21	CFG2	8			CFG2	8			
AA22	CFG1	8			CFG1	8			
AB23	CFG0	8			CFG0	8			
AC26	PROGRAMN	8			PROGRAMN	8			
AB24	CCLK	8			CCLK	8			
AA23	INITN	8			INITN	8			
AB25	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
Y19	PR68B	8	WRITEN***	C	WRITEN***	8			
Y21	PR68A	8	CS1N***	T	CS1N***	8			
AB26	PR67B	8	CSN***	C	CSN***	8			
Y22	PR67A	8	D0/SPIFASTN***	T	D0/SPIFASTN***	8			
VCCIO	VCCIO8	8				8			
W19	PR66B	8	D1***	C	D1***	8			
Y20	PR66A	8	D2***	T	D2***	8			
W22	PR65B	8	D3***	C	D3***	8			
GNDIO	GNDIO8	-				-			
W18	PR65A	8	D4***	T	D4***	8			
Y23	PR64B	8	D5***	C	D5***	8			
AA24	PR64A	8	D6***	T	D6***	8			
W21	PR63B	8	D7/SPID0***	C	D7/SPID0***	8			
VCCIO	VCCIO8	8			VCCIO8	8			
V20	PR63A	8	DI/CSSPI0N***	T	DI/CSSPI0N***	8			
W23	PR62B	8	DOUT/CSON/CSSPI1N***	C	DOUT/CSON/ CSSPI1N***	8			
Y24	PR62A	8	BUSY/SISPI***	T	BUSY/SISPI***	8			
V19	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
V21	PR60B	3	RLM0_GDLLC_FB_A	C	PR65B	3	RLM0_GDLLC_FB_A	C	
GNDIO	GNDIO3	-			GNDIO3	-			
U19	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T	PR65A	3	RLM0_GDLLT_FB_A	T	
AA26	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*	PR64B	3	RLM0_GDLLC_IN_A	C*	
Y26	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*	PR64A	3	RLM0_GDLLT_IN_A	T*	
V23	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C	PR63B	3	RLM0_GPLLC_IN_A	C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K3	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
N10	VCCIO7	7			VCCIO7	7			
N3	VCCIO7	7			VCCIO7	7			
P10	VCCIO7	7			VCCIO7	7			
R6	VCCIO7	7			VCCIO7	7			
AA25	VCCIO8	8			VCCIO8	8			
AD28	VCCIO8	8			VCCIO8	8			
AA10	VCCAUX	-			VCCAUX	-			
AA11	VCCAUX	-			VCCAUX	-			
AA20	VCCAUX	-			VCCAUX	-			
AA21	VCCAUX	-			VCCAUX	-			
K10	VCCAUX	-			VCCAUX	-			
K11	VCCAUX	-			VCCAUX	-			
K20	VCCAUX	-			VCCAUX	-			
K21	VCCAUX	-			VCCAUX	-			
L10	VCCAUX	-			VCCAUX	-			
L11	VCCAUX	-			VCCAUX	-			
L20	VCCAUX	-			VCCAUX	-			
L21	VCCAUX	-			VCCAUX	-			
Y10	VCCAUX	-			VCCAUX	-			
Y11	VCCAUX	-			VCCAUX	-			
Y20	VCCAUX	-			VCCAUX	-			
Y21	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A13	GND	-			GND	-			
A18	GND	-			GND	-			
A24	GND	-			GND	-			
A30	GND	-			GND	-			
A7	GND	-			GND	-			
AA14	GND	-			GND	-			
AA15	GND	-			GND	-			
AA16	GND	-			GND	-			
AA17	GND	-			GND	-			
AA24	GND	-			GND	-			
AA27	GND	-			GND	-			
AA4	GND	-			GND	-			
AB24	GND	-			GND	-			
AB7	GND	-			GND	-			
AD12	GND	-			GND	-			
AD19	GND	-			GND	-			
AD27	GND	-			GND	-			
AE22	GND	-			GND	-			
AE27	GND	-			GND	-			
AE4	GND	-			GND	-			
AE9	GND	-			GND	-			
AF14	GND	-			GND	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G7	PL8A	7	LDQ6	T (LVDS)*	NC	-			
G8	PL6A	7	LDQS6****	T (LVDS)*	NC	-			
G9	PL5A	7	LDQ6	T	NC	-			
H19	NC	-			NC	-			
H20	NC	-			NC	-			
H21	NC	-			NC	-			
H22	NC	-			NC	-			
H6	PL8B	7	LDQ6	C (LVDS)*	NC	-			
H8	PL5B	7	LDQ6	C	NC	-			
H9	PL2A	7	LDQ6	T (LVDS)*	NC	-			
J10	PL2B	7	LDQ6	C (LVDS)*	NC	-			
J20	NC	-			NC	-			
J21	NC	-			NC	-			
J9	PL4A	7	LDQ6	T (LVDS)*	NC	-			
K9	PL4B	7	LDQ6	C (LVDS)*	NC	-			
R9	NC	-			NC	-			
U22	NC	-			NC	-			
W9	NC	-			NC	-			
N13	VCCPLL	-			VCCPLL	-			
N18	VCCPLL	-			VCCPLL	-			
V13	VCCPLL	-			VCCPLL	-			
V18	VCCPLL	-			VCCPLL	-			

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA8	PL65A	6	LDQ64	T	PL73A	6	LDQ72	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y9	PL65B	6	LDQ64	C	PL73B	6	LDQ72	C
AA6	PL66A	6	LDQ64	T (LVDS)*	PL74A	6	LDQ72	T (LVDS)*
AA7	PL66B	6	LDQ64	C (LVDS)*	PL74B	6	LDQ72	C (LVDS)*
AA4	PL67A	6	LDQ64	T	PL75A	6	LDQ72	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA3	PL67B	6	LDQ64	C	PL75B	6	LDQ72	C
AA9	PL69A	6	LDQ73	T (LVDS)*	PL77A	6	LDQ81	T (LVDS)*
AA10	PL69B	6	LDQ73	C (LVDS)*	PL77B	6	LDQ81	C (LVDS)*
AA5	PL70A	6	LDQ73	T	PL78A	6	LDQ81	T
AB6	PL70B	6	LDQ73	C	PL78B	6	LDQ81	C
AB1	PL71A	6	LDQ73	T (LVDS)*	PL79A	6	LDQ81	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AB2	PL71B	6	LDQ73	C (LVDS)*	PL79B	6	LDQ81	C (LVDS)*
AC8	PL72A	6	LDQ73	T	PL80A	6	LDQ81	T
AB10	PL72B	6	LDQ73	C	PL80B	6	LDQ81	C
AC1	PL73A	6	LDQS73	T (LVDS)*	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AC2	PL73B	6	LDQ73	C (LVDS)*	PL81B	6	LDQ81	C (LVDS)*
AB7	PL74A	6	LDQ73	T	PL82A	6	LDQ81	T
AB5	PL74B	6	LDQ73	C	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6			VCCIO6	6		
AC3	PL75A	6	LDQ73	T (LVDS)*	PL83A	6	LDQ81	T (LVDS)*
AC4	PL75B	6	LDQ73	C (LVDS)*	PL83B	6	LDQ81	C (LVDS)*
AC10	PL76A	6	LDQ73	T	PL84A	6	LDQ81	T
AC9	PL76B	6	LDQ73	C	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-			GNDIO6	-		
AC7	NC	-			PL86A	6	LDQ90	T (LVDS)*
AC5	NC	-			PL86B	6	LDQ90	C (LVDS)*
AC6	NC	-			PL87A	6	LDQ90	T
AD5	NC	-			PL87B	6	LDQ90	C
-	-	-			VCCIO6	6		
AD4	NC	-			PL88A	6	LDQ90	T (LVDS)*
AD3	NC	-			PL88B	6	LDQ90	C (LVDS)*
AD10	NC	-			PL89A	6	LDQ90	T
AD8	NC	-			PL89B	6	LDQ90	C
-	-	-			GNDIO6	-		
AD2	NC	-			PL90A	6	LDQS90	T (LVDS)*
AD1	NC	-			PL90B	6	LDQ90	C (LVDS)*
AD9	NC	-			PL91A	6	LDQ90	T
-	-	-			VCCIO6	6		
AC11	NC	-			PL91B	6	LDQ90	C
AD6	NC	-			PL92A	6	LDQ90	T (LVDS)*
AD7	NC	-			PL92B	6	LDQ90	C (LVDS)*
AE1	NC	-			PL93A	6	LDQ90	T
-	-	-			GNDIO6	-		
AE2	NC	-			PL93B	6	LDQ90	C
AF2	PL78A	6	LDQ82	T (LVDS)*	PL95A	6	LDQ99	T (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK20	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
AN22	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
AL21	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AH19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
AJ20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
AD20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
AF20	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ19	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
AH20	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
AE20	PB73A	4	BDQ69	T	PB82A	4	BDQ78	T
AG20	PB73B	4	BDQ69	C	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
AH22	NC	-			PB89A	4	BDQ87	T
-	-	-			VCCIO4	4		
AH21	NC	-			PB89B	4	BDQ87	C
AG22	NC	-			PB90A	4	BDQ87	T
AG21	NC	-			PB90B	4	BDQ87	C
-	-	-			GNDIO4	-		
AM22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T
AL22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AP23	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T
AN23	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AM24	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T
AL24	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C
AK22	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T
AJ22	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C
AL23	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T
AK23	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4			VCCIO4	4		
AJ23	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T
AH23	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-			GNDIO4	-		
AL28	LRC_SQ_VCCRX3	13			LRC_SQ_VCCRX3	13		
AM26	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T
AN26	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13		
AM27	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C
AN27	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13		
AP26	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T
AL26	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13		
AP27	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C
AN28	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13		
AP28	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C
AK28	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13		
AP29	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484C	331	1.2V	-5	fpBGA	484	COM	35
LFE2-35E-6F484C	331	1.2V	-6	fpBGA	484	COM	35
LFE2-35E-7F484C	331	1.2V	-7	fpBGA	484	COM	35
LFE2-35E-5F672C	450	1.2V	-5	fpBGA	672	COM	35
LFE2-35E-6F672C	450	1.2V	-6	fpBGA	672	COM	35
LFE2-35E-7F672C	450	1.2V	-7	fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484C	339	1.2V	-5	fpBGA	484	COM	50
LFE2-50E-6F484C	339	1.2V	-6	fpBGA	484	COM	50
LFE2-50E-7F484C	339	1.2V	-7	fpBGA	484	COM	50
LFE2-50E-5F672C	500	1.2V	-5	fpBGA	672	COM	50
LFE2-50E-6F672C	500	1.2V	-6	fpBGA	672	COM	50
LFE2-50E-7F672C	500	1.2V	-7	fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672C	500	1.2V	-5	fpBGA	672	COM	70
LFE2-70E-6F672C	500	1.2V	-6	fpBGA	672	COM	70
LFE2-70E-7F672C	500	1.2V	-7	fpBGA	672	COM	70
LFE2-70E-5F900C	583	1.2V	-5	fpBGA	900	COM	70
LFE2-70E-6F900C	583	1.2V	-6	fpBGA	900	COM	70
LFE2-70E-7F900C	583	1.2V	-7	fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144I	90	1.2V	-5	TQFP	144	IND	6
LFE2-6E-6T144I	90	1.2V	-6	TQFP	144	IND	6
LFE2-6E-5F256I	190	1.2V	-5	fpBGA	256	IND	6
LFE2-6E-6F256I	190	1.2V	-6	fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144I	93	1.2V	-5	TQFP	144	IND	12
LFE2-12E-6T144I	93	1.2V	-6	TQFP	144	IND	12
LFE2-12E-5Q208I	131	1.2V	-5	PQFP	208	IND	12
LFE2-12E-6Q208I	131	1.2V	-6	PQFP	208	IND	12
LFE2-12E-5F256I	193	1.2V	-5	fpBGA	256	IND	12
LFE2-12E-6F256I	193	1.2V	-6	fpBGA	256	IND	12
LFE2-12E-5F484I	297	1.2V	-5	fpBGA	484	IND	12
LFE2-12E-6F484I	297	1.2V	-6	fpBGA	484	IND	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Date	Version	Section	Change Summary
June 2013 (cont.)	04.0 (cont.)	DC and Switching Characteristics	sysCLOCK SPLL Timing table – Corrected signal names for t_{RST} parameter.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added t_{SUMCDI} and t_{HMCDI} parameters.
September 2013	04.1	Architecture	Updated Selectable Master Clock (CCLK) Frequencies during Configuration table.
		DC and Switching Characteristics	Added information on f_{MAXSPI} parameter in LatticeECP2/M sys-CONFIG Port Timing Specifications table.