Lattice Semiconductor Corporation - LFE2-20SE-5QN208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Not For New Designs
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5qn208c

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sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

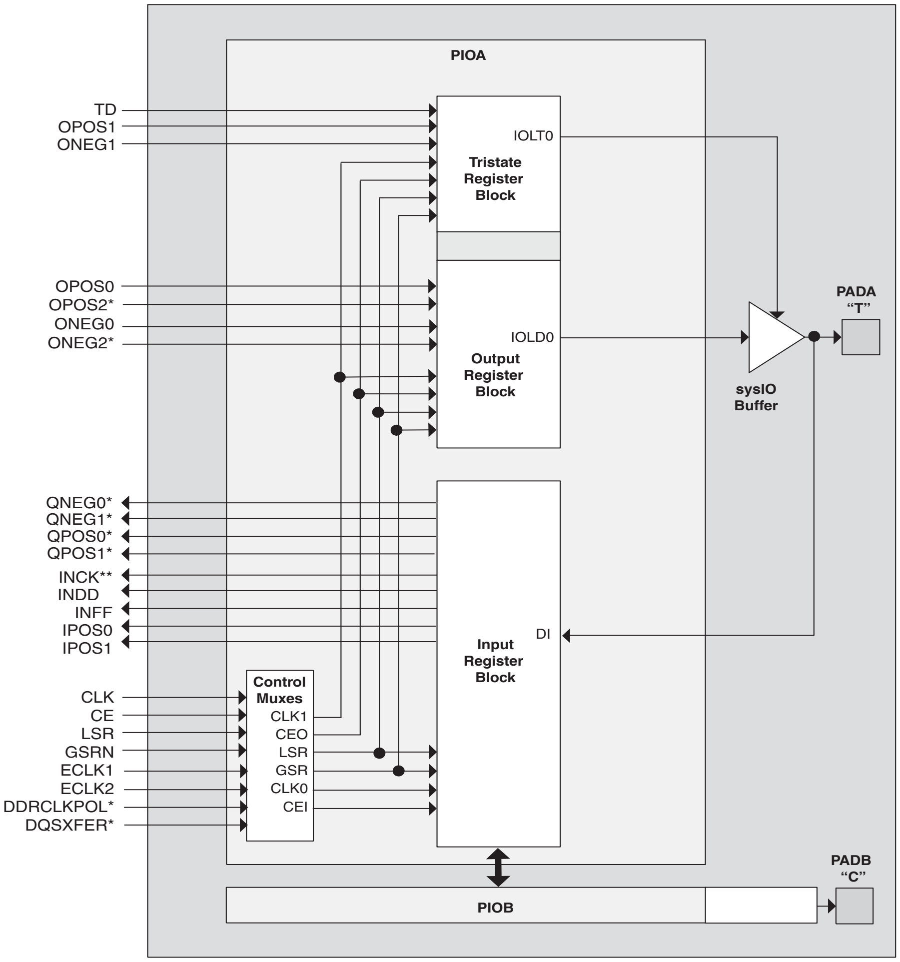
Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

Figure 2-28. PIC Diagram



*Signals are available on left/right/bottom edges only.
** Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-28. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

Figure 2-29. Input Register Block for Left, Right and Bottom Edges

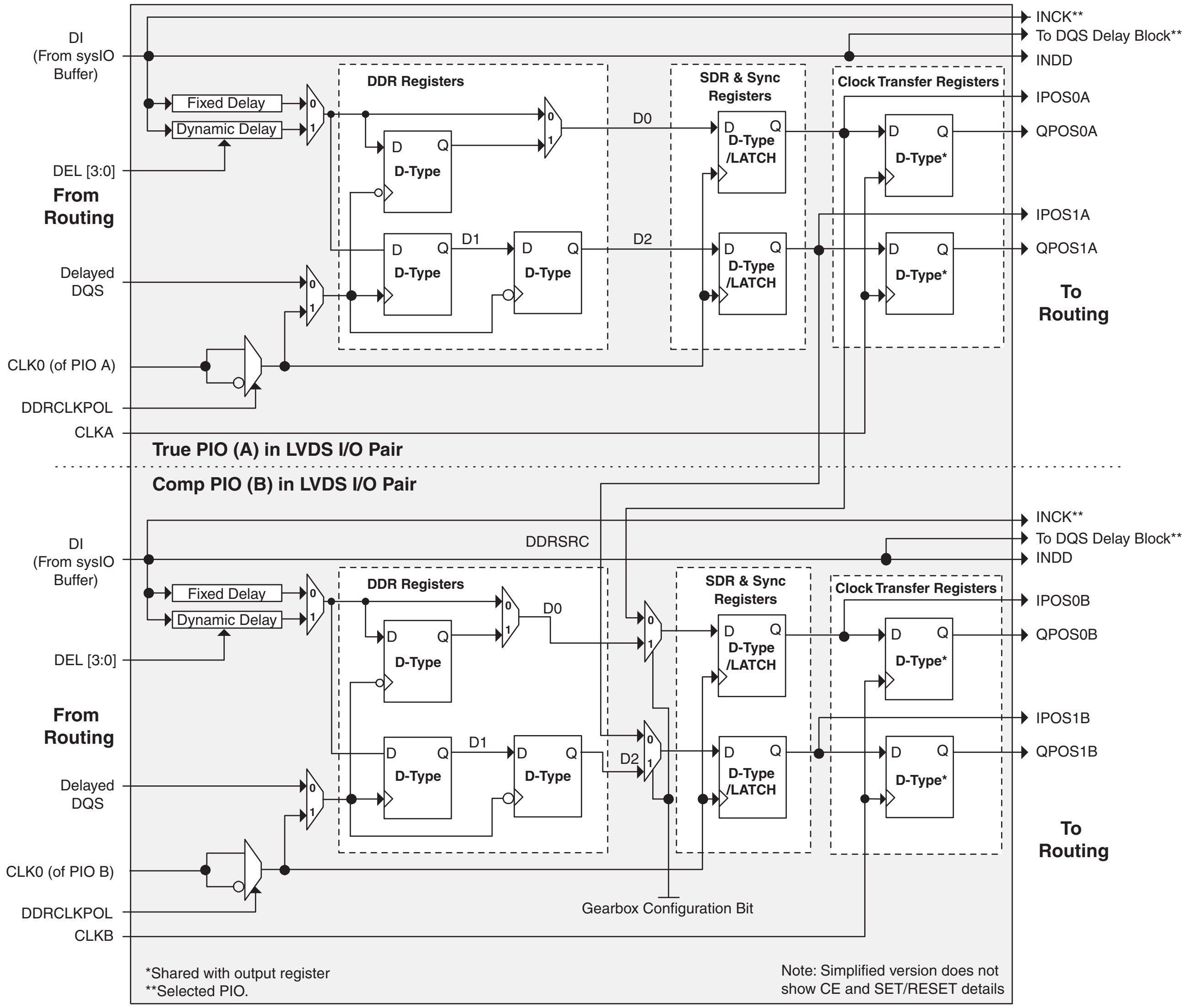
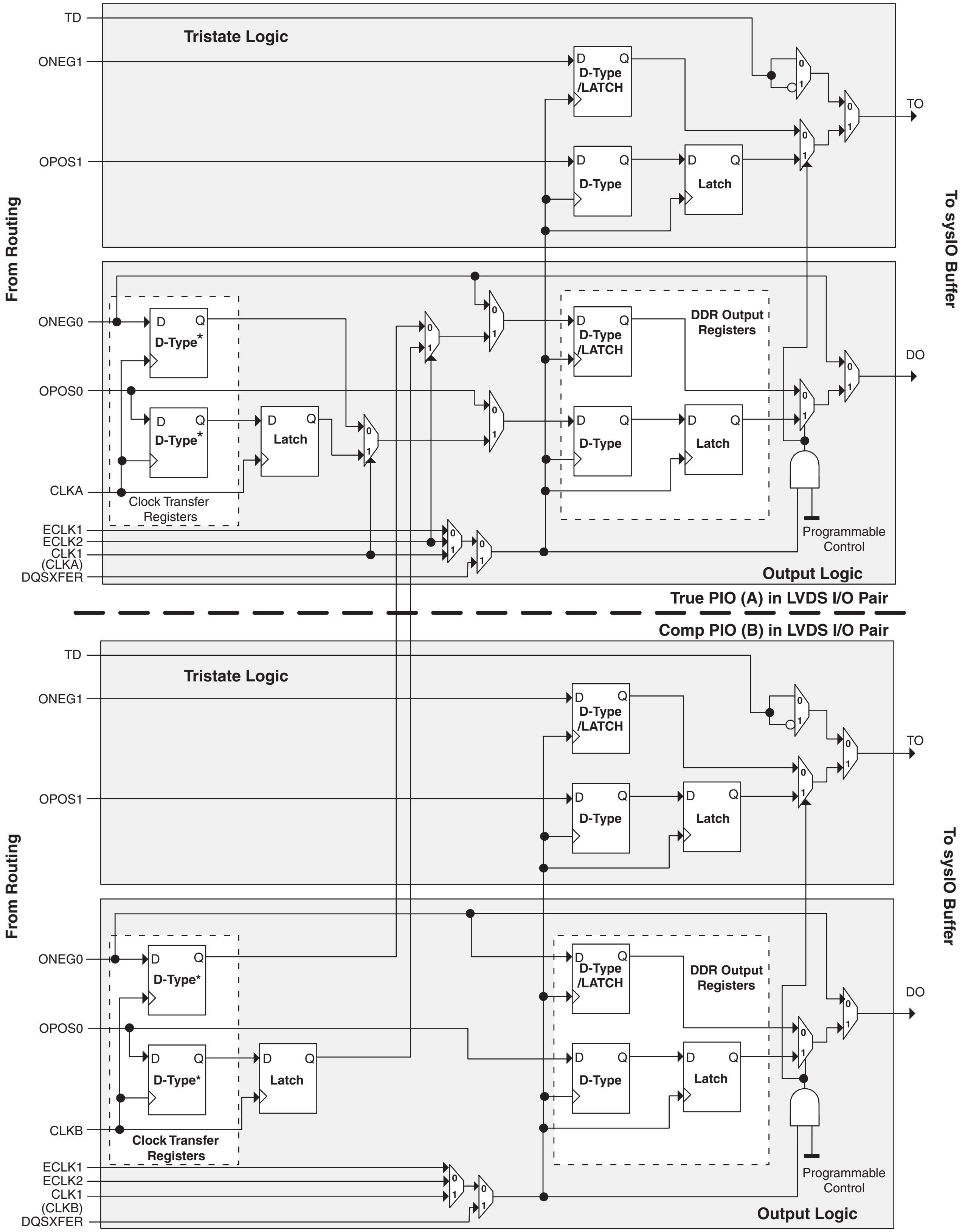


Figure 2-31. Output and Tristate Block for Left, Right and Bottom Edges



* Shared with input register

Note: Simplified version does not show CE and SET/RESET details

Figure 2-37. LatticeECP2 Banks

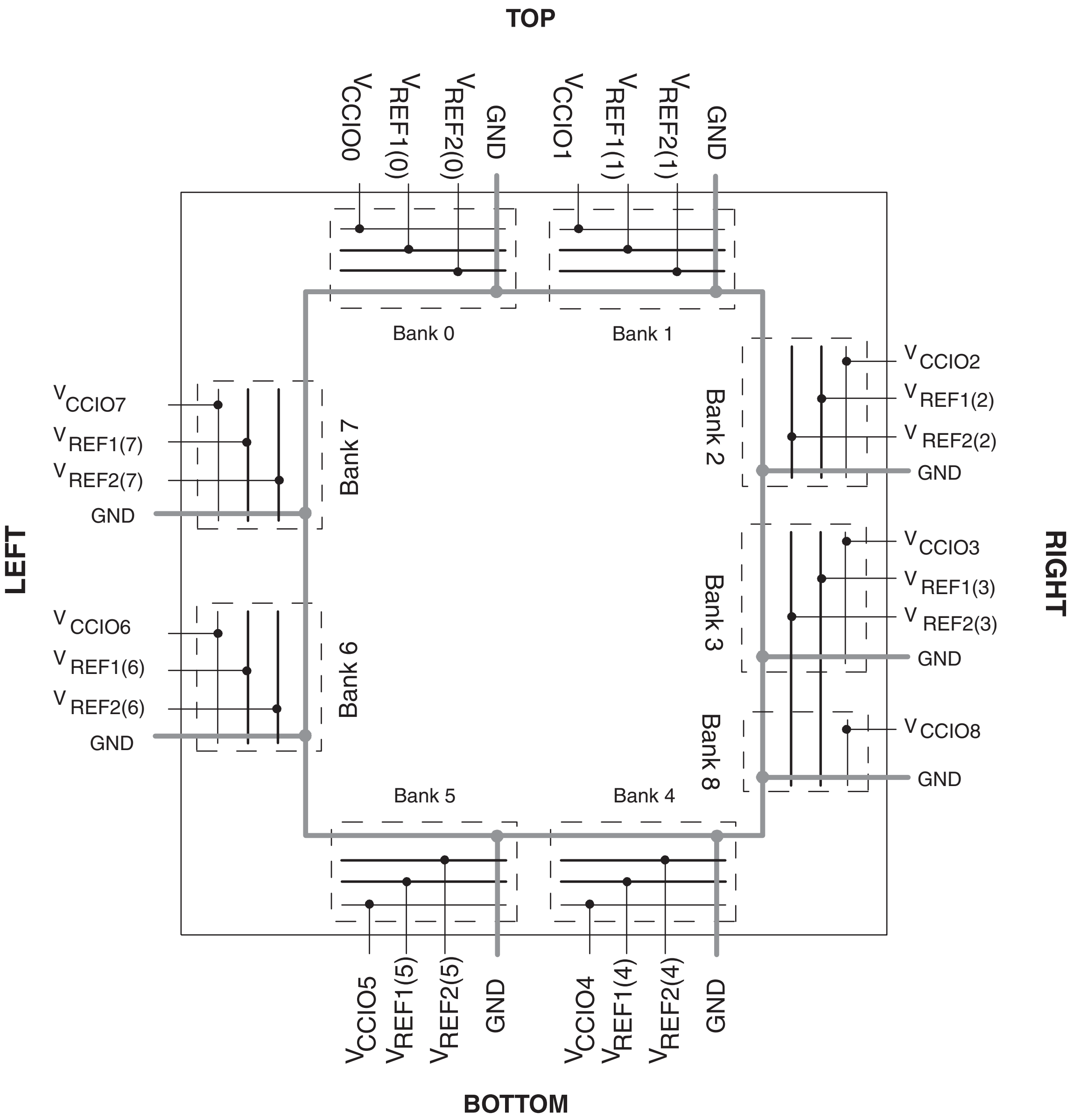
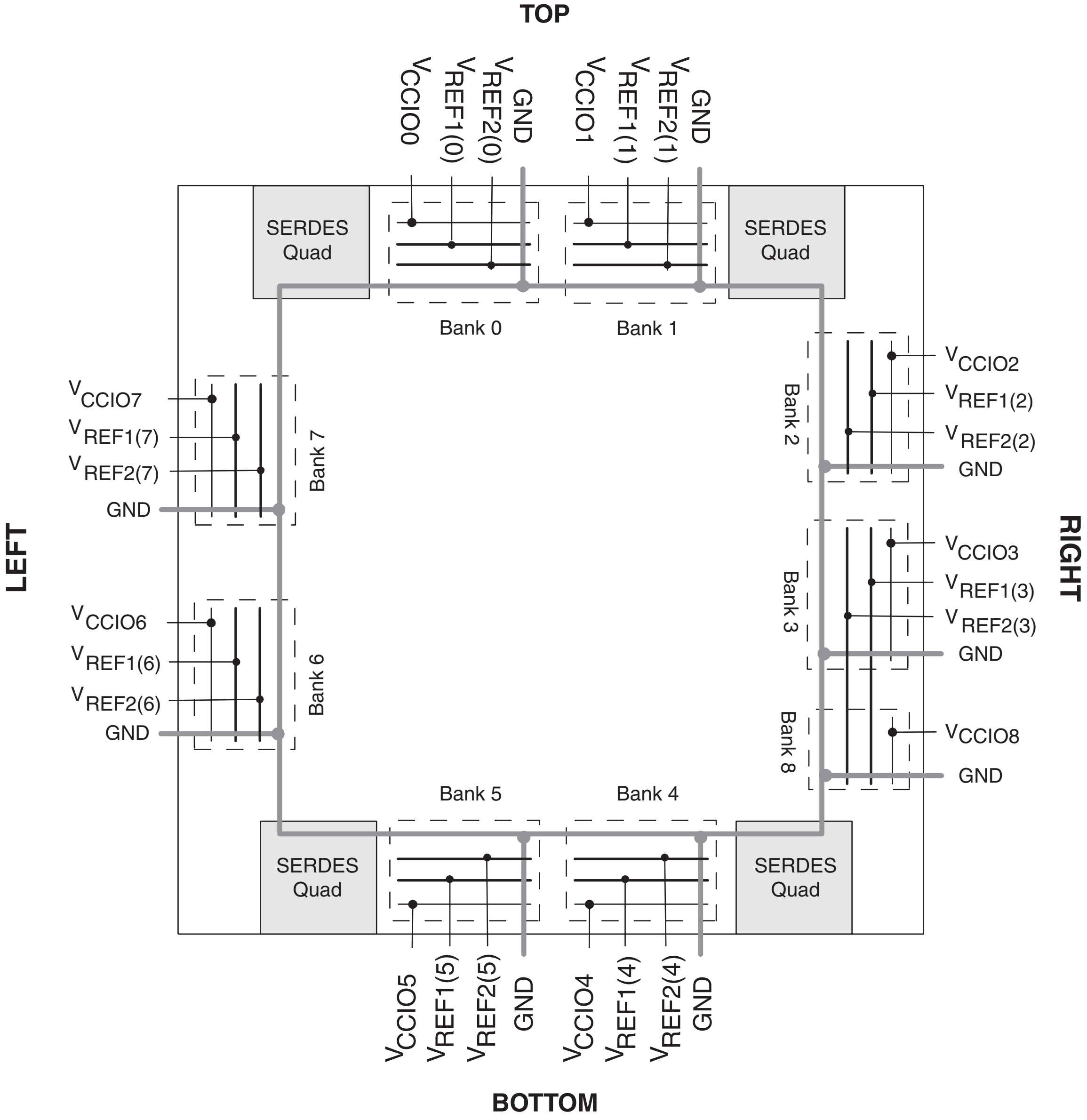


Figure 2-38. LatticeECP2M Banks



LatticeECP2/M devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Bottom (Bank 4 and Bank 5) sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the bottom banks of the device consist of two single-ended output drivers and two

LatticeECP2/M Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t_{RSTREC_SPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing[2,3]								
t_{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t_{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t_{tHP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t_{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
$t_{SUADDSUB}$	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
$t_{HADDSUB}$	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Single Ended User I/O		90	190	93	131	193	297
Differential Pair User I/O		43	95	45	62	96	148
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	34	54	33	40	54	57
	Dedicated Pins	3	3	3	3	3	3
VCC		10	7	10	14	7	16
VCCAUX		4	4	4	8	4	16
VCCPLL		0	0	0	0	0	0
VCCIO	Bank0	1	2	1	2	2	4
	Bank1	1	2	1	2	2	4
	Bank2	1	2	1	2	2	4
	Bank3	1	2	1	2	2	4
	Bank4	1	2	1	2	2	4
	Bank5	1	2	1	2	2	4
	Bank6	1	2	1	2	2	4
	Bank7	1	2	1	2	2	4
	Bank8	1	1	1	2	1	2
GND, GND0 to GND7		12	20	12	22	20	60
NC		4	3	1	0	0	44
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	8/4	18/6	8/4	18/9	18/9	50/25
	Bank1	17/8	34/17	18/9	18/9	34/17	46/23
	Bank2	4/2	20/10	4/2	11/5	20/10	24/12
	Bank3	8/4	12/6	8/4	11/5	12/6	16/8
	Bank4	18/9	32/16	18/9	19/9	32/16	46/23
	Bank5	8/4	14/7	10/5	18/9	17/8	46/23
	Bank6	9/4	26/13	9/4	18/8	26/13	32/16
	Bank7	12/6	20/10	12/6	12/6	20/10	23/11
	Bank8	6/2	14/7	6/2	6/2	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	1	5	1	4	5	6
	Bank3 (Right Edge)	3	3	3	3	3	4
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	2	7	2	6	7	8
	Bank7 (Left Edge)	5	5	5	5	5	5
	Bank8 (Right Edge)	0	0	0	0	0	0

LatticeECP2M Power Supply and NC

Signal	256 fpBGA	484 fpBGA
V_{CC}	G7, G9, H7, J10, K10, K8	J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
V_{CCIO0}	E7	B5, B9, E7, H9
V_{CCIO1}	E10	D13, E16, H14
V_{CCIO2}	E14, G12	E21, G18, J15, K19
V_{CCIO3}	K12, M14	N19, P15, T18, V21
V_{CCIO4}	M10, P12	AA18, R14, V16, W13
V_{CCIO5}	M7, P5	AA5, R9, V7, W10
V_{CCIO6}	K5, M3	N4, P8, T5, V2
V_{CCIO7}	E3, G5	E2, G5, J8, K4
V_{CCIO8}	T15	AA22, U19
V_{CCJ}	K7	W4
V_{CCAUX}	G8, H10, J7, K9	H11, H12, L15, L8, M15, M8, R11, R12
V_{CCPLL}	G10	R8, H15, H8, R15
SERDES Power[3]	C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3	C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10
GND[1]	A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13
NC[2]	D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9	**LFE2M20:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15 **LFE2M35:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15, U6 **LFE2M50:** Y15, W15, AB20, AB21, AA20, AB19, AB18, Y22, Y21, Y17, Y18, Y16, W17, Y19, Y20, W19, W18, V17, V18, D15, G14, G15, D14, E15, E14, F15, F14, F13, G12, G13

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
-	-	-			GNDIO7	-		
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*
F4	PL3A	7		T	PL5A	7	LDQ8	T
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*
F5	PL3B	7		C	PL5B	7	LDQ8	C
VCCIO	VCCIO7	7			VCCIO7	7		
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*
G6	PL5A	7		T	PL7A	7	LDQ8	T
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*
G7	PL5B	7		C	PL7B	7	LDQ8	C
GNDIO	GNDIO7	-			GNDIO7	-		
F1	NC	-			PL9A	7	LDQ8	T
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*
F2	NC	-			PL9B	7	LDQ8	C
-	-	-			VCCIO7	7		
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*
G1	NC	-			PL11A	7	LDQ8	T
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*
G2	NC	-			PL11B	7	LDQ8	C
-	-	-			GNDIO	-		
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T
VCCIO	VCCIO7	7			VCCIO7	7		
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO	-		
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T
VCCIO	VCCIO7	7			VCCIO7	7		
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO	-		
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*
VCCIO	VCCIO6	6			-	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7/LDQ6	T (LVDS)*
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7/LDQ6	C (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
F6	PL3A	7		T	PL3A	7	LDQ6	T
F5	PL3B	7		C	PL3B	7	LDQ6	C
VCCIO	VCCIO7	7			VCCIO7	7		
E4	NC	-			PL4A	7	LDQ6	T (LVDS)*
E3	NC	-			PL4B	7	LDQ6	C (LVDS)*
E2	NC	-			PL5A	7	LDQ6	T
E1	NC	-			PL5B	7	LDQ6	C
GND	GNDIO7	-			GNDIO7	-		
H6	NC	-			PL6A	7	LDQS6	T (LVDS)*
H5	NC	-			PL6B	7	LDQ6	C (LVDS)*
F2	NC	-			PL7A	7	LDQ6	T
VCCIO	VCCIO7	7			VCCIO7	7		
F1	NC	-			PL7B	7	LDQ6	C
H8	NC	-			PL8A	7	LDQ6	T (LVDS)*
J9	NC	-			PL8B	7	LDQ6	C (LVDS)*
G4	NC	-			PL9A	7	LDQ6	T
GND	GNDIO7	-			GNDIO7	-		
G3	NC	-			PL9B	7	LDQ6	C
H7	PL4A	7	LDQ8	T (LVDS)*	PL10A	7	LDQ14	T (LVDS)*
J8	PL4B	7	LDQ8	C (LVDS)*	PL10B	7	LDQ14	C (LVDS)*
G2	PL5A	7	LDQ8	T	PL11A	7	LDQ14	T
G1	PL5B	7	LDQ8	C	PL11B	7	LDQ14	C
H3	PL6A	7	LDQ8	T (LVDS)*	PL12A	7	LDQ14	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
H4	PL6B	7	LDQ8	C (LVDS)*	PL12B	7	LDQ14	C (LVDS)*
J5	PL7A	7	LDQ8	T	PL13A	7	LDQ14	T
J4	PL7B	7	LDQ8	C	PL13B	7	LDQ14	C
J3	PL8A	7	LDQS8	T (LVDS)*	PL14A	7	LDQS14	T (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
K4	PL8B	7	LDQ8	C (LVDS)*	PL14B	7	LDQ14	C (LVDS)*
H1	PL9A	7	LDQ8	T	PL15A	7	LDQ14	T
H2	PL9B	7	LDQ8	C	PL15B	7	LDQ14	C
VCCIO	VCCIO7	7			VCCIO7	7		
K6	PL10A	7	LDQ8	T (LVDS)*	PL16A	7	LDQ14	T (LVDS)*
K7	PL10B	7	LDQ8	C (LVDS)*	PL16B	7	LDQ14	C (LVDS)*
J1	PL11A	7	LDQ8	T	PL17A	7	LDQ14	T
J2	PL11B	7	LDQ8	C	PL17B	7	LDQ14	C
GND	GNDIO7	-			GNDIO7	-		
VCCIO	VCCIO7	7			VCCIO7	7		
K3	NC	-			NC	-		
K2	NC	-			NC	-		
GND	GNDIO7	-			GNDIO7	-		
K1	NC	-			NC	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-20E/20SE				LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U1	NC	-			PL34A	6	LDQ31	T
V1	NC	-			PL34B	6	LDQ31	C
GND	GNDIO6	-			GNDIO6	-		
P3	NC	-			NC	-		
R3	NC	-			NC	-		
R4	NC	-			NC	-		
U2	NC	-			NC	-		
VCCIO	VCCIO6	6			VCCIO6	6		
V2	NC	-			NC	-		
W2	NC	-			NC	-		
T6	NC	-			PL38A	6	LDQ39	T
R5	NC	-			PL38B	6	LDQ39	C
GND	GNDIO6	-			GNDIO6	-		
R6	PL25A	6	LDQS25***	T (LVDS)*	PL39A	6	LDQS39***	T (LVDS)*
R7	PL25B	6	LDQ25	C (LVDS)*	PL39B	6	LDQ39	C (LVDS)*
W1	PL26A	6	LDQ25	T	PL40A	6	LDQ39	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y2	PL26B	6	LDQ25	C	PL40B	6	LDQ39	C
Y1	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*	PL41A	6	LLM0_GDLLT_IN_A**/LDQ39	T (LVDS)*
AA2	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*	PL41B	6	LLM0_GDLLC_IN_A**/LDQ39	C (LVDS)*
T5	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T	PL42A	6	LLM0_GDLLT_FB_A/LDQ39	T
GND	GNDIO6	-			GNDIO6	-		
T7	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C	PL42B	6	LLM0_GDLLC_FB_A/LDQ39	C
R8	VCC	6			VCCPLL	6		
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
U3	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*	PL44A	6	LLM0_GPLLT_IN_A**/LDQ48	T (LVDS)*
U4	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*	PL44B	6	LLM0_GPLLC_IN_A**/LDQ48	C (LVDS)*
V3	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T	PL45A	6	LLM0_GPLLT_FB_A/LDQ48	T
U5	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C	PL45B	6	LLM0_GPLLC_FB_A/LDQ48	C
V4	PL32A	6	LDQ34	T (LVDS)*	PL46A	6	LDQ48	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V5	PL32B	6	LDQ34	C (LVDS)*	PL46B	6	LDQ48	C (LVDS)*
Y3	PL33A	6	LDQ34	T	PL47A	6	LDQ48	T
Y4	PL33B	6	LDQ34	C	PL47B	6	LDQ48	C
W3	PL34A	6	LDQS34	T (LVDS)*	PL48A	6	LDQS48	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
W4	PL34B	6	LDQ34	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*
AA1	PL35A	6	LDQ34	T	PL49A	6	LDQ48	T
AB1	PL35B	6	LDQ34	C	PL49B	6	LDQ48	C
VCCIO	VCCIO6	6			VCCIO6	6		
U8	PL36A	6	LDQ34	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*
U7	PL36B	6	LDQ34	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*
V8	PL37A	6	LDQ34	T	PL51A	6	LDQ48	T
U6	PL37B	6	LDQ34	C	PL51B	6	LDQ48	C
GND	GNDIO6	-			GNDIO6	-		
W6	PL38A	6	LDQ42	T (LVDS)*	PL52A	6	LDQ56	T (LVDS)*

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

	LFE2-20E/20SE				LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D4	PT7B	0		C	PT7B	0		C
D3	PT7A	0		T	PT7A	0		T
C2	PT6B	0		C	PT6B	0		C
C1	PT6A	0		T	PT6A	0		T
G8	PT5B	0		C	PT5B	0		C
GND	GNDIO0	-			GNDIO0	-		
G7	PT5A	0		T	PT5A	0		T
E7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT4A	0		T	PT4A	0		T
E6	PT3B	0		C	PT3B	0		C
E5	PT3A	0		T	PT3A	0		T
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
D11	VCCIO0	0			VCCIO0	0		
D6	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		
J12	VCCIO0	0			VCCIO0	0		
D16	VCCIO1	1			VCCIO1	1		
D21	VCCIO1	1			VCCIO1	1		
G18	VCCIO1	1			VCCIO1	1		
J15	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
F23	VCCIO2	2			VCCIO2	2		
J20	VCCIO2	2			VCCIO2	2		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R19	GND	-		
R20	GND	-		
T11	GND	-		
T12	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T19	GND	-		
T20	GND	-		
U11	GND	-		
U12	GND	-		
U13	GND	-		
U14	GND	-		
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U19	GND	-		
U20	GND	-		
V12	GND	-		
V13	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V18	GND	-		
V19	GND	-		
V28	GND	-		
V3	GND	-		
W12	GND	-		
W13	GND	-		
W14	GND	-		
W15	GND	-		
W16	GND	-		
W17	GND	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

	LFE2M20E/SE				LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A3	GND	-			GND	-		
A9	GND	-			GND	-		
B12	GND	-			GND	-		
B6	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		
R12	GND	-			GND	-		
R5	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
D10	NC	-			NC	-		
D11	NC	-			NC	-		
D12	NC	-			NC	-		
D13	NC	-			NC	-		
D14	NC	-			NC	-		
D4	NC	-			NC	-		
D5	NC	-			NC	-		
D6	NC	-			NC	-		
D7	NC	-			NC	-		
E11	NC	-			NC	-		
E6	NC	-			NC	-		
E8	NC	-			NC	-		
E9	NC	-			NC	-		
F10	NC	-			NC	-		
F7	NC	-			NC	-		
F8	NC	-			NC	-		
F9	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO0	-			GNDIO0	-		
F7	PT9B	0		C	PT9B	0		C
G7	PT9A	0		T	PT9A	0		T
C3	PT8B	0		C	PT8B	0		C
D4	PT8A	0		T	PT8A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F6	PT7B	0		C	PT7B	0		C
E6	PT7A	0		T	PT7A	0		T
E5	PT6B	0		C	PT6B	0		C
D6	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
D3	PT5B	0		C	PT5B	0		C
E3	PT5A	0		T	PT5A	0		T
D5	PT4B	0		C	PT4B	0		C
E4	PT4A	0		T	PT4A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
C2	PT3B	0		C	PT3B	0		C
B2	PT3A	0		T	PT3A	0		T
B1	PT2B	0		C	PT2B	0		C
C1	PT2A	0		T	PT2A	0		T
R8	VCCPLL	-			VCCPLL	-		
H15	VCCPLL	-			VCCPLL	-		
H8	VCCPLL	-			VCCPLL	-		
R15	VCCPLL	-			VCCPLL	-		
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
B5	VCCIO0	0			VCCIO0	0		
B9	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
D13	VCCIO1	1			VCCIO1	1		
E16	VCCIO1	1			VCCIO1	1		
H14	VCCIO1	1			VCCIO1	1		
E21	VCCIO2	2			VCCIO2	2		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	NC	-			NC	-		
F14	NC	-			NC	-		
F13	NC	-			NC	-		
G12	NC	-			NC	-		
G13	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
GNDIO	GNDIO7	-		
L1	PL36A	7	LDQS36	T (LVDS)*
L2	PL36B	7	LDQ36	C (LVDS)*
M7	PL37A	7	LDQ36	T
VCCIO	VCCIO7	7		
L5	PL37B	7	LDQ36	C
L3	PL38A	7	LDQ36	T (LVDS)*
L4	PL38B	7	LDQ36	C (LVDS)*
M1	PL39A	7	PCLKT7_0/LDQ36	T
GNDIO	GNDIO7	-		
M2	PL39B	7	PCLKC7_0/LDQ36	C
M6	PL41A	6	PCLKT6_0	T (LVDS)*
M5	PL41B	6	PCLKC6_0	C (LVDS)*
M3	PL42A	6	VREF2_6	T
M4	PL42B	6	VREF1_6	C
VCCIO	VCCIO6	6		
N7	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	-		
N6	PL45B	6	LLM3_SPLLC_IN_A	C (LVDS)*
N1	PL46A	6	LLM3_SPLLT_FB_A	T
N2	PL46B	6	LLM3_SPLLC_FB_A	C
VCCIO	VCCIO6	6		
GNDIO	GNDIO6	-		
P6	PL52A	6	LDQS52****	T (LVDS)*
N5	PL52B	6	LDQ52	C (LVDS)*
P1	PL53A	6	LDQ52	T
VCCIO	VCCIO6	6		
P2	PL53B	6	LDQ52	C
P3	PL54A	6	LDQ52	T (LVDS)*
P4	PL54B	6	LDQ52	C (LVDS)*
P5	PL55A	6	LDQ52	T
GNDIO	GNDIO6	-		
P7	PL55B	6	LDQ52	C
VCCIO	VCCIO6	6		
GNDIO	GNDIO6	-		
R1	PL62A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
GNDIO	GNDIO6	-		
R2	PL62B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
R3	PL63A	6	LLM0_GPLLT_FB_A	T
R4	PL63B	6	LLM0_GPLLC_FB_A	C
VCCIO	VCCIO6	6		
R6	PL64A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
R5	PL64B	6	LLM0_GDLLC_IN_A**	C (LVDS)*

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
D19	PT93B	1		C
E18	PT93A	1		T
D18	PT92B	1		C
C17	PT92A	1		T
A17	PT91B	1		C
B17	PT91A	1		T
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
J18	PT75B	1		C
J19	PT75A	1		T
H17	PT74B	1		C
J17	PT74A	1		T
F18	PT73B	1		C
F17	PT73A	1		T
GNDIO	GNDIO1	-		
A16	PT72B	1		C
B16	PT72A	1		T
G17	PT71B	1		C
G16	PT71A	1		T
VCCIO	VCCIO1	1		
H16	PT70B	1		C
F16	PT70A	1		T
J16	PT69B	1		C
G15	PT69A	1		T
GNDIO	GNDIO1	-		
C16	PT68B	1		C
D16	PT68A	1		T
J15	PT67B	1		C
H15	PT67A	1		T
VCCIO	VCCIO1	1		
A15	PT66B	1	VREF2_1	C
B15	PT66A	1	VREF1_1	T
F15	PT65B	1	PCLKC1_0	C
E16	PT65A	1	PCLKT1_0	T
C15	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
D15	PT64A	0	PCLKT0_0	T
C14	PT63B	0	VREF2_0	C
E15	PT63A	0	VREF1_0	T
G14	PT62B	0		C
VCCIO	VCCIO0	0		
J14	PT62A	0		T
F14	PT61B	0		C

LatticeECP2 Standard Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144C	90	1.2V	-5	TQFP	144	COM	6
LFE2-6E-6T144C	90	1.2V	-6	TQFP	144	COM	6
LFE2-6E-7T144C	90	1.2V	-7	TQFP	144	COM	6
LFE2-6E-5F256C	190	1.2V	-5	fpBGA	256	COM	6
LFE2-6E-6F256C	190	1.2V	-6	fpBGA	256	COM	6
LFE2-6E-7F256C	190	1.2V	-7	fpBGA	256	COM	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144C	93	1.2V	-5	TQFP	144	COM	12
LFE2-12E-6T144C	93	1.2V	-6	TQFP	144	COM	12
LFE2-12E-7T144C	93	1.2V	-7	TQFP	144	COM	12
LFE2-12E-5Q208C	131	1.2V	-5	PQFP	208	COM	12
LFE2-12E-6Q208C	131	1.2V	-6	PQFP	208	COM	12
LFE2-12E-7Q208C	131	1.2V	-7	PQFP	208	COM	12
LFE2-12E-5F256C	193	1.2V	-5	fpBGA	256	COM	12
LFE2-12E-6F256C	193	1.2V	-6	fpBGA	256	COM	12
LFE2-12E-7F256C	193	1.2V	-7	fpBGA	256	COM	12
LFE2-12E-5F484C	297	1.2V	-5	fpBGA	484	COM	12
LFE2-12E-6F484C	297	1.2V	-6	fpBGA	484	COM	12
LFE2-12E-7F484C	297	1.2V	-7	fpBGA	484	COM	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5Q208C	131	1.2V	-5	PQFP	208	COM	20
LFE2-20E-6Q208C	131	1.2V	-6	PQFP	208	COM	20
LFE2-20E-7Q208C	131	1.2V	-7	PQFP	208	COM	20
LFE2-20E-5F256C	193	1.2V	-5	fpBGA	256	COM	20
LFE2-20E-6F256C	193	1.2V	-6	fpBGA	256	COM	20
LFE2-20E-7F256C	193	1.2V	-7	fpBGA	256	COM	20
LFE2-20E-5F484C	331	1.2V	-5	fpBGA	484	COM	20
LFE2-20E-6F484C	331	1.2V	-6	fpBGA	484	COM	20
LFE2-20E-7F484C	331	1.2V	-7	fpBGA	484	COM	20
LFE2-20E-5F672C	402	1.2V	-5	fpBGA	672	COM	20
LFE2-20E-6F672C	402	1.2V	-6	fpBGA	672	COM	20
LFE2-20E-7F672C	402	1.2V	-7	fpBGA	672	COM	20