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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Not For New Designs
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	131
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-5qn208i

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available on each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-7 shows the capabilities of the block.

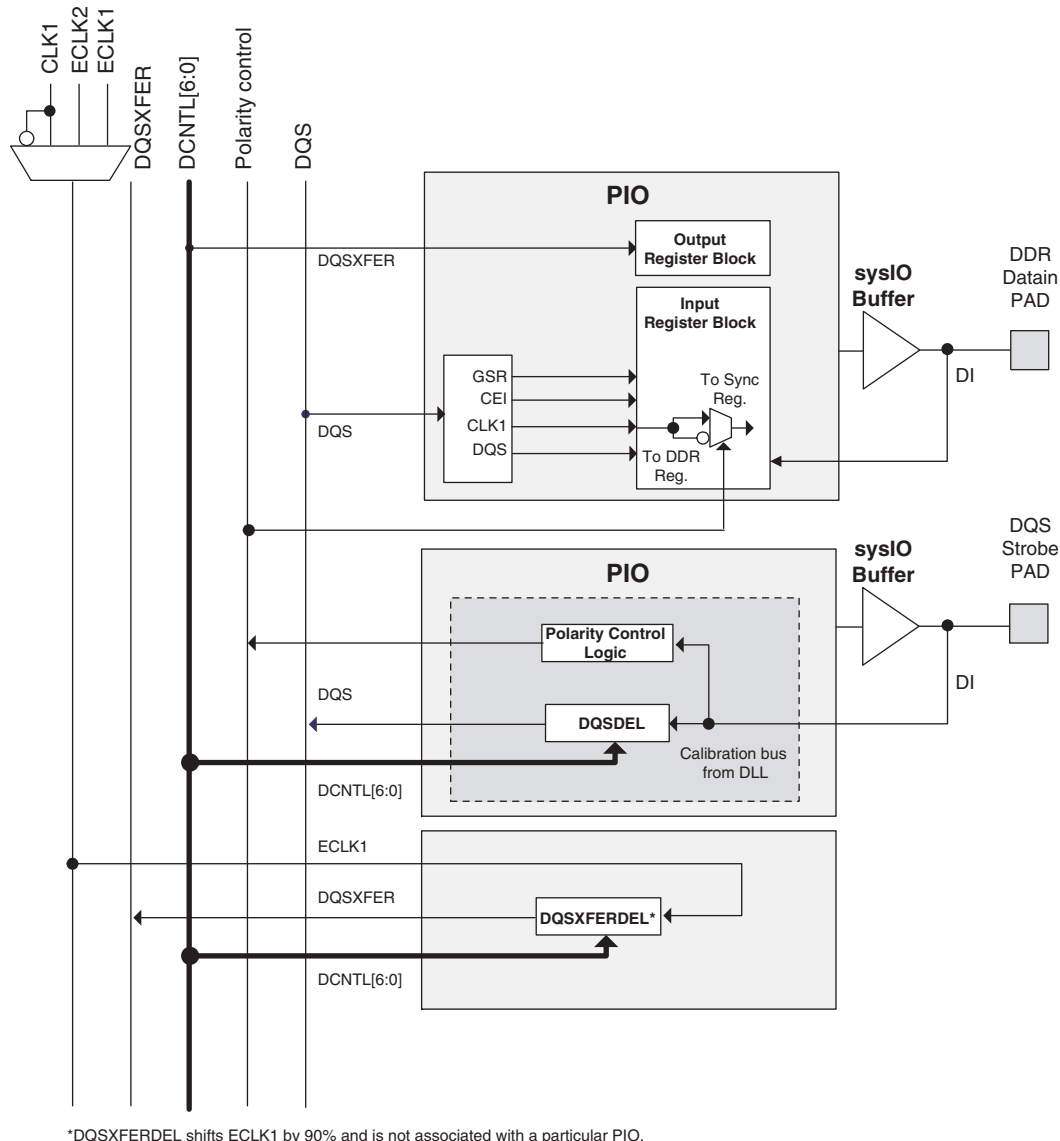
Table 2-7. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADDSUB	4	2	—
MULTADDSUBSUM	2	1	—

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the ‘Signed/Unsigned’ options the operands can be switched between signed and unsigned on every cycle.
- In the ‘Add/Sub’ option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

Figure 2-36. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

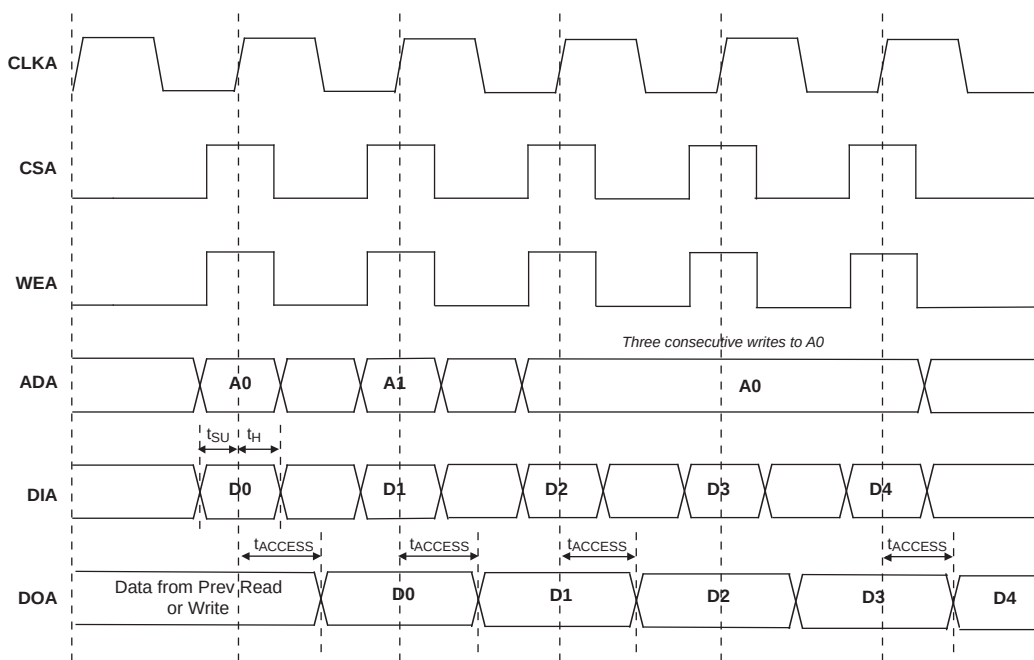
Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR2}	DDR Clock Frequency	ECP2/M	133	266	133	200	133	166	MHz
SPI4.2 I/O Pin Parameters Static Alignment^{4, 8, 11}									
	Maximum Data Rate	ECP2-20	—	750	—	622	—	622	Mbps
		ECP2-35	—	750	—	622	—	622	Mbps
		ECP2-50	—	750	—	622	—	622	Mbps
		ECP2-70	—	750	—	622	—	622	Mbps
		ECP2M20	—	622	—	622	—	622	Mbps
		ECP2M35	—	622	—	622	—	622	Mbps
		ECP2M50	—	622	—	622	—	622	Mbps
		ECP2M70	—	622	—	622	—	622	Mbps
		ECP2M100	—	622	—	622	—	622	Mbps
$t_{DVACLKSPI}$	Data Valid After CLK (Receive)	ECP2-20	—	0.25	—	0.25	—	0.25	UI
		ECP2-35	—	0.25	—	0.25	—	0.25	UI
		ECP2-50	—	0.25	—	0.25	—	0.25	UI
		ECP2-70	—	0.25	—	0.25	—	0.25	UI
		ECP2M20	—	0.21	—	0.21	—	0.21	UI
		ECP2M35	—	0.21	—	0.21	—	0.21	UI
		ECP2M50	—	0.21	—	0.21	—	0.21	UI
		ECP2M70	—	0.21	—	0.21	—	0.21	UI
		ECP2M100	—	0.21	—	0.21	—	0.21	UI
$t_{DVECLKSPI}$	Data Hold After CLK (Receive)	ECP2-20	0.75	—	0.75	—	0.75	—	UI
		ECP2-35	0.75	—	0.75	—	0.75	—	UI
		ECP2-50	0.75	—	0.75	—	0.75	—	UI
		ECP2-70	0.75	—	0.75	—	0.75	—	UI
		ECP2M20	0.79	—	0.79	—	0.79	—	UI
		ECP2M35	0.79	—	0.79	—	0.79	—	UI
		ECP2M50	0.79	—	0.79	—	0.79	—	UI
		ECP2M70	0.79	—	0.79	—	0.79	—	UI
		ECP2M100	0.79	—	0.79	—	0.79	—	UI
t_{DIASPI}	Data Invalid After Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND ¹	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	LFE2M50: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 LFE2M70/LFE2M100: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC ²	LFE2M35: AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 LFE2M50: AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	LFE2M50: G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 LFE2M70/LFE2M100: AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T7	PL29B	6	LDQ28	C	PL43B	6	LDQ42	C	
T6	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
AA2	PL31A	6	LDQ28	T	PL45A	6	LDQ42	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y1	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	
AA1	PL31B	6	LDQ28	C	PL45B	6	LDQ42	C	
W1	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
V3	PL30B	6	LDQ28	C (LVDS)*	PL44B	6	LDQ42	C (LVDS)*	
GNDIO	GNDIO6	-			GNDIO	-			
V4	PL30A	6	LDQ28	T (LVDS)*	PL44A	6	LDQ42	T (LVDS)*	
U5	TDI	-			TDI	-			
U7	TCK	-			TCK	-			
V6	TDO	-			TDO	-			
V5	TMS	-			TMS	-			
T8	VCCJ	-			VCCJ	-			
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
GNDIO	GNDIO5	-			GNDIO	-			
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO	-			
-	-	-			VCCIO5	5			
Y6	PB12A	5	BDQ15	T	PB21A	5	BDQ24	T	
W7	PB11A	5	BDQ15	T	PB20A	5	BDQ24	T	
Y7	PB12B	5	BDQ15	C	PB21B	5	BDQ24	C	
W8	PB11B	5	BDQ15	C	PB20B	5	BDQ24	C	
U8	PB14A	5	BDQ15	T	PB23A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA7	PB13A	5	BDQ15	T	PB22A	5	BDQ24	T	
U9	PB14B	5	BDQ15	C	PB23B	5	BDQ24	C	

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB29B	5	BDQ33	C	PB29B	5	BDQ33	C	
AE10	PB30A	5	BDQ33	T	PB30A	5	BDQ33	T	
AF10	PB30B	5	BDQ33	C	PB30B	5	BDQ33	C	
W14	PB31A	5	BDQ33	T	PB31A	5	BDQ33	T	
AB13	PB31B	5	BDQ33	C	PB31B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB32A	5	BDQ33	T	PB32A	5	BDQ33	T	
AB14	PB32B	5	BDQ33	C	PB32B	5	BDQ33	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB33A	5	BDQS33	T	PB33A	5	BDQS33	T	
AF11	PB33B	5	BDQ33	C	PB33B	5	BDQ33	C	
AD14	PB34A	5	BDQ33	T	PB34A	5	BDQ33	T	
AA15	PB34B	5	BDQ33	C	PB34B	5	BDQ33	C	
AE12	PB35A	5	PCLKT5_0/BDQ33	T	PB35A	5	PCLKT5_0/BDQ33	T	
AF12	PB35B	5	PCLKC5_0/BDQ33	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB40A	4	PCLKT4_0/BDQ42	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB40B	4	PCLKC4_0/BDQ42	C	PB40B	4	PCLKC4_0/BDQ42	C	
AE13	PB41A	4	BDQ42	T	PB41A	4	BDQ42	T	
AF13	PB41B	4	BDQ42	C	PB41B	4	BDQ42	C	
AB17	PB42A	4	BDQS42	T	PB42A	4	BDQS42	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB42B	4	BDQ42	C	PB42B	4	BDQ42	C	
AE14	PB43A	4	BDQ42	T	PB43A	4	BDQ42	T	
AF14	PB43B	4	BDQ42	C	PB43B	4	BDQ42	C	
AA16	PB44A	4	BDQ42	T	PB44A	4	BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB44B	4	BDQ42	C	PB44B	4	BDQ42	C	
AC17	PB45A	4	BDQ42	T	PB45A	4	BDQ42	T	
AB16	PB45B	4	BDQ42	C	PB45B	4	BDQ42	C	
AE15	PB46A	4	BDQ42	T	PB46A	4	BDQ42	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB46B	4	BDQ42	C	PB46B	4	BDQ42	C	
AE16	PB47A	4	BDQ51	T	PB47A	4	BDQ51	T	
AF16	PB47B	4	BDQ51	C	PB47B	4	BDQ51	C	
Y16	PB48A	4	BDQ51	T	PB48A	4	BDQ51	T	
AB18	PB48B	4	BDQ51	C	PB48B	4	BDQ51	C	
AD17	PB49A	4	BDQ51	T	PB49A	4	BDQ51	T	
AD18	PB49B	4	BDQ51	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB50A	4	BDQ51	T	PB50A	4	BDQ51	T	
AD19	PB50B	4	BDQ51	C	PB50B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB51A	4	BDQS51	T	PB51A	4	BDQS51	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U1	PL53A	6	LDQ50	T	PL66A	6	LDQ63	T	
V1	PL53B	6	LDQ50	C	PL66B	6	LDQ63	C	
GND	GNDIO6	-			GNDIO6	-			
P3	PL54A	6	LDQ58	T (LVDS)*	PL67A	6	LDQ71	T (LVDS)*	
R3	PL54B	6	LDQ58	C (LVDS)*	PL67B	6	LDQ71	C (LVDS)*	
R4	PL55A	6	LDQ58	T	PL68A	6	LDQ71	T	
U2	PL55B	6	LDQ58	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
V2	PL56A	6	LDQ58	T (LVDS)*	PL69A	6	LDQ71	T (LVDS)*	
W2	PL56B	6	LDQ58	C (LVDS)*	PL69B	6	LDQ71	C (LVDS)*	
T6	PL57A	6	LDQ58	T	PL70A	6	LDQ71	T	
R5	PL57B	6	LDQ58	C	PL70B	6	LDQ71	C	
GND	GNDIO6	-			GNDIO6	-			
R6	PL58A	6	LDQS58	T (LVDS)*	PL71A	6	LDQS71	T (LVDS)*	
R7	PL58B	6	LDQ58	C (LVDS)*	PL71B	6	LDQ71	C (LVDS)*	
W1	PL59A	6	LDQ58	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y2	PL59B	6	LDQ58	C	PL72B	6	LDQ71	C	
Y1	PL60A	6	LLM0_GDLLT_IN_A**/LDQ58	T (LVDS)*	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*	
AA2	PL60B	6	LLM0_GDLLC_IN_A**/LDQ58	C (LVDS)*	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*	
T5	PL61A	6	LLM0_GDLLT_FB_A/LDQ58	T	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T	
GND	GNDIO6	-			GNDIO6	-			
T7	PL61B	6	LLM0_GDLLC_FB_D/LDQ58	C	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C	
R8	VCCPLL	6			VCCPLL	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
U3	PL63A	6	LLM0_GPLLT_IN_A**/LDQ67	T (LVDS)*	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*	
U4	PL63B	6	LLM0_GPLLC_IN_A**/LDQ67	C (LVDS)*	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*	
V3	PL64A	6	LLM0_GPLLT_FB_A/LDQ67	T	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T	
U5	PL64B	6	LLM0_GPLLC_FB_A/LDQ67	C	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C	
V4	PL65A	6	LDQ67	T (LVDS)*	PL78A	6	LDQ80	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
V5	PL65B	6	LDQ67	C (LVDS)*	PL78B	6	LDQ80	C (LVDS)*	
Y3	PL66A	6	LDQ67	T	PL79A	6	LDQ80	T	
Y4	PL66B	6	LDQ67	C	PL79B	6	LDQ80	C	
W3	PL67A	6	LDQS67	T (LVDS)*	PL80A	6	LDQS80	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
W4	PL67B	6	LDQ67	C (LVDS)*	PL80B	6	LDQ80	C (LVDS)*	
AA1	PL68A	6	LDQ67	T	PL81A	6	LDQ80	T	
AB1	PL68B	6	LDQ67	C	PL81B	6	LDQ80	C	
VCCIO	VCCIO6	6			VCCIO6	6			
U8	PL69A	6	LDQ67	T (LVDS)*	PL82A	6	LDQ80	T (LVDS)*	
U7	PL69B	6	LDQ67	C (LVDS)*	PL82B	6	LDQ80	C (LVDS)*	
V8	PL70A	6	LDQ67	T	PL83A	6	LDQ80	T	
U6	PL70B	6	LDQ67	C	PL83B	6	LDQ80	C	
GND	GNDIO6	-			GNDIO6	-			
W6	PL71A	6	LDQ75	T (LVDS)*	PL84A	6	LDQ88	T (LVDS)*	

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T	
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			
GNDIO	GNDIO1	-			GNDIO1	-			
VCCIO	VCCIO1	1			VCCIO1	1			
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
G10	VCCPLL	-			VCCPLL	-			
G7	VCC	-			VCC	-			
G9	VCC	-			VCC	-			
H7	VCC	-			VCC	-			
J10	VCC	-			VCC	-			
K10	VCC	-			VCC	-			
K8	VCC	-			VCC	-			
E7	VCCIO0	0			VCCIO0	0			
VCCIO	VCCIO0	0			VCCIO0	0			
E10	VCCIO1	1			VCCIO1	1			
VCCIO	VCCIO1	1			VCCIO1	1			
E14	VCCIO2	2			VCCIO2	2			
G12	VCCIO2	2			VCCIO2	2			
VCCIO	VCCIO2	2			VCCIO2	2			
K12	VCCIO3	3			VCCIO3	3			
M14	VCCIO3	3			VCCIO3	3			
VCCIO	VCCIO3	3			VCCIO3	3			
M10	VCCIO4	4			VCCIO4	4			
P12	VCCIO4	4			VCCIO4	4			
VCCIO	VCCIO4	4			VCCIO4	4			
M7	VCCIO5	5			VCCIO5	5			
P5	VCCIO5	5			VCCIO5	5			
VCCIO	VCCIO5	5			VCCIO5	5			
K5	VCCIO6	6			VCCIO6	6			
M3	VCCIO6	6			VCCIO6	6			
VCCIO	VCCIO6	6			VCCIO6	6			
E3	VCCIO7	7			VCCIO7	7			
G5	VCCIO7	7			VCCIO7	7			
VCCIO	VCCIO7	7			VCCIO7	7			
T15	VCCIO8	8			VCCIO8	8			
VCCIO	VCCIO8	8			VCCIO8	8			
G8	VCCAUX	-			VCCAUX	-			
H10	VCCAUX	-			VCCAUX	-			
J7	VCCAUX	-			VCCAUX	-			
K9	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A15	GND	-			GND	-			
A16	GND	-			GND	-			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G5	VCCIO7	7		
J8	VCCIO7	7		
K4	VCCIO7	7		
AA22	VCCIO8	8		
U19	VCCIO8	8		
H11	VCCAUX	-		
H12	VCCAUX	-		
L15	VCCAUX	-		
L8	VCCAUX	-		
M15	VCCAUX	-		
M8	VCCAUX	-		
R11	VCCAUX	-		
R12	VCCAUX	-		
A1	GND	-		
A10	GND	-		
A16	GND	-		
A22	GND	-		
AA19	GND	-		
AA4	GND	-		
AB1	GND	-		
AB22	GND	-		
B13	GND	-		
B19	GND	-		
B4	GND	-		
D16	GND	-		
D2	GND	-		
D21	GND	-		
D7	GND	-		
G19	GND	-		
G4	GND	-		
H10	GND	-		
H13	GND	-		
J14	GND	-		
J9	GND	-		
K10	GND	-		
K11	GND	-		
K12	GND	-		
K13	GND	-		
K15	GND	-		
K20	GND	-		
K3	GND	-		
K8	GND	-		
L10	GND	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C6	PT12B	0		C	PT12B	0		C	
F10	PT12A	0		T	PT12A	0		T	
D7	PT11B	0		C	PT11B	0		C	
H11	PT11A	0		T	PT11A	0		T	
D5	PT10B	0		C	PT10B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E6	PT10A	0		T	PT10A	0		T	
G10	PT9B	0		C	PT9B	0		C	
F9	PT9A	0		T	PT9A	0		T	
H10	PT8B	0		C	PT8B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
E7	PT8A	0		T	PT8A	0		T	
B3	PT7B	0		C	PT7B	0		C	
C5	PT7A	0		T	PT7A	0		T	
B2	PT6B	0		C	PT6B	0		C	
C4	PT6A	0		T	PT6A	0		T	
G9	PT5B	0		C	PT5B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F7	PT5A	0		T	PT5A	0		T	
C3	PT4B	0		C	PT4B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
D4	PT4A	0		T	PT4A	0		T	
J10	PT3B	0		C	PT3B	0		C	
F8	PT3A	0		T	PT3A	0		T	
G8	PT2B	0		C	PT2B	0		C	
G7	PT2A	0		T	PT2A	0		T	
L12	VCC	-			VCC	-			
L13	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L15	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N16	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P16	VCC	-			VCC	-			
R11	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R15	VCC	-			VCC	-			
R16	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T13	VCC	-			VCC	-			
T14	VCC	-			VCC	-			
T15	VCC	-			VCC	-			
B12	VCCIO0	0			VCCIO0	0			
B7	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA6	NC	-			PL79B	6	LDQ82	C	
AB4	NC	-			PL80A	6	LDQ82	T (LVDS)*	
-	-	-			VCCIO6	6			
AB5	NC	-			PL80B	6	LDQ82	C (LVDS)*	
AA8	NC	-			PL81A	6	LDQ82	T	
AA9	NC	-			PL81B	6	LDQ82	C	
AC1	PL62A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
AC2	PL62B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	
AC4	PL63A	6	LLM0_GPLLT_FB_A	T	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	
AC3	PL63B	6	LLM0_GPLLC_FB_A	C	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AC7	PL64A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	
AC6	PL64B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	
AC5	PL65A	6	LLM0_GDLLT_FB_A	T	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	
AD3	PL65B	6	LLM0_GDLLC_FB_A	C	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
AD2	PL67A	6	LDQ71	T (LVDS)*	PL87A	6		T	
AD1	PL67B	6	LDQ71	C (LVDS)*	PL87B	6		C	
AE2	TCK	-			TCK	-			
AE1	TDI	-			TDI	-			
AF2	TMS	-			TMS	-			
AF1	TDO	-			TDO	-			
AG1	VCCJ	-			VCCJ	-			
AH1	VCC	-			LLC_SQ_VCCR3	14			
AK2	PB11A	5	BDQ15	T	LLC_SQ_HDINP3	14		T	
AJ1	NC	-			LLC_SQ_VCCIB3	14			
AJ2	PB11B	5	BDQ15	C	LLC_SQ_HDINN3	14		C	
AH4	VCC	-			LLC_SQ_VCCTX3	14			
AK5	PB13A	5	BDQ15	T	LLC_SQ_HDOUTP3	14		T	
AK4	NC	-			LLC_SQ_VCCOB3	14			
AJ5	PB13B	5	BDQ15	C	LLC_SQ_HDOUTN3	14		C	
AH5	VCC	-			LLC_SQ_VCCTX2	14			
AJ6	PB14B	5	BDQ15	C	LLC_SQ_HDOUTN2	14		C	
AH6	NC	-			LLC_SQ_VCCOB2	14			
AK6	PB14A	5	BDQ15	T	LLC_SQ_HDOUTP2	14		T	
AH2	VCC	-			LLC_SQ_VCCR2	14			
AJ3	PB12B	5	BDQ15	C	LLC_SQ_HDINN2	14		C	
AH3	NC	-			LLC_SQ_VCCIB2	14			
AK3	PB12A	5	BDQ15	T	LLC_SQ_HDINP2	14		T	
AH7	VCC	-			LLC_SQ_VCCP	14			
AG7	PB15A	5	BDQS15	T	LLC_SQ_REFCLKP	14		T	
AF7	PB15B	5	BDQ15	C	LLC_SQ_REFCLKN	14		C	
AJ7	VCCAUX	-			LLC_SQ_VCCAUX33	14			
AK11	PB18A	5	BDQ15	T	LLC_SQ_HDINP1	14		T	
AH11	NC	-			LLC_SQ_VCCIB1	14			
AJ11	PB18B	5	BDQ15	C	LLC_SQ_HDINN1	14		C	

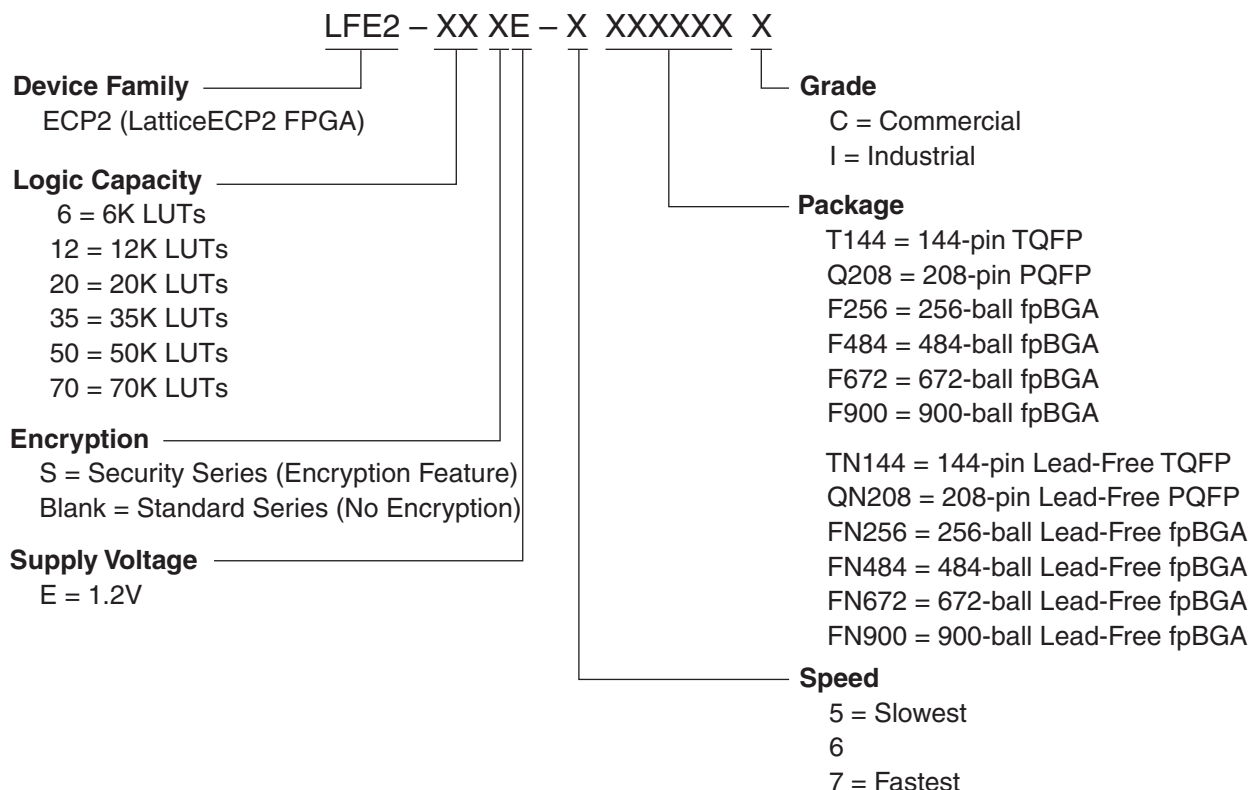
LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K3	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
N10	VCCIO7	7			VCCIO7	7			
N3	VCCIO7	7			VCCIO7	7			
P10	VCCIO7	7			VCCIO7	7			
R6	VCCIO7	7			VCCIO7	7			
AA25	VCCIO8	8			VCCIO8	8			
AD28	VCCIO8	8			VCCIO8	8			
AA10	VCCAUX	-			VCCAUX	-			
AA11	VCCAUX	-			VCCAUX	-			
AA20	VCCAUX	-			VCCAUX	-			
AA21	VCCAUX	-			VCCAUX	-			
K10	VCCAUX	-			VCCAUX	-			
K11	VCCAUX	-			VCCAUX	-			
K20	VCCAUX	-			VCCAUX	-			
K21	VCCAUX	-			VCCAUX	-			
L10	VCCAUX	-			VCCAUX	-			
L11	VCCAUX	-			VCCAUX	-			
L20	VCCAUX	-			VCCAUX	-			
L21	VCCAUX	-			VCCAUX	-			
Y10	VCCAUX	-			VCCAUX	-			
Y11	VCCAUX	-			VCCAUX	-			
Y20	VCCAUX	-			VCCAUX	-			
Y21	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A13	GND	-			GND	-			
A18	GND	-			GND	-			
A24	GND	-			GND	-			
A30	GND	-			GND	-			
A7	GND	-			GND	-			
AA14	GND	-			GND	-			
AA15	GND	-			GND	-			
AA16	GND	-			GND	-			
AA17	GND	-			GND	-			
AA24	GND	-			GND	-			
AA27	GND	-			GND	-			
AA4	GND	-			GND	-			
AB24	GND	-			GND	-			
AB7	GND	-			GND	-			
AD12	GND	-			GND	-			
AD19	GND	-			GND	-			
AD27	GND	-			GND	-			
AE22	GND	-			GND	-			
AE27	GND	-			GND	-			
AE4	GND	-			GND	-			
AE9	GND	-			GND	-			
AF14	GND	-			GND	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

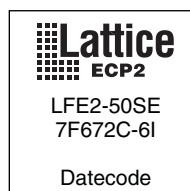
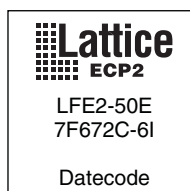
LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J2	PL34B	7	LDQ32	C (LVDS)*
H1	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-		
J1	PL35B	7	LDQ32	C
GNDIO	GNDIO7	-		
L5	PL41A	7	LDQ45	T (LVDS)*
L4	PL41B	7	LDQ45	C (LVDS)*
N9	PL42A	7	LDQ45	T
N7	PL42B	7	LDQ45	C
K2	PL43A	7	LDQ45	T (LVDS)*
K1	PL43B	7	LDQ45	C (LVDS)*
P9	PL44A	7	LDQ45	T
P7	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-		
M6	PL45A	7	LDQS45	T (LVDS)*
M5	PL45B	7	LDQ45	C (LVDS)*
N5	PL46A	7	LDQ45	T
N6	PL46B	7	LDQ45	C
M4	PL47A	7	LDQ45	T (LVDS)*
M3	PL47B	7	LDQ45	C (LVDS)*
P6	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-		
P8	PL48B	7	LDQ45	C
L3	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
L2	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
P5	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T
P4	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
L1	PL52A	7	LDQ54	T (LVDS)*
M2	PL52B	7	LDQ54	C (LVDS)*
R5	PL53A	7	LDQ54	T
R4	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-		
M1	PL54A	7	LDQS54	T (LVDS)*
N2	PL54B	7	LDQ54	C (LVDS)*
R8	PL55A	7	LDQ54	T
T9	PL55B	7	LDQ54	C
P3	PL56A	7	LDQ54	T (LVDS)*
P2	PL56B	7	LDQ54	C (LVDS)*
N1	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-		
P1	PL57B	7	PCLKC7_0/LDQ54	C
T5	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
T4	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*

LatticeECP2 Part Number Description



Ordering Information

Note: LatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152C	436	1.2V	-5	fpBGA	1152	Com	70
LFE2M70SE-6F1152C	436	1.2V	-6	fpBGA	1152	Com	70
LFE2M70SE-7F1152C	436	1.2V	-7	fpBGA	1152	Com	70
LFE2M70SE-5F900C	416	1.2V	-5	fpBGA	900	Com	70
LFE2M70SE-6F900C	416	1.2V	-6	fpBGA	900	Com	70
LFE2M70SE-7F900C	416	1.2V	-7	fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152C	520	1.2V	-5	fpBGA	1152	Com	100
LFE2M100SE-6F1152C	520	1.2V	-6	fpBGA	1152	Com	100
LFE2M100SE-7F1152C	520	1.2V	-7	fpBGA	1152	Com	100
LFE2M100SE-5F900C	416	1.2V	-5	fpBGA	900	Com	100
LFE2M100SE-6F900C	416	1.2V	-6	fpBGA	900	Com	100
LFE2M100SE-7F900C	416	1.2V	-7	fpBGA	900	Com	100

Date	Version	Section	Change Summary
August 2007 (cont.)	02.8 (cont.)	DC and Switching (cont.)	sysCLOCK GPLL timing has been updated.
		Pinout Information	Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information.
		Ordering Information	1156-fpBGA package option has been removed from the LatticeECP2M family.
September 2007	02.9	Pinout Information	Added Thermal Management text section.
February 2008	03.0	Architecture	Added LVC MOS33D description.
		DC and Switching	LatticeECP2M Supply Current has been updated.
			Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11).
			Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated.
			Table 3-8. Channel output Jitter (Max) has been updated.
		Pinout Information	Signal description has been updated.
April 2008	03.1	Pinout Information	Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100.
June 2008	03.2	Pinout Information	Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated.
		Introduction	Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
August 2008	03.3	DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
		Pinout Information	Added information for [LOC]DQ[num] to Signal Descriptions table.
January 2009	03.4	DC and Switching Characteristics	Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode.
			Added Channel Output Jitter table for x20 mode.
November 2009	03.5	DC and Switching Characteristics	Updated SPI/SPI _m Configuration Waveforms diagram.
			Updated footnotes in LatticeECP2 Initialization Supply Current table.
			Updated footnotes in LatticeECP2M Initialization Supply Current table.
			Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table.
			Updated max. value for t _{DINIT} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.
			Updated Serial Output Timing and Levels table.
			Updated Figure 3-5 MLVDS
			Updated Table 3-7 Serial Output Timing and Levels
			Updated Table 3-15 Power Down/Power Up Specification
		Pinout Information	Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5.

Date	Version	Section	Change Summary
June 2013 (cont.)	04.0 (cont.)	DC and Switching Characteristics	sysCLOCK SPLL Timing table – Corrected signal names for t_{RST} parameter.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added t_{SUMCDI} and t_{HMCDI} parameters.
September 2013	04.1	Architecture	Updated Selectable Master Clock (CCLK) Frequencies during Configuration table.
		DC and Switching Characteristics	Added information on f_{MAXSPI} parameter in LatticeECP2/M sys-CONFIG Port Timing Specifications table.