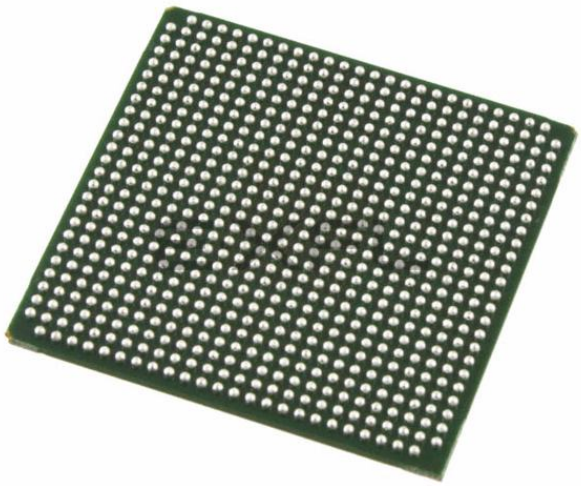
Lattice Semiconductor Corporation - LFE2-20SE-6FN672I Datasheet



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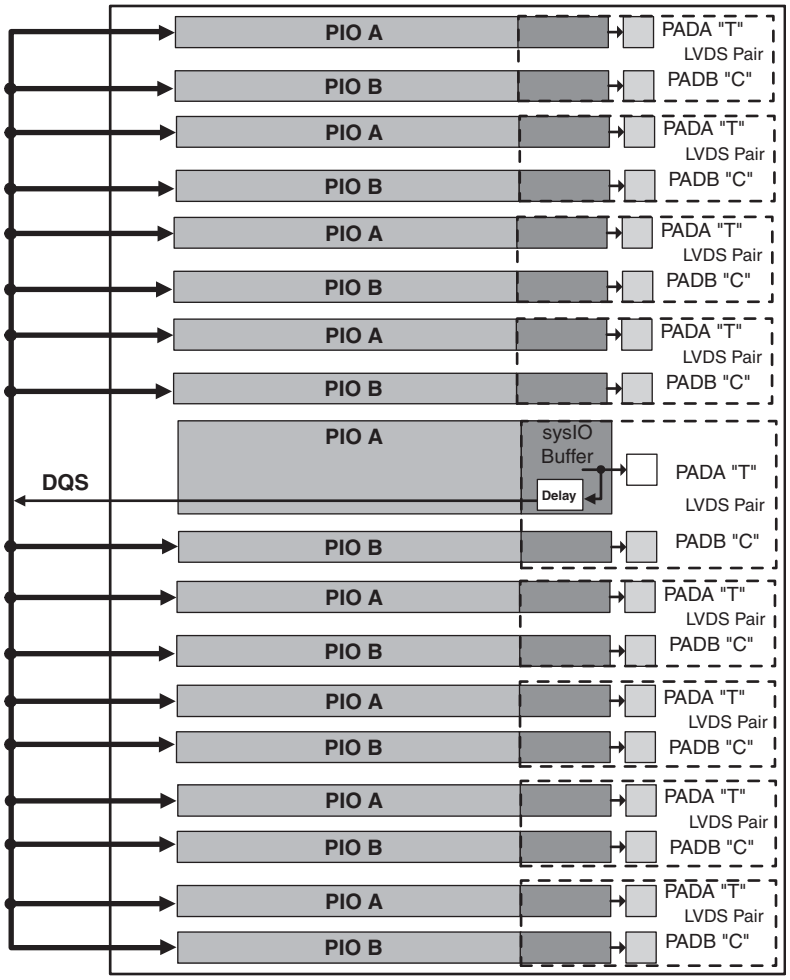
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2625
Number of Logic Elements/Cells	21000
Total RAM Bits	282624
Number of I/O	402
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-20se-6fn672i

Figure 2-34. DQS Input Routing for the Bottom Edge of the Device



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-35 and Figure 2-36 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-35. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

SERDES Power Supply Requirements (LatticeECP2M Family Only)[1]

Over Recommended Operating Conditions

Symbol	Description	Typ.[2]	Units
Standby (Power Down)			
$I_{CCTX-SB}$	V_{CCTX} current (per channel)	10	µA
$I_{CCRX-SB}$	V_{CCRX} current (per channel)	75	µA
$I_{CCIB-SB}$	Input buffer current (per channel)	0	µA
$I_{CCOB-SB}$	Output buffer current (per channel)	0	µA
I_{CCP-SB}	SERDES PLL current (per quad)	30	µA
$I_{CCAX33-SB}$	SERDES termination current (per quad)	10	µA
Operating (Data Rate = 3.125 Gbps)			
$I_{CCTX-OP}$	V_{CCTX} current (per channel)	19	mA
$I_{CCRX-OP}$	V_{CCRX} current (per channel)	34	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	13	mA
I_{CCP-OP}	SERDES PLL current (per quad)	26	mA
$I_{CCAX33-OP}$	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.
2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power[1]

Symbol	Description	Typ.[2]	Units
$P_{S-1CH-31}$	SERDES power (one channel @ 3.125 Gbps)	90	mW
$P_{S-1CH-25}$	SERDES power (one channel @ 2.5 Gbps)	87	mW
$P_{S-1CH-12}$	SERDES power (one channel @ 1.25 Gbps)	86	mW
$P_{S-1CH-02}$	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25ºC and 1.2V.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Bottom Edge of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		131	193	331	402	331	450
Differential Pair User I/O		62	96	165	200	165	224
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	42	54	60	64	60	68
	Dedicated Pins	3	3	3	3	3	3
VCC		14	7	18	24	16	22
VCCAUX		8	4	16	16	16	16
VCCPLL		0	0	0	0	2	2
VCCIO	Bank0	2	2	4	5	4	5
	Bank1	2	2	4	5	4	5
	Bank2	2	2	4	5	4	5
	Bank3	2	2	4	5	4	5
	Bank4	2	2	4	5	4	5
	Bank5	2	2	4	5	4	5
	Bank6	2	2	4	5	4	5
	Bank7	2	2	4	5	4	5
	Bank8	2	1	2	2	2	2
GND, GND0 to GND7		22	20	60	72	60	72
NC		0	1	8	101	8	102
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	18/9	18/9	50/25	67/33	50/25	67/33
	Bank1	18/9	34/17	46/23	52/26	46/23	52/26
	Bank2	11/5	20/10	34/17	36/18	34/17	48/24
	Bank3	11/5	12/6	22/11	32/16	22/11	42/21
	Bank4	19/9	32/16	46/23	50/25	46/23	54/27
	Bank5	18/9	17/8	46/23	68/34	46/23	68/34
	Bank6	18/8	26/13	40/20	48/24	40/20	58/29
	Bank7	12/6	20/10	33/16	35/17	33/16	47/23
	Bank8	6/2	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	4	5	9	9	9	12
	Bank3 (Right Edge)	3	3	5	8	5	9
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	6	7	10	12	10	13
	Bank7 (Left Edge)	5	5	8	8	8	11
	Bank8 (Right Edge)	0	0	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*
6	VCCAUX	-			VCCAUX	-		
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*
9	VCCIO7	7			VCCIO7	7		
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*
11	GND	-			GND	-		
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C
16	VCC	-			VCC	-		
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C
21	GND	-			GND	-		
22	VCC	-			VCC	-		
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C
25	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
28	PL22A	6			PL22A	6		
29	VCC	-			VCC	-		
30	GND	-			GND	-		
31	VCCIO6	6			VCCIO6	6		
32	TCK	-			TCK	-		
33	TDI	-			TDI	-		
34	TDO	-			TDO	-		
35	VCCJ	-			VCCJ	-		
36	TMS	-			TMS	-		
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
39	VCCAUX	-			VCCAUX	-		
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C
42	VCCIO5	5			VCCIO5	5		
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C
45	NC	5			PB16A	5	BDQ15	T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J13	J13	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
J12	J12	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
H12	H12	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GND	GND	GNDIO3	-		
H13	H13	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
H15	H15	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO	VCCIO3	3		
H16	H16	PR22A	3	VREF1_3/RDQ25	T
H11	H11	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J11	J11	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
G16	G16	PR19B	2	PCLKC2_0/RDQ16	C
GND	GND	GNDIO2	-		
G15	G15	PR19A	2	PCLKT2_0/RDQ16	T
F15	F15	PR17B	2	RDQ16	C
G11	G11	PR18B	2	RDQ16	C (LVDS)*
F14	F14	PR17A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
F12	F12	PR18A	2	RDQ16	T (LVDS)*
G14	G14	PR16B	2	RDQ16	C (LVDS)*
G13	G13	PR16A	2	RDQS16	T (LVDS)*
GND	GND	GNDIO2	-		
F16	F16	PR14B	2	RDQ16	C (LVDS)*
F9	F9	PR15B	2	RDQ16	C
E16	E16	PR14A	2	RDQ16	T (LVDS)*
F10	F10	PR15A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
D16	D16	PR13B	2	RDQ16	C
D15	D15	PR13A	2	RDQ16	T
C15	C15	PR6B	2	RDQ8	C (LVDS)*
C16	C16	PR7B	2	RDQ8	C
GND	GND	GNDIO2	-		
D14	D14	PR6A	2	RDQ8	T (LVDS)*
B16	B16	PR7A	2	RDQ8	T
F13	F13	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO	VCCIO2	2		
E13	E13	PR2A	2	VREF1_2	T (LVDS)*
F11	F11	PT64B	1	VREF2_1	C
E11	E11	PT64A	1	VREF1_1	T
GND	GND	GNDIO1	-		
A15	A15	PT63B	1		C
E12	E12	PT62B	1		C
B15	B15	PT63A	1		T

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
-	-	-			GNDIO7	-		
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*
F4	PL3A	7		T	PL5A	7	LDQ8	T
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*
F5	PL3B	7		C	PL5B	7	LDQ8	C
VCCIO	VCCIO7	7			VCCIO7	7		
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*
G6	PL5A	7		T	PL7A	7	LDQ8	T
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*
G7	PL5B	7		C	PL7B	7	LDQ8	C
GNDIO	GNDIO7	-			GNDIO7	-		
F1	NC	-			PL9A	7	LDQ8	T
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*
F2	NC	-			PL9B	7	LDQ8	C
-	-	-			VCCIO7	7		
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*
G1	NC	-			PL11A	7	LDQ8	T
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*
G2	NC	-			PL11B	7	LDQ8	C
-	-	-			GNDIO	-		
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T
VCCIO	VCCIO7	7			VCCIO7	7		
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO	-		
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T
VCCIO	VCCIO7	7			VCCIO7	7		
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO	-		
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*
VCCIO	VCCIO6	6			-	-		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB82A	4	VREF2_4/BDQ78	T	PB100A	4	VREF2_4/BDQ96	T
AB23	PB82B	4	VREF1_4/BDQ78	C	PB100B	4	VREF1_4/BDQ96	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR77B	8	WRITEN	C	PR90B	8	WRITEN	C
Y22	PR77A	8	CS1N	T	PR90A	8	CS1N	T
AC25	PR76B	8	CSN	C	PR89B	8	CSN	C
AB25	PR76A	8	D0/SPIFASTN	T	PR89A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR75B	8	D1	C	PR88B	8	D1	C
AC26	PR75A	8	D2	T	PR88A	8	D2	T
Y23	PR74B	8	D3	C	PR87B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR74A	8	D4	T	PR87A	8	D4	T
AA25	PR73B	8	D5	C	PR86B	8	D5	C
AB26	PR73A	8	D6	T	PR86A	8	D6	T
W23	PR72B	8	D7/SPID0	C	PR85B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR72A	8	DI/CSSPI0N	T	PR85A	8	DI/CSSPI0N	T
Y24	PR71B	8	DOUT/CSON	C	PR84B	8	DOUT/CSON	C
Y25	PR71A	8	BUSY/SISPI	T	PR84A	8	BUSY/SISPI	T
W24	PR70B	3	RDQ67	C	PR83B	3	RDQ80	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR70A	3	RDQ67	T	PR83A	3	RDQ80	T
AA26	PR69B	3	RDQ67	C (LVDS)*	PR82B	3	RDQ80	C (LVDS)*
Y26	PR69A	3	RDQ67	T (LVDS)*	PR82A	3	RDQ80	T (LVDS)*
U21	PR68B	3	RDQ67	C	PR81B	3	RDQ80	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR68A	3	RDQ67	T	PR81A	3	RDQ80	T
W25	PR67B	3	RDQ67	C (LVDS)*	PR80B	3	RDQ80	C (LVDS)*
W26	PR67A	3	RDQS67	T (LVDS)*	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR66B	3	RDQ67	C	PR79B	3	RDQ80	C
V25	PR66A	3	RDQ67	T	PR79A	3	RDQ80	T
V26	PR65B	3	RDQ67	C (LVDS)*	PR78B	3	RDQ80	C (LVDS)*
U26	PR65A	3	RDQ67	T (LVDS)*	PR78A	3	RDQ80	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR64B	3	RLM0_GPLLC_FB_A/RDQ67	C	PR77B	3	RLM0_GPLLC_FB_A/RDQ80	C
U23	PR64A	3	RLM0_GPLLT_FB_A/RDQ67	T	PR77A	3	RLM0_GPLLT_FB_A/RDQ80	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			-	-		
F16	XRES	-			XRES	-		
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M19	PR50A	3	RDQ52	T (LVDS)*
M18	PR49B	3	RDQ52	C
VCCIO	VCCIO3	3		
L16	PR49A	3	RDQ52	T
L22	PR48B	3	RDQ52	C (LVDS)*
L21	PR48A	3	RDQ52	T (LVDS)*
GNDIO	GNDIO3	-		
K22	PR46B	3	RLM3_SPLLC_FB_A	C
VCCIO	VCCIO3	3		
K21	PR46A	3	RLM3_SPLLT_FB_A	T
L17	PR45B	3	RLM3_SPLLC_IN_A	C (LVDS)*
L18	PR45A	3	RLM3_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-		
L20	PR44B	3		C
L19	PR44A	3		T
K16	PR43B	3		C (LVDS)*
K17	PR43A	3		T (LVDS)*
VCCIO	VCCIO3	3		
J16	PR42B	3	VREF2_3	C
K18	PR42A	3	VREF1_3	T
J22	PR41B	3	PCLKC3_0	C (LVDS)*
J21	PR41A	3	PCLKT3_0	T (LVDS)*
H22	PR39B	2	PCLKC2_0/RDQ36	C
H21	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-		
J17	PR38B	2	RDQ36	C (LVDS)*
J18	PR38A	2	RDQ36	T (LVDS)*
J20	PR37B	2	RDQ36	C
J19	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2		
H16	PR36B	2	RDQ36	C (LVDS)*
H17	PR36A	2	RDQS36	T (LVDS)*
G22	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-		
G21	PR35A	2	RDQ36	T
H20	PR34B	2	RDQ36	C (LVDS)*
H19	PR34A	2	RDQ36	T (LVDS)*
G16	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2		
H18	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
F22	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C (LVDS)*
F21	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T (LVDS)*
G20	PR30B	2	RDQ27	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C
VCCIO	VCCIO5	5			VCCIO5	5		
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T
GNDIO	GNDIO5	-			GNDIO5	-		
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C
-	-	-			VCCIO5	5		
-	-	-			GNDIO5	-		
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T
GNDIO	GNDIO5	-			GNDIO5	-		
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T
GNDIO	GNDIO4	-			GNDIO4	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K19	VCCIO1	1		
F28	VCCIO2	2		
J25	VCCIO2	2		
K28	VCCIO2	2		
M21	VCCIO2	2		
M24	VCCIO2	2		
N21	VCCIO2	2		
N28	VCCIO2	2		
P21	VCCIO2	2		
R25	VCCIO2	2		
AA28	VCCIO3	3		
AB25	VCCIO3	3		
AE28	VCCIO3	3		
T25	VCCIO3	3		
U21	VCCIO3	3		
V21	VCCIO3	3		
V28	VCCIO3	3		
W21	VCCIO3	3		
W24	VCCIO3	3		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AE19	VCCIO4	4		
AF22	VCCIO4	4		
AG17	VCCIO4	4		
AG25	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AE12	VCCIO5	5		
AF9	VCCIO5	5		
AG14	VCCIO5	5		
AG6	VCCIO5	5		
AA3	VCCIO6	6		
AB6	VCCIO6	6		
AE3	VCCIO6	6		
T6	VCCIO6	6		
U10	VCCIO6	6		
V10	VCCIO6	6		
V3	VCCIO6	6		
W10	VCCIO6	6		
W7	VCCIO6	6		
F3	VCCIO7	7		
J6	VCCIO7	7		
K3	VCCIO7	7		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U20	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V27	GND	-		
V4	GND	-		
W23	GND	-		
W8	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
AA26	NC	-		
AB10	NC	-		
AB11	NC	-		
AB12	NC	-		
AB13	NC	-		
AB14	NC	-		
AB15	NC	-		
AB16	NC	-		
AB17	NC	-		
AB19	NC	-		
AB20	NC	-		
AB21	NC	-		
AB9	NC	-		
AC10	NC	-		
AC11	NC	-		
AC21	NC	-		
AC22	NC	-		
AC8	NC	-		
AC9	NC	-		
AD21	NC	-		
AD22	NC	-		
AD4	NC	-		
AD5	NC	-		
AD6	NC	-		
AD7	NC	-		
AD8	NC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE12	NC	-			NC	-		
AE13	NC	-			NC	-		
AE19	NC	-			NC	-		
AE21	NC	-			NC	-		
AE22	NC	-			NC	-		
AE23	NC	-			NC	-		
AF11	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
AF24	NC	-			NC	-		
AF8	NC	-			NC	-		
AF9	NC	-			NC	-		
AG10	NC	-			NC	-		
AG11	NC	-			NC	-		
AG24	NC	-			NC	-		
AG25	NC	-			NC	-		
AG26	NC	-			NC	-		
AG3	NC	-			NC	-		
AG7	NC	-			NC	-		
AG8	NC	-			NC	-		
AG9	NC	-			NC	-		
AH10	NC	-			NC	-		
AH11	NC	-			NC	-		
AH13	NC	-			NC	-		
AH24	NC	-			NC	-		
AH25	NC	-			NC	-		
AH26	NC	-			NC	-		
AH27	NC	-			NC	-		
AH5	NC	-			NC	-		
AH6	NC	-			NC	-		
AH7	NC	-			NC	-		
AH8	NC	-			NC	-		
AH9	NC	-			NC	-		
AJ10	NC	-			NC	-		
AJ11	NC	-			NC	-		
AJ13	NC	-			NC	-		
AJ24	NC	-			NC	-		
AJ25	NC	-			NC	-		
AJ26	NC	-			NC	-		
AJ27	NC	-			NC	-		
AJ3	NC	-			NC	-		
AJ4	NC	-			NC	-		
AJ5	NC	-			NC	-		
AJ6	NC	-			NC	-		
AJ7	NC	-			NC	-		
AJ8	NC	-			NC	-		
AJ9	NC	-			NC	-		
AK10	NC	-			NC	-		
AK11	NC	-			NC	-		

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2M20SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	35
LFE2M35SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50SE-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152I	436	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-6FN1152I	436	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2/M Family Data Sheet Supplemental Information

July 2012 **Data Sheet DS1006**

For Further Information

A variety of technical notes for the LatticeECP2/M family are available on the Lattice web site at www.latticesemi.com.

- TN1102, LatticeECP2/M sysIO Usage Guide
- TN1103, LatticeECP2/M sysCLOCK PLL Design and Usage Guide
- TN1104, LatticeECP2/M Memory Usage Guide
- TN1105, LatticeECP2/M High-Speed I/O Interface
- TN1106, Power Estimation and Management for LatticeECP2/M Devices
- TN1107, LatticeECP2/M sysDSP Usage Guide
- TN1108, LatticeECP2/M sysCONFIG Usage Guide
- TN1109, LatticeECP2/M Configuration Encryption Usage Guide
- TN1113, LatticeECP2/M Soft Error Detection (SED) Usage Guide
- TN1124, LatticeECP2M SERDES/PCS Usage Guide
- TN1162, LatticeECP2/M Hardware Checklist

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com