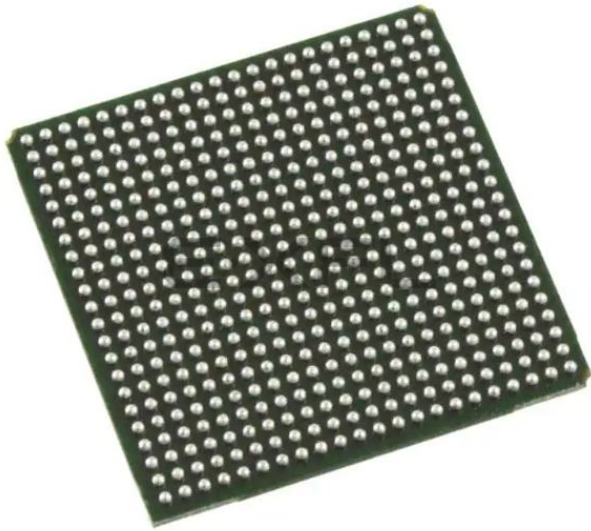




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

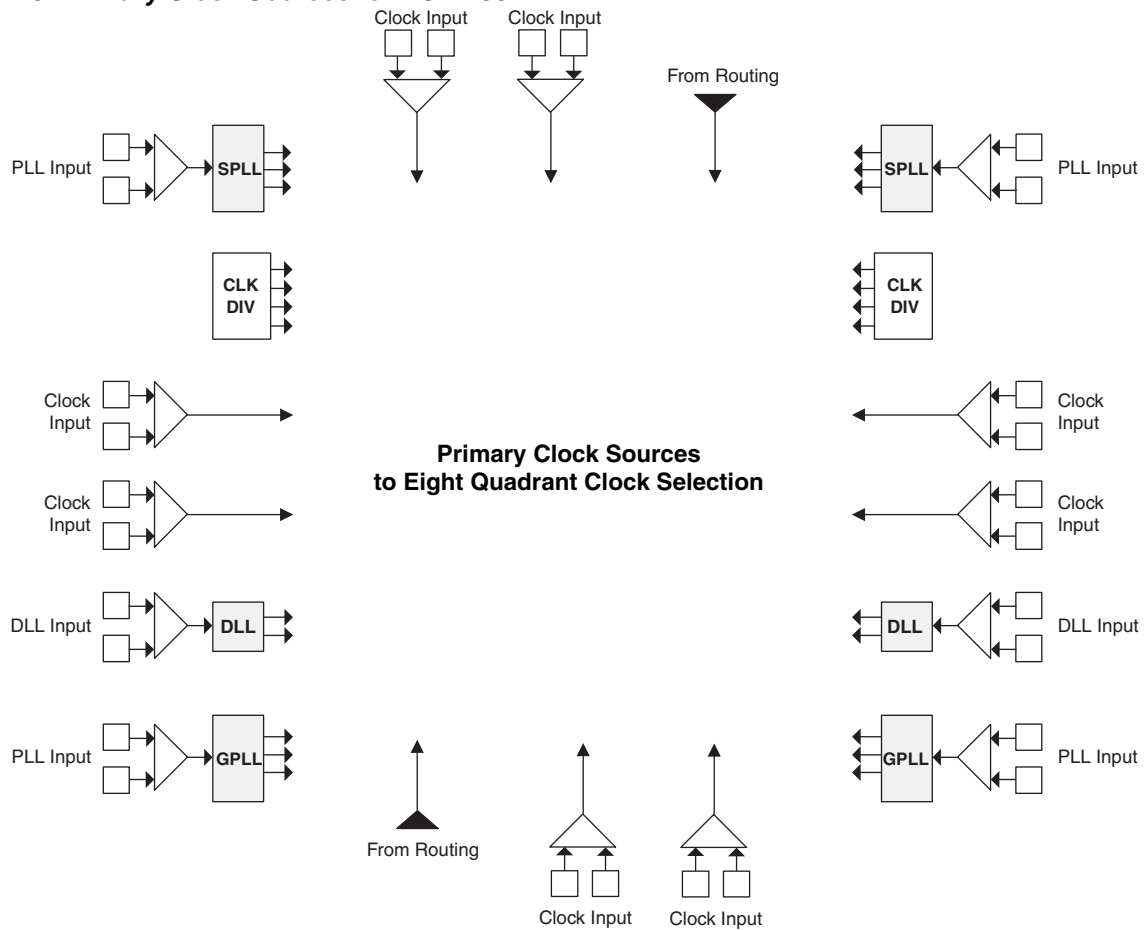
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

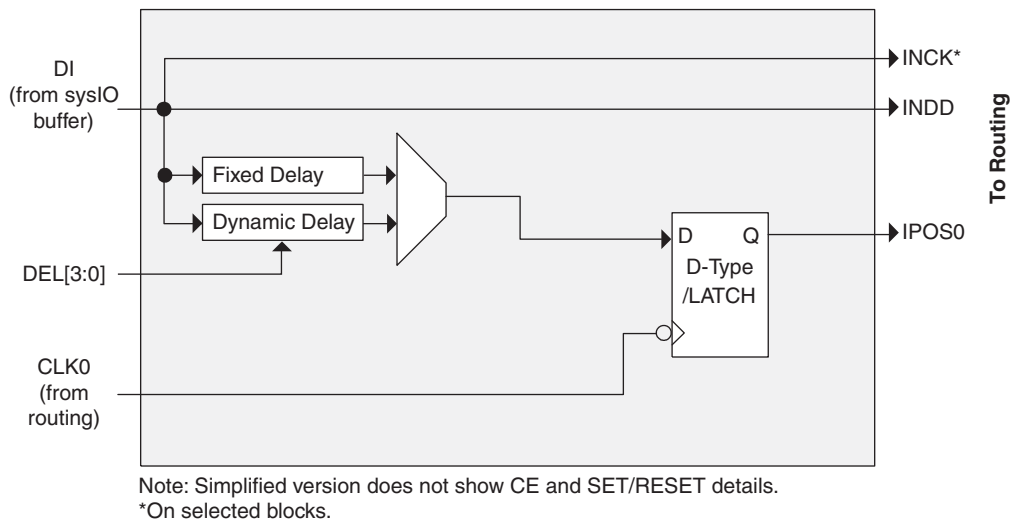
Product Status	Active
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	331
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35e-5fn484i

Figure 2-10. Primary Clock Sources for ECP2-50



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Figure 2-30. Input Register Block Top Edge



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the PIOs on the left, right and bottom contain a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-31 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-32 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining the output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams: ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-32 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
36x36 Multiplier (All Registers)	372	MHz
18x18 Multiplier/Accumulate (Input and Output Registers)	295	MHz
18x18 Multiplier-Add/Sub-Sum (All Reg- isters)	420	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	304	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	227	MHz
8x8 Matrix Multiplier	223	MHz

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUE}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _{HE}	Clock to Data Hold - PIO Input Register	LFE2-6	0.90	—	1.10	—	1.30	—	ns
		LFE2-12	0.90	—	1.10	—	1.30	—	ns
		LFE2-20	0.90	—	1.10	—	1.30	—	ns
		LFE2-35	0.90	—	1.10	—	1.30	—	ns
		LFE2-50	0.90	—	1.10	—	1.30	—	ns
		LFE2-70	0.90	—	1.10	—	1.30	—	ns
		LFE2M20	0.90	—	1.10	—	1.30	—	ns
		LFE2M35	0.90	—	1.10	—	1.30	—	ns
		LFE2M50	1.20	—	1.40	—	1.60	—	ns
		LFE2M70	1.20	—	1.40	—	1.60	—	ns
		LFE2M100	1.20	—	1.40	—	1.60	—	ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.00	—	1.30	—	1.60	—	ns
		LFE2-12	1.00	—	1.30	—	1.60	—	ns
		LFE2-20	1.00	—	1.30	—	1.60	—	ns
		LFE2-35	1.00	—	1.30	—	1.60	—	ns
		LFE2-50	1.00	—	1.30	—	1.60	—	ns
		LFE2-70	1.00	—	1.30	—	1.60	—	ns
		LFE2M20	1.20	—	1.60	—	1.90	—	ns
		LFE2M35	1.20	—	1.60	—	1.90	—	ns
		LFE2M50	1.20	—	1.60	—	1.90	—	ns
		LFE2M70	1.20	—	1.60	—	1.90	—	ns
		LFE2M100	1.20	—	1.60	—	1.90	—	ns

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
136	PT6B	0		C	PT16B	0		C
137	PT6A	0		T	PT16A	0		T
138	GND	-			GND	-		
139	VCCIO0	0			VCCIO0	0		
140	PT4B	0		C	PT6B	0		C
141	PT4A	0		T	PT6A	0		T
142	VCCAUX	-			VCCAUX	-		
143	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
144	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one-to-one connection with a package ball or pin.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*	PR44B	3	RLM0_GPLL_C_IN_A**/RDQ48	C (LVDS)*	
U25	PR30A	3	RLM0_GPLL_T_IN_A**/RDQ34	T (LVDS)*	PR44A	3	RLM0_GPLL_T_IN_A**/RDQ48	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCC	3			VCCPLL	3			
T19	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C	PR42B	3	RLM0_GDLLC_FB_A/RDQ39	C	
U20	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T	PR42A	3	RLM0_GDLLT_FB_A/RDQ39	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*	PR41B	3	RLM0_GDLLC_IN_A**/RDQ39	C (LVDS)*	
T26	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*	PR41A	3	RLM0_GDLLT_IN_A**/RDQ39	T (LVDS)*	
T20	PR26B	3	RDQ25	C	PR40B	3	RDQ39	C	
T22	PR26A	3	RDQ25	T	PR40A	3	RDQ39	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR25B	3	RDQ25	C (LVDS)*	PR39B	3	RDQ39	C (LVDS)*	
R25	PR25A	3	RDQS25***	T (LVDS)*	PR39A	3	RDQS39***	T (LVDS)*	
R22	NC	-			PR38B	3	RDQ39	C	
GND	GNDIO3	-			GNDIO3	-			
T21	NC	-			PR38A	3	RDQ39	T	
P26	NC	-			NC	-			
P25	NC	-			NC	-			
R24	NC	-			NC	-			
VCCIO	VCCIO3	3			VCCIO3	3			
R23	NC	-			NC	-			
P20	NC	-			NC	-			
R19	NC	-			NC	-			
P21	NC	-			PR34B	3	RDQ31	C	
GND	GNDIO3	-			GNDIO3	-			
P19	NC	-			PR34A	3	RDQ31	T	
P23	NC	-			PR33B	3	RDQ31	C (LVDS)*	
P22	NC	-			PR33A	3	RDQ31	T (LVDS)*	
N22	NC	-			PR32B	3	RDQ31	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	NC	-			PR32A	3	RDQ31	T	
N26	NC	-			PR31B	3	RDQ31	C (LVDS)*	
N25	NC	-			PR31A	3	RDQS31	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR24B	3	RDQ25	C	PR30B	3	RDQ31	C	
N20	PR24A	3	RDQ25	T	PR30A	3	RDQ31	T	
M26	PR23B	3	RDQ25	C (LVDS)*	PR29B	3	RDQ31	C (LVDS)*	
M25	PR23A	3	RDQ25	T (LVDS)*	PR29A	3	RDQ31	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR22B	3	VREF2_3/RDQ25	C	PR28B	3	VREF2_3/RDQ31	C	
N21	PR22A	3	VREF1_3/RDQ25	T	PR28A	3	VREF1_3/RDQ31	T	
L26	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	
L25	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	
N24	PR19B	2	PCLKC2_0/RDQ16	C	PR25B	2	PCLKC2_0/RDQ22	C	
M23	PR19A	2	PCLKT2_0/RDQ16	T	PR25A	2	PCLKT2_0/RDQ22	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K28	PR25A	2	RDQ29	T (LVDS)*
J24	PR24B	2	RDQ21	C
J26	PR24A	2	RDQ21	T
GND	GNDIO2	-		
K29	PR23B	2	RDQ21	C (LVDS)*
K30	PR23A	2	RDQ21	T (LVDS)*
J23	PR22B	2	RDQ21	C
J25	PR22A	2	RDQ21	T
VCCIO	VCCIO2	99		
J27	PR21B	2	RDQ21	C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2	RDQ21	C
GND	GNDIO2	-		
H24	PR20A	2	RDQ21	T
J29	PR19B	2	RDQ21	C (LVDS)*
J30	PR19A	2	RDQ21	T (LVDS)*
H25	PR18B	2	RDQ21	C
VCCIO	VCCIO2	2		
H23	PR18A	2	RDQ21	T
G27	PR15B	2	RUM1_SPLLC_FB_A/RDQ12	C
GND	GNDIO2	-		
H27	PR15A	2	RUM1_SPLLT_FB_A/RDQ12	T
G29	PR14B	2	RUM1_SPLLC_IN_A/RDQ12	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A/RDQ12	T (LVDS)*
VCCIO	VCCIO2	2		
GND	GNDIO2	-		
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
VCCIO	VCCIO2	2		
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO2	-		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
VCCIO	VCCIO2	2		
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO1	-		
C25	PT99B	1		C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
F20	PR30A	2	RDQ27	T
GNDIO	GNDIO2	-		
G17	PR29B	2	RDQ27	C (LVDS)*
F17	PR29A	2	RDQ27	T (LVDS)*
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E22	PR14B	2		C
D22	PR14A	2		T
VCCIO	VCCIO2	-		
E20	PR13B	2		C (LVDS)*
D20	PR13A	2		T (LVDS)*
D19	PR12B	2	RUM0_SPLLC_FB_A	C
GNDIO	GNDIO2	-		
E19	PR12A	2	RUM0_SPLLT_FB_A	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*
VCCIO	VCCIO2	-		
E18	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-		
D18	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
F16	XRES	-		
C22	URC_SQ_VCCR0	12		
A21	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCR1	12		
B20	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C15	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B15	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C14	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A18	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C18	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B18	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C17	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B17	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A16	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A17	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T	
C16	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B14	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B13	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A14	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C13	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			
-	-	-			GNDIO1	-			
-	-	-			VCCIO1	1			
E17	PT46B	1		C	PT55B	1		C	
D17	PT46A	1		T	PT55A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
F17	PT45B	1		C	PT54B	1		C	
D16	PT45A	1		T	PT54A	1		T	
F19	PT44B	1		C	PT53B	1		C	
F18	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
E16	PT43B	1		C	PT52B	1		C	
D15	PT43A	1		T	PT52A	1		T	
G18	PT42B	1		C	PT51B	1		C	
E15	PT42A	1		T	PT51A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
G17	PT41B	1		C	PT50B	1		C	
E14	PT41A	1		T	PT50A	1		T	
D14	PT40B	1		C	PT49B	1		C	
D13	PT40A	1		T	PT49A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
F15	PT39B	1	VREF2_1	C	PT48B	1	VREF2_1	C	
E12	PT39A	1	VREF1_1	T	PT48A	1	VREF1_1	T	
H17	PT38B	1	PCLKC1_0	C	PT47B	1	PCLKC1_0	C	
E13	PT38A	1	PCLKT1_0	T	PT47A	1	PCLKT1_0	T	
C12	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
G15	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T	
C11	PT36B	0	VREF2_0	C	PT45B	0	VREF2_0	C	
F14	PT36A	0	VREF1_0	T	PT45A	0	VREF1_0	T	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F11	VCCIO0	0			VCCIO0	0			
J13	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	1			
D18	VCCIO1	1			VCCIO1	1			
F16	VCCIO1	1			VCCIO1	1			
J14	VCCIO1	1			VCCIO1	1			
K15	VCCIO1	1			VCCIO1	1			
G25	VCCIO2	2			VCCIO2	2			
L21	VCCIO2	2			VCCIO2	2			
M17	VCCIO2	2			VCCIO2	2			
M25	VCCIO2	2			VCCIO2	2			
N18	VCCIO2	2			VCCIO2	2			
P18	VCCIO3	3			VCCIO3	3			
R17	VCCIO3	3			VCCIO3	3			
R25	VCCIO3	3			VCCIO3	3			
T21	VCCIO3	3			VCCIO3	3			
Y25	VCCIO3	3			VCCIO3	3			
AA16	VCCIO4	4			VCCIO4	4			
AC18	VCCIO4	4			VCCIO4	4			
U15	VCCIO4	4			VCCIO4	4			
V14	VCCIO4	4			VCCIO4	4			
AA11	VCCIO5	5			VCCIO5	5			
V13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AE7	VCCIO5	5			VCCIO5	5			
U12	VCCIO5	5			VCCIO5	5			
P9	VCCIO6	6			VCCIO6	6			
R10	VCCIO6	6			VCCIO6	6			
R2	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
Y2	VCCIO6	6			VCCIO6	6			
G2	VCCIO7	7			VCCIO7	7			
L6	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M2	VCCIO7	7			VCCIO7	7			
N9	VCCIO7	7			VCCIO7	7			
AC24	VCCIO8	8			VCCIO8	8			
U17	VCCIO8	8			VCCIO8	8			
J11	VCCAUX	-			VCCAUX	-			
J12	VCCAUX	-			VCCAUX	-			
J15	VCCAUX	-			VCCAUX	-			
J16	VCCAUX	-			VCCAUX	-			
L18	VCCAUX	-			VCCAUX	-			
L9	VCCAUX	-			VCCAUX	-			
M18	VCCAUX	-			VCCAUX	-			
M9	VCCAUX	-			VCCAUX	-			
R18	VCCAUX	-			VCCAUX	-			
R9	VCCAUX	-			VCCAUX	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AH25	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13			
AJ25	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C	
AH26	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13			
AJ26	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C	
AK27	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13			
AK26	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T	
AH27	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13			
AJ29	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C	
AJ30	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13			
AK29	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T	
AH30	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13			
AG27	CFG2	8			CFG2	8			
AD25	CFG1	8			CFG1	8			
AG28	CFG0	8			CFG0	8			
AG30	PROGRAMN	8			PROGRAMN	8			
AG29	CCLK	8			CCLK	8			
AC24	INITN	8			INITN	8			
AF27	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
AF28	WRITEN***	8			WRITEN***	8			
AE26	CS1N***	8			CS1N***	8			
AB23	CSN***	8			CSN***	8			
AF29	D0/SPIFASTN***	8			D0/SPIFASTN***	8			
VCCIO	VCCIO8	8			VCCIO8	8			
AF30	D1***	8			D1***	8			
AD26	D2***	8			D2***	8			
AE29	D3***	8			D3***	8			
GNDIO	GNDIO8	-			GNDIO8	-			
AE30	D4***	8			D4***	8			
AD29	D5***	8			D5***	8			
AC25	D6***	8			D6***	8			
AD30	D7/SPID0***	8			D7/SPID0***	8			
VCCIO	VCCIO8	8			VCCIO8	8			
AA22	DI/CSSPI0N***	8			DI/CSSPI0N***	8			
AC26	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8			
AA23	BUSY/SISPI***	8			BUSY/SISPI***	8			
AB22	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
AC27	PR65B	3	RLM0_GDLLC_FB_A	C	PR85B	3	RLM0_GDLLC_FB_A/RDQ82	C	
GNDIO	GNDIO3	-			GNDIO3	-			
AC28	PR65A	3	RLM0_GDLLT_FB_A	T	PR85A	3	RLM0_GDLLT_FB_A/RDQ82	T	
AC29	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR84B	3	RLM0_GDLLC_IN_A**/RDQ82	C (LVDS)*	
AC30	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR84A	3	RLM0_GDLLT_IN_A**/RDQ82	T (LVDS)*	
AB30	PR63B	3	RLM0_GPLL_C_IN_A**	C	PR83B	3	RLM0_GPLL_C_IN_A**/RDQ82	C	
VCCIO	VCCIO3	3			VCCIO3	3			
AA30	PR63A	3	RLM0_GPLLT_IN_A**	T	PR83A	3	RLM0_GPLLT_IN_A**/RDQ82	T	
AB29	PR62B	3	RLM0_GPLL_C_FB_A	C (LVDS)*	PR82B	3	RLM0_GPLL_C_FB_A/RDQ82	C (LVDS)*	
AB28	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR82A	3	RLM0_GPLLT_FB_A/RDQ82	T (LVDS)*	
GNDIO	GNDIO3	-			GNDIO3	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			VCCIO2	2			
H23	NC	-			PR15B	2	RDQ15	C (LVDS)*	
H24	NC	-			PR15A	2	RDQS15	T (LVDS)*	
D28	NC	-			PR14B	2	RDQ15	C	
-	-	-			GNDIO2	-			
E28	NC	-			PR14A	2	RDQ15	T	
G24	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
H25	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
D27	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
GNDIO	GNDIO2	-			VCCIO2	2			
E27	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	
G25	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
F24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
VCCIO	VCCIO2	-			-	-			
GNDIO	GNDIO2	-			GNDIO2	-			
F25	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G23	XRES	-			XRES	1			
C30	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A29	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B30	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B29	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C27	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A26	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A27	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B26	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C26	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B25	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C25	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A25	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C29	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B28	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C28	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A28	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B24	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E24	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D24	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C24	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A20	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	
C20	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B20	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C19	URC_SQ_VCCR_X2	12			URC_SQ_VCCR_X2	12			
A23	URC_SQ_HDOUT_P2	12		T	URC_SQ_HDOUT_P2	12		T	
C23	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B23	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C22	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B22	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M2	PL26A	7	LDQ28	T (LVDS)*	PL30A	7	LDQ32	T (LVDS)*
M1	PL26B	7	LDQ28	C (LVDS)*	PL30B	7	LDQ32	C (LVDS)*
L6	PL27A	7	LDQ28	T	PL31A	7	LDQ32	T
L5	PL27B	7	LDQ28	C	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-			GNDIO7	-		
L3	PL28A	7	LDQS28	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*
L4	PL28B	7	LDQ28	C (LVDS)*	PL32B	7	LDQ32	C (LVDS)*
M3	PL29A	7	LDQ28	T	PL33A	7	LDQ32	T
VCCIO	VCCIO7	7			VCCIO7	7		
M4	PL29B	7	LDQ28	C	PL33B	7	LDQ32	C
N1	PL30A	7	LDQ28	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*
N2	PL30B	7	LDQ28	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*
M5	PL31A	7	LDQ28	T	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
N6	PL31B	7	LDQ28	C	PL35B	7	LDQ32	C
P3	NC	-			PL37A	7		T (LVDS)*
-	-	-			GNDIO7	-		
P4	NC	-			PL37B	7		C (LVDS)*
P9	NC	-			PL38A	7		T
M7	NC	-			PL38B	7		C
-	-	-			VCCIO7	7		
P1	NC	-			PL39A	7		T (LVDS)*
P2	NC	-			PL39B	7		C (LVDS)*
N7	NC	-			PL40A	7		T
P7	NC	-			PL40B	7		C
-	-	-			GNDIO7	-		
P5	PL33A	7	LDQ37	T (LVDS)*	PL41A	7	LDQ45	T (LVDS)*
N5	PL33B	7	LDQ37	C (LVDS)*	PL41B	7	LDQ45	C (LVDS)*
P8	PL34A	7	LDQ37	T	PL42A	7	LDQ45	T
P6	PL34B	7	LDQ37	C	PL42B	7	LDQ45	C
VCCIO	VCCIO7	7			VCCIO7	7		
R3	PL35A	7	LDQ37	T (LVDS)*	PL43A	7	LDQ45	T (LVDS)*
R4	PL35B	7	LDQ37	C (LVDS)*	PL43B	7	LDQ45	C (LVDS)*
R10	PL36A	7	LDQ37	T	PL44A	7	LDQ45	T
P11	PL36B	7	LDQ37	C	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-			GNDIO7	-		
R7	PL37A	7	LDQS37	T (LVDS)*	PL45A	7	LDQS45	T (LVDS)*
R8	PL37B	7	LDQ37	C (LVDS)*	PL45B	7	LDQ45	C (LVDS)*
R5	PL38A	7	LDQ37	T	PL46A	7	LDQ45	T
VCCIO	VCCIO7	7			VCCIO7	7		
T5	PL38B	7	LDQ37	C	PL46B	7	LDQ45	C
R1	PL39A	7	LDQ37	T (LVDS)*	PL47A	7	LDQ45	T (LVDS)*
R2	PL39B	7	LDQ37	C (LVDS)*	PL47B	7	LDQ45	C (LVDS)*
R11	PL40A	7	LDQ37	T	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-			GNDIO7	-		
T10	PL40B	7	LDQ37	C	PL48B	7	LDQ45	C
T1	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
T2	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
U10	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U22	GND	-			GND	-		
U23	GND	-			GND	-		
V12	GND	-			GND	-		
V13	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V18	GND	-			GND	-		
V19	GND	-			GND	-		
V20	GND	-			GND	-		
V22	GND	-			GND	-		
V23	GND	-			GND	-		
W12	GND	-			GND	-		
W13	GND	-			GND	-		
W15	GND	-			GND	-		
W16	GND	-			GND	-		
W17	GND	-			GND	-		
W18	GND	-			GND	-		
W19	GND	-			GND	-		
W20	GND	-			GND	-		
W22	GND	-			GND	-		
W23	GND	-			GND	-		
W26	GND	-			GND	-		
W31	GND	-			GND	-		
W4	GND	-			GND	-		
W9	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
Y18	GND	-			GND	-		
Y19	GND	-			GND	-		
A11	NC	-			NC	-		
A12	NC	-			NC	-		
A23	NC	-			NC	-		
A24	NC	-			NC	-		
AA11	NC	-			NC	-		
AB11	NC	-			NC	-		
AC26	NC	-			NC	-		
AC30	NC	-			NC	-		
AD11	NC	-			NC	-		
AD12	NC	-			NC	-		
AD13	NC	-			NC	-		
AD14	NC	-			NC	-		
AD15	NC	-			NC	-		
AD19	NC	-			NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD23	NC	-			NC	-		
AE10	NC	-			NC	-		
AE11	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2-35SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2-35SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2-35SE-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2-35SE-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2-35SE-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2-50SE-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2-50SE-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	Com	50
LFE2-50SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2-50SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2-50SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	70
LFE2-70SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	70
LFE2-70SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	70
LFE2-70SE-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2-70SE-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2-70SE-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	Ind	6
LFE2-6SE-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	Ind	6
LFE2-6SE-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	Ind	6
LFE2-6SE-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	Ind	12
LFE2-12SE-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	Ind	12
LFE2-12SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	12
LFE2-12SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	12
LFE2-12SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	Ind	12
LFE2-12SE-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	Ind	12