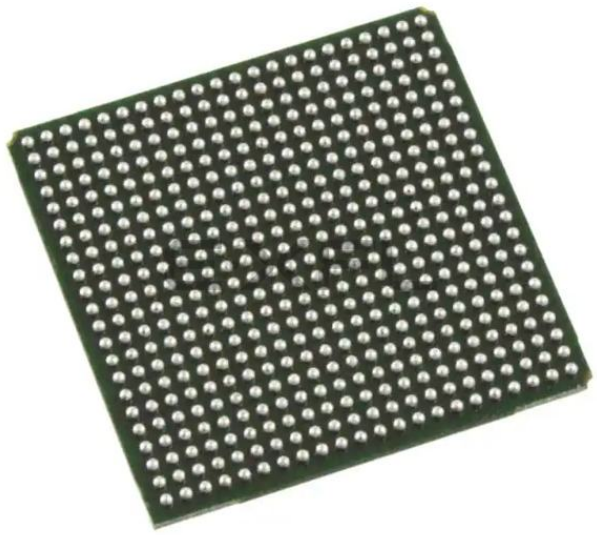

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4000 |
| Number of Logic Elements/Cells | 32000 |
| Total RAM Bits | 339968 |
| Number of I/O | 331 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35e-6fn484i |

*Table 1-2. LatticeECP2M (Including "S-Series") Family Selection*

| Device | ECP2M20 | ECP2M35 | ECP2M50 | ECP2M70 | ECP2M100 |
|---|---|---|---|---|---|
| LUTs (K) | 19 | 34 | 48 | 67 | 95 |
| sysMEM Blocks (18kb) | 66 | 114 | 225 | 246 | 288 |
| Embedded Memory (Kbits) | 1217 | 2101 | 4147 | 4534 | 5308 |
| Distributed Memory (Kbits) | 41 | 71 | 101 | 145 | 202 |
| sysDSP Blocks | 6 | 8 | 22 | 24 | 42 |
| 18x18 Multipliers | 24 | 32 | 88 | 96 | 168 |
| GPLL+SPLL+DLL | 2+6+2 | 2+6+2 | 2+6+2 | 2+6+2 | 2+6+2 |
| Maximum Available I/O | 304 | 410 | 410 | 436 | 520 |
| **Packages and SERDES / I/O Combinations** | | | | | |
| 256-ball fpBGA (17 x 17 mm) | 4 / 140 | 4 / 140 | | | |
| 484-ball fpBGA (23 x 23 mm) | 4 / 304 | 4 / 303 | 4 / 270 | | |
| 672-ball fpBGA (27 x 27 mm) | | 4 / 410 | 8 / 372 | | |
| 900-ball fpBGA (31 x 31 mm) | | | 8 / 410 | 16 / 416 | 16 / 416 |
| 1152-ball fpBGA (35 x 35 mm) | | | | 16 / 436 | 16 / 520 |

## Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

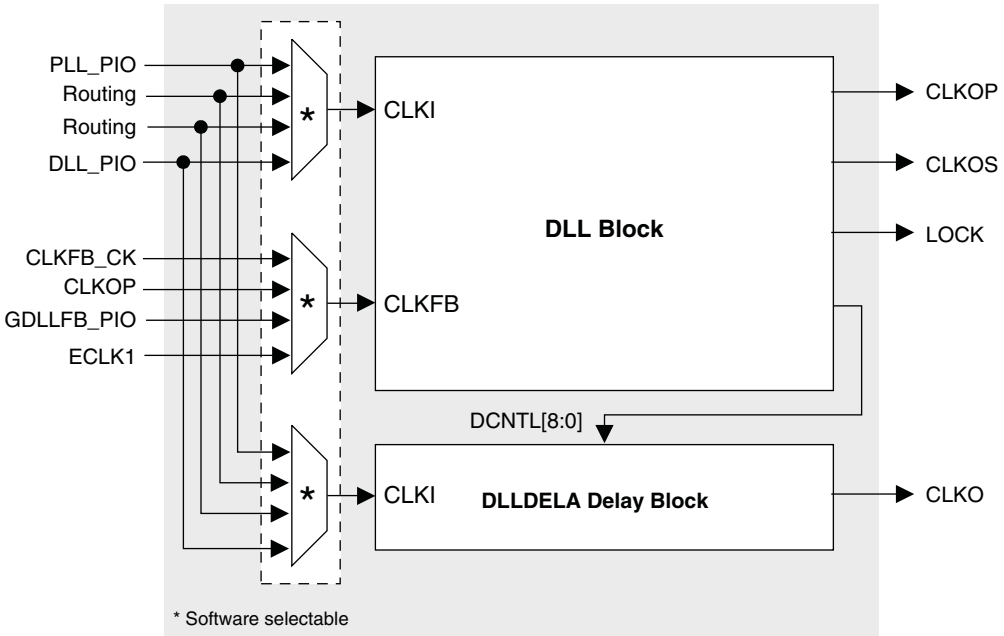
*Table 2-5. DLL Signals*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | DLL feed input from DLL output, clock net, routing or external pin |
| RSTN | I | Active low synchronous reset |
| ALUHOLD | I | Active high freezes the ALU |
| UDDCNTL | I | Synchronous enable signal (hold high for two cycles) from routing |
| DCNTL[8:0] | O | Encoded digital control signals for PIC INDEL and slave delay calibration |
| CLKOP | O | The primary clock output |
| CLKOS | O | The secondary clock output with fine phase shift and/or division by 2 or by 4 |
| LOCK | O | Active high phase lock indicator |

## DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

*Figure 2-7. DLLDELA Delay Block*




## PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

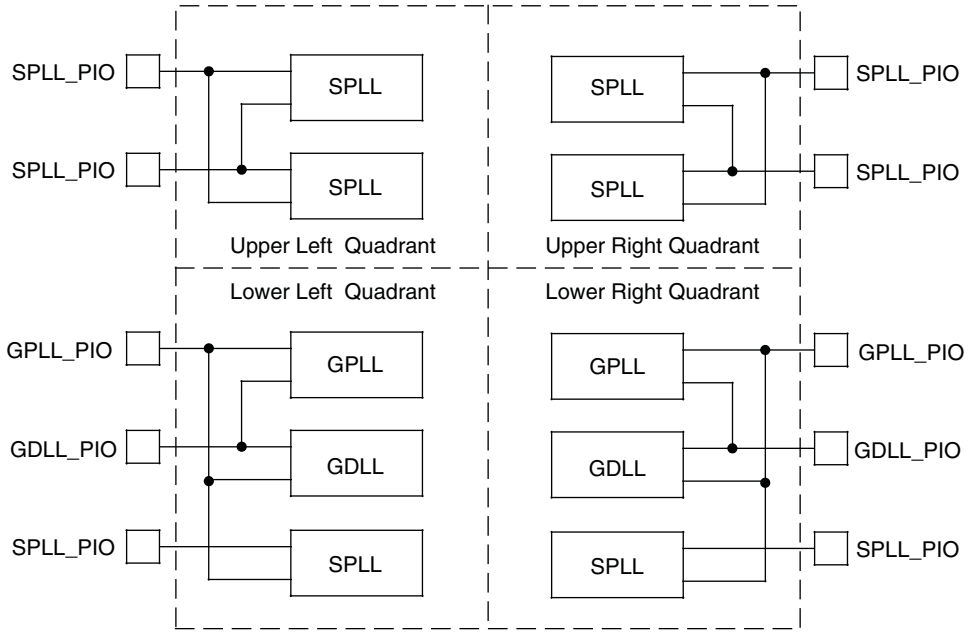
The DLLs in the LatticeECP2/M are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

## GPLL/SPLL/GDLL PIO Input Pin Connections (LatticeECP2M Family Only)

All LatticeECP2M devices contain two GDLLs, two GPLLs and six SPLLs, arranged in quadrants as shown in Figure 2-8. In the LatticeECP2M devices GPLLs, SPLLs and GDLLs share their input pins. Figure 2-8 shows the sharing of SPLLs input pin connections in the upper two quadrants and the sharing of GDLL, GPLL and SPLL input pin connections in the lower two quadrants.

***Figure 2-8. Sharing of PIO Pins by GPLL, SPLL and GDLL in LatticeECP2M Devices***



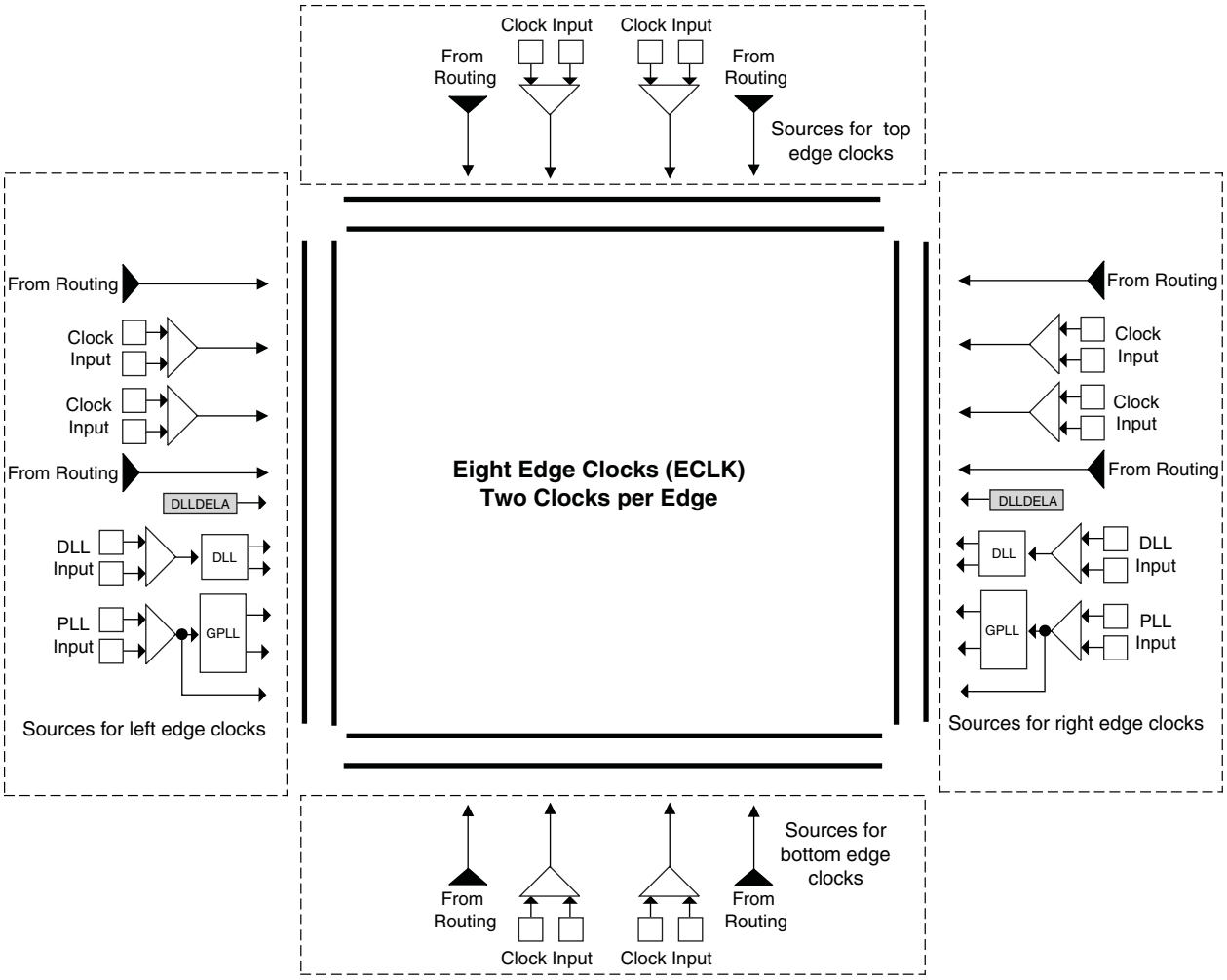

## Clock Dividers

LatticeECP2/M devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL-DELA delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information about clock dividers, please see the list of additional technical documentation at the end of this data sheet. Figure 2-9 shows the clock divider connections.

## Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

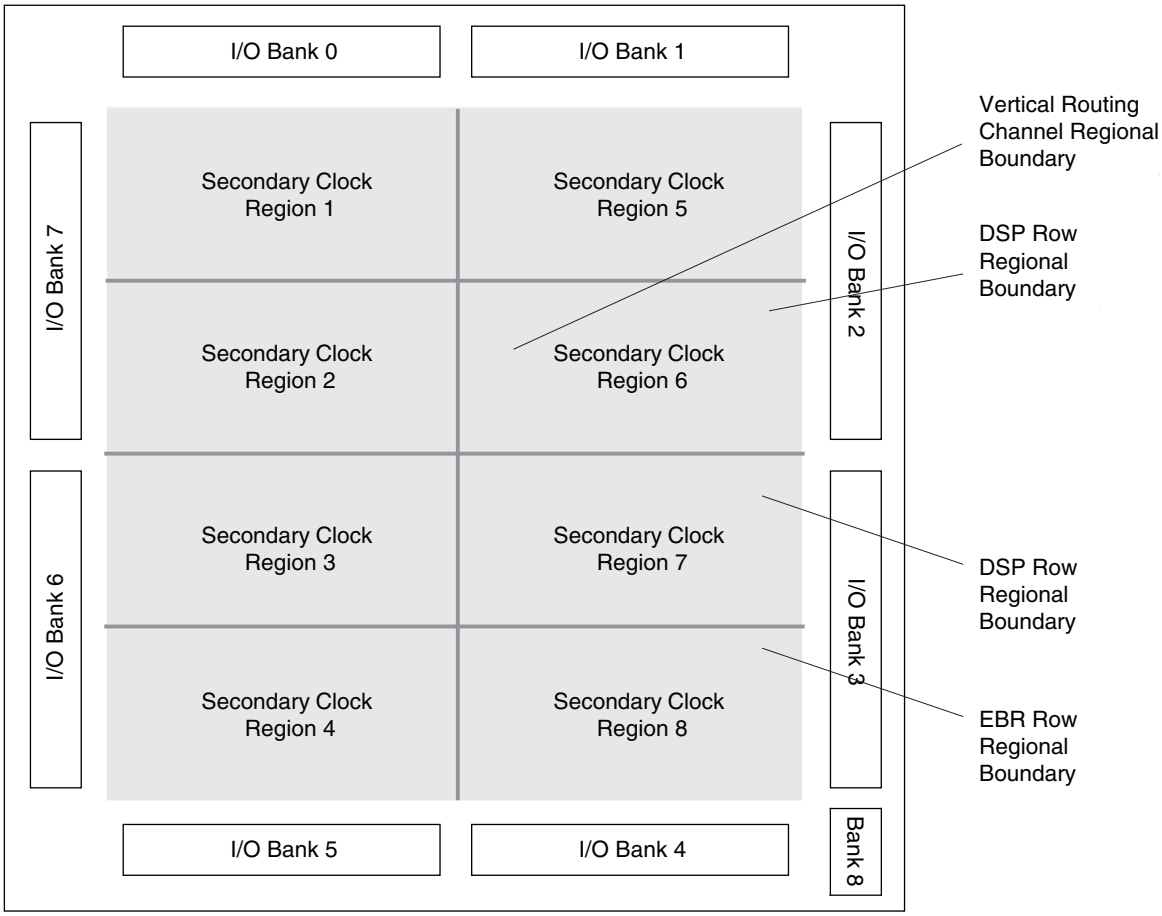
***Figure 2-12. Edge Clock Sources***



this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distrubed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

***Figure 2-15. Secondary Clock Regions ECP2-50***



## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| [LOC]DQS[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number. |
| [LOC]DQ[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number. |
| **Test and Programming (Dedicated Pins)** | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |
| TDO | O | Output pin. Test Data Out pin used to shift data out of a device using 1149.1. |
| VCCJ | — | Power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (Used During sysCONFIG) | | |
| CFG[2:0] | I | Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY/SISPI | I/O | Read control command in SPI or SPIm mode. |
| CSN | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| CS1N | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| WRITEN | I | Write Data on Parallel port (active low). |
| D[0]/SPIFASTN | I/O | sysCONFIG Port Data I/O for Parallel mode.<br>sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. |
| D[1:6] | I/O | sysCONFIG Port Data I/O for Parallel |
| D[7]/SPID0 | I/O | sysCONFIG Port Data I/O for Parallel, SPI, SPIm |
| DOUT/CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. |
| DI/CSSPI0N | I/O | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes. |
| **Dedicated SERDES Signals**[1, 2, 3] | | |
| [LOC]_SQ_VCCAUX33 | — | Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused. |
| [LOC]_SQ_REFCLKN | I | Negative Reference Clock Input |
| [LOC]_SQ_REFCLKP | I | Positive Reference Clock Input |
| [LOC]_SQ_VCCP | — | PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused. |

## LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

| Pin Type | | LFE2-50 | | LFE2-70 | |
|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 672 fpBGA | 900 fpBGA |
| Single Ended User I/O | | 339 | 500 | 500 | 583 |
| Differential Pair User I/O | | 169 | 249 | 249 | 290 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 68 | 79 | 79 | 89 |
| | Dedicated Pins | 3 | 3 | 3 | 3 |
| VCC | | 16 | 20 | 20 | 26 |
| VCCAUX | | 16 | 16 | 16 | 17 |
| VCCPLL | | 4 | 4 | 2 | 4 |
| VCCIO | Bank0 | 4 | 5 | 5 | 6 |
| | Bank1 | 4 | 5 | 5 | 6 |
| | Bank2 | 4 | 5 | 5 | 6 |
| | Bank3 | 4 | 5 | 5 | 6 |
| | Bank4 | 4 | 5 | 5 | 6 |
| | Bank5 | 4 | 5 | 5 | 6 |
| | Bank6 | 4 | 5 | 5 | 6 |
| | Bank7 | 4 | 5 | 5 | 6 |
| | Bank8 | 2 | 2 | 2 | 2 |
| GND, GND0 to GND7 | | 60 | 72 | 72 | 104 |
| NC | | 0 | 3 | 5 | 101 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 50/25 | 67/33 | 67/33 | 84/42 |
| | Bank1 | 46/23 | 66/33 | 66/33 | 76/38 |
| | Bank2 | 38/19 | 56/28 | 56/28 | 74/37 |
| | Bank3 | 22/11 | 48/24 | 48/24 | 48/24 |
| | Bank4 | 46/23 | 62/31 | 62/31 | 72/35 |
| | Bank5 | 46/23 | 68/34 | 68/34 | 80/40 |
| | Bank6 | 40/20 | 64/32 | 64/32 | 64/32 |
| | Bank7 | 37/18 | 55/27 | 55/27 | 71/35 |
| | Bank8 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 9 | 13 | 13 | 18 |
| | Bank3 (Right Edge) | 5 | 12 | 12 | 12 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 10 | 16 | 16 | 16 |
| | Bank7 (Left Edge) | 8 | 12 | 12 | 16 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 184 | GND | - | | | GND | - | | |
| 185 | PT28A | 0 | PCLKT0_0 | T | PT37A | 0 | PCLKT0_0 | T |
| 186 | PT26B | 0 | | C | PT36B | 0 | | C |
| 187 | PT26A | 0 | | T | PT36A | 0 | | T |
| 188 | VCC | - | | | VCC | - | | |
| 189 | PT20B | 0 | | C | PT30B | 0 | | C |
| 190 | VCCAUX | - | | | VCCAUX | - | | |
| 191 | PT20A | 0 | | T | PT30A | 0 | | T |
| 192 | GND | - | | | GND | - | | |
| 193 | PT18B | 0 | | C | PT26B | 0 | | C |
| 194 | PT18A | 0 | | T | PT26A | 0 | | T |
| 195 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 196 | PT16B | 0 | | C | PT20B | 0 | | C |
| 197 | PT16A | 0 | | T | PT20A | 0 | | T |
| 198 | VCC | - | | | VCC | - | | |
| 199 | PT12B | 0 | | C | PT12B | 0 | | C |
| 200 | PT12A | 0 | | T | PT12A | 0 | | T |
| 201 | GND | - | | | GND | - | | |
| 202 | PT8B | 0 | | C | PT8B | 0 | | C |
| 203 | PT8A | 0 | | T | PT8A | 0 | | T |
| 204 | PT6B | 0 | | C | PT6B | 0 | | C |
| 205 | PT6A | 0 | | T | PT6A | 0 | | T |
| 206 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| 207 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| 208 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M8 | PB8B | 5 | PCLKC5_0/BDQ6 | C | PB26B | 5 | PCLKC5_0/BDQ24 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| P7 | PB13A | 4 | PCLKT4_0/BDQ15 | T | PB31A | 4 | PCLKT4_0/BDQ33 | T |
| R8 | PB13B | 4 | PCLKC4_0/BDQ15 | C | PB31B | 4 | PCLKC4_0/BDQ33 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T5 | PB14A | 4 | BDQ15 | T | PB32A | 4 | BDQ33 | T |
| T6 | PB14B | 4 | BDQ15 | C | PB32B | 4 | BDQ33 | C |
| T8 | PB15A | 4 | BDQS15 | T | PB33A | 4 | BDQS33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R7 | PB16A | 4 | BDQ15 | T | PB34A | 4 | BDQ33 | T |
| T9 | PB15B | 4 | BDQ15 | C | PB33B | 4 | BDQ33 | C |
| T7 | PB16B | 4 | BDQ15 | C | PB34B | 4 | BDQ33 | C |
| L8 | PB17A | 4 | BDQ15 | T | PB35A | 4 | BDQ33 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| P8 | PB18A | 4 | BDQ15 | T | PB36A | 4 | BDQ33 | T |
| L9 | PB17B | 4 | BDQ15 | C | PB35B | 4 | BDQ33 | C |
| N8 | PB18B | 4 | BDQ15 | C | PB36B | 4 | BDQ33 | C |
| R9 | PB19A | 4 | BDQ15 | T | PB37A | 4 | BDQ33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R10 | PB19B | 4 | BDQ15 | C | PB37B | 4 | BDQ33 | C |
| - | - | - | | | VCCIO | 4 | | |
| - | - | - | | | GNDIO4 | 4 | | |
| N9 | PB20A | 4 | BDQ24 | T | PB47A | 4 | BDQ51 | T |
| T10 | PB21A | 4 | BDQ24 | T | PB48A | 4 | BDQ51 | T |
| M9 | PB20B | 4 | BDQ24 | C | PB47B | 4 | BDQ51 | C |
| R11 | PB21B | 4 | BDQ24 | C | PB48B | 4 | BDQ51 | C |
| P10 | PB22A | 4 | BDQ24 | T | PB49A | 4 | BDQ51 | T |
| N11 | PB23A | 4 | BDQ24 | T | PB50A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| N10 | PB22B | 4 | BDQ24 | C | PB49B | 4 | BDQ51 | C |
| P11 | PB23B | 4 | BDQ24 | C | PB50B | 4 | BDQ51 | C |
| T11 | PB24A | 4 | BDQS24 | T | PB51A | 4 | BDQS51 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| M11 | PB25A | 4 | BDQ24 | T | PB52A | 4 | BDQ51 | T |
| T12 | PB24B | 4 | BDQ24 | C | PB51B | 4 | BDQ51 | C |
| L11 | PB25B | 4 | BDQ24 | C | PB52B | 4 | BDQ51 | C |
| T13 | PB26A | 4 | BDQ24 | T | PB53A | 4 | BDQ51 | T |
| R13 | PB27A | 4 | BDQ24 | T | PB54A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T14 | PB26B | 4 | BDQ24 | C | PB53B | 4 | BDQ51 | C |
| P13 | PB27B | 4 | BDQ24 | C | PB54B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| N12 | PB28A | 4 | VREF2_4/BDQ24 | T | PB55A | 4 | VREF2_4/BDQ51 | T |
| M12 | PB28B | 4 | VREF1_4/BDQ24 | C | PB55B | 4 | VREF1_4/BDQ51 | C |
| R15 | CFG2 | 8 | | | CFG2 | 8 | | |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T7 | PL29B | 6 | LDQ28 | C | PL43B | 6 | LDQ42 | C |
| T6 | PL26B | 6 | LDQ28 | C (LVDS)* | PL40B | 6 | LDQ42 | C (LVDS)* |
| AA2 | PL31A | 6 | LDQ28 | T | PL45A | 6 | LDQ42 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y1 | PL28A | 6 | LDQS28 | T (LVDS)* | PL42A | 6 | LDQS42 | T (LVDS)* |
| AA1 | PL31B | 6 | LDQ28 | C | PL45B | 6 | LDQ42 | C |
| W1 | PL28B | 6 | LDQ28 | C (LVDS)* | PL42B | 6 | LDQ42 | C (LVDS)* |
| V3 | PL30B | 6 | LDQ28 | C (LVDS)* | PL44B | 6 | LDQ42 | C (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO | - | | |
| V4 | PL30A | 6 | LDQ28 | T (LVDS)* | PL44A | 6 | LDQ42 | T (LVDS)* |
| U5 | TDI | - | | | TDI | - | | |
| U7 | TCK | - | | | TCK | - | | |
| V6 | TDO | - | | | TDO | - | | |
| V5 | TMS | - | | | TMS | - | | |
| T8 | VCCJ | - | | | VCCJ | - | | |
| W4 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| Y3 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| W3 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| Y2 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| AB3 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| W5 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AB2 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| W6 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| AB5 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| Y4 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| AB4 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA3 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AB6 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA5 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| AA6 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| Y5 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| - | - | - | | | VCCIO5 | 5 | | |
| Y6 | PB12A | 5 | BDQ15 | T | PB21A | 5 | BDQ24 | T |
| W7 | PB11A | 5 | BDQ15 | T | PB20A | 5 | BDQ24 | T |
| Y7 | PB12B | 5 | BDQ15 | C | PB21B | 5 | BDQ24 | C |
| W8 | PB11B | 5 | BDQ15 | C | PB20B | 5 | BDQ24 | C |
| U8 | PB14A | 5 | BDQ15 | T | PB23A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA7 | PB13A | 5 | BDQ15 | T | PB22A | 5 | BDQ24 | T |
| U9 | PB14B | 5 | BDQ15 | C | PB23B | 5 | BDQ24 | C |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J22 | PR29B | 3 | RDQ31 | C (LVDS)* | PR48B | 3 | RDQ50 | C (LVDS)* |
| H22 | PR29A | 3 | RDQ31 | T (LVDS)* | PR48A | 3 | RDQ50 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| M20 | PR28B | 3 | VREF2_3/RDQ31 | C | PR47B | 3 | VREF2_3/RDQ50 | C |
| L21 | PR28A | 3 | VREF1_3/RDQ31 | T | PR47A | 3 | VREF1_3/RDQ50 | T |
| K21 | PR27B | 3 | PCLKC3_0/RDQ31 | C (LVDS)* | PR46B | 3 | PCLKC3_0/RDQ50 | C (LVDS)* |
| J21 | PR27A | 3 | PCLKT3_0/RDQ31 | T (LVDS)* | PR46A | 3 | PCLKT3_0/RDQ50 | T (LVDS)* |
| M18 | PR25B | 2 | PCLKC2_0/RDQ22 | C | PR44B | 2 | PCLKC2_0/RDQ41 | C |
| L17 | PR25A | 2 | PCLKT2_0/RDQ22 | T | PR44A | 2 | PCLKT2_0/RDQ41 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L19 | PR24B | 2 | RDQ22 | C (LVDS)* | PR43B | 2 | RDQ41 | C (LVDS)* |
| L20 | PR24A | 2 | RDQ22 | T (LVDS)* | PR43A | 2 | RDQ41 | T (LVDS)* |
| L18 | PR23B | 2 | RDQ22 | C | PR42B | 2 | RDQ41 | C |
| K17 | PR23A | 2 | RDQ22 | T | PR42A | 2 | RDQ41 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| K18 | PR22B | 2 | RDQ22 | C (LVDS)* | PR41B | 2 | RDQ41 | C (LVDS)* |
| K19 | PR22A | 2 | RDQS22 | T (LVDS)* | PR41A | 2 | RDQS41 | T (LVDS)* |
| G22 | PR21B | 2 | RDQ22 | C | PR40B | 2 | RDQ41 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F22 | PR21A | 2 | RDQ22 | T | PR40A | 2 | RDQ41 | T |
| J17 | PR20B | 2 | RDQ22 | C (LVDS)* | PR39B | 2 | RDQ41 | C (LVDS)* |
| J18 | PR20A | 2 | RDQ22 | T (LVDS)* | PR39A | 2 | RDQ41 | T (LVDS)* |
| K20 | PR19B | 2 | RDQ22 | C | PR38B | 2 | RDQ41 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| J19 | PR19A | 2 | RDQ22 | T | PR38A | 2 | RDQ41 | T |
| H21 | PR18B | 2 | RDQ22 | C (LVDS)* | PR37B | 2 | RDQ41 | C (LVDS)* |
| G21 | PR18A | 2 | RDQ22 | T (LVDS)* | PR37A | 2 | RDQ41 | T (LVDS)* |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | VCCIO | 2 | | |
| H17 | NC | - | | | PR26B | 2 | RUM0_SPLLC_FB_A/RDQ24 | C |
| H16 | NC | - | | | PR26A | 2 | RUM0_SPLLT_FB_A/RDQ24 | T |
| H20 | NC | - | | | PR25B | 2 | RUM0_SPLLC_IN_A/RDQ24 | C |
| H18 | NC | - | | | PR25A | 2 | RUM0_SPLLT_IN_A/RDQ24 | T |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | VCCIO | 2 | | |
| F21 | PR17B | 2 | RDQ14 | C | PR19B | 2 | RDQ16 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR17A | 2 | RDQ14 | T | PR19A | 2 | RDQ16 | T |
| D22 | PR16B | 2 | RDQ14 | C (LVDS)* | PR18B | 2 | RDQ16 | C (LVDS)* |
| E21 | PR16A | 2 | RDQ14 | T (LVDS)* | PR18A | 2 | RDQ16 | T (LVDS)* |
| G20 | PR15B | 2 | RDQ14 | C | PR17B | 2 | RDQ16 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO | 2 | | |
| F20 | PR15A | 2 | RDQ14 | T | PR17A | 2 | RDQ16 | T |
| H19 | PR14B | 2 | RDQ14 | C (LVDS)* | PR16B | 2 | RDQ16 | C (LVDS)* |
| G19 | PR14A | 2 | RDQS14 | T (LVDS)* | PR16A | 2 | RDQS16 | T (LVDS)* |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K1 | PL27B | 7 | LDQ29 | C (LVDS)* |
| K5 | PL28A | 7 | LDQ29 | T |
| K7 | PL28B | 7 | LDQ29 | C |
| GND | GNDIO7 | - | | |
| K4 | PL29A | 7 | LDQS29 | T (LVDS)* |
| K3 | PL29B | 7 | LDQ29 | C (LVDS)* |
| L8 | PL30A | 7 | LDQ29 | T |
| VCCIO | VCCIO7 | 7 | | |
| L6 | PL30B | 7 | LDQ29 | C |
| L2 | PL31A | 7 | LDQ29 | T (LVDS)* |
| L1 | PL31B | 7 | LDQ29 | C (LVDS)* |
| L7 | PL32A | 7 | LDQ29 | T |
| GND | GNDIO7 | - | | |
| L5 | PL32B | 7 | LDQ29 | C |
| L4 | PL33A | 7 | LDQ37 | T (LVDS)* |
| L3 | PL33B | 7 | LDQ37 | C (LVDS)* |
| M8 | PL34A | 7 | LDQ37 | T |
| M6 | PL34B | 7 | LDQ37 | C |
| VCCIO | VCCIO7 | 7 | | |
| M2 | PL35A | 7 | LDQ37 | T (LVDS)* |
| M1 | PL35B | 7 | LDQ37 | C (LVDS)* |
| M7 | PL36A | 7 | LDQ37 | T |
| M5 | PL36B | 7 | LDQ37 | C |
| GND | GNDIO7 | - | | |
| M4 | PL37A | 7 | LDQS37 | T (LVDS)* |
| M3 | PL37B | 7 | LDQ37 | C (LVDS)* |
| N6 | PL38A | 7 | LUM0_SPLLT_IN_A/LDQ37 | T |
| VCCIO | VCCIO7 | 7 | | |
| N8 | PL38B | 7 | LUM0_SPLLC_IN_A/LDQ37 | C |
| N5 | PL39A | 7 | LUM0_SPLLT_FB_A/LDQ37 | T |
| N7 | PL39B | 7 | LUM0_SPLLC_FB_A/LDQ37 | C |
| GND | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| T9 | PL50A | 7 | LDQ54 | |
| R9 | PL51A | 7 | LDQ54 | T |
| P7 | PL51B | 7 | LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | |
| N2 | PL52A | 7 | LDQ54 | T (LVDS)* |
| N1 | PL52B | 7 | LDQ54 | C (LVDS)* |
| P6 | PL53A | 7 | LDQ54 | T |
| P5 | PL53B | 7 | LDQ54 | C |
| GND | GNDIO7 | - | | |
| P4 | PL54A | 7 | LDQS54 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AD18 | PB66A | 4 | BDQ69 | T |
| AF18 | PB66B | 4 | BDQ69 | C |
| AC18 | PB67A | 4 | BDQ69 | T |
| AE18 | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AG19 | PB68A | 4 | BDQ69 | T |
| AH19 | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AE19 | PB69A | 4 | BDQS69 | T |
| AF19 | PB69B | 4 | BDQ69 | C |
| AC19 | PB70A | 4 | BDQ69 | T |
| AD19 | PB70B | 4 | BDQ69 | C |
| AJ19 | PB71A | 4 | BDQ69 | T |
| AK19 | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AF20 | PB72A | 4 | BDQ69 | T |
| AH20 | PB72B | 4 | BDQ69 | C |
| AE20 | PB73A | 4 | BDQ69 | T |
| AG20 | PB73B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AD20 | PB74A | 4 | BDQ78 | T |
| AC20 | PB74B | 4 | BDQ78 | C |
| AH21 | PB75A | 4 | BDQ78 | T |
| AF21 | PB75B | 4 | BDQ78 | C |
| AJ20 | PB76A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK20 | PB76B | 4 | BDQ78 | C |
| AG21 | PB77A | 4 | BDQ78 | T |
| AE21 | PB77B | 4 | BDQ78 | C |
| AD21 | PB78A | 4 | BDQS78 | T |
| GND | GNDIO4 | - | | |
| AC21 | PB78B | 4 | BDQ78 | C |
| AD22 | PB79A | 4 | BDQ78 | T |
| AB21 | PB79B | 4 | BDQ78 | C |
| AJ21 | PB80A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK21 | PB80B | 4 | BDQ78 | C |
| GND | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | |
| AJ25 | PB87A | 4 | BDQS87*** | T |
| AK24 | PB87B | 4 | BDQ87 | C |
| AJ24 | PB88A | 4 | BDQ87 | T |
| AK25 | PB88B | 4 | BDQ87 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| L11 | GND | - | | |
| L12 | GND | - | | |
| L13 | GND | - | | |
| M10 | GND | - | | |
| M11 | GND | - | | |
| M12 | GND | - | | |
| M13 | GND | - | | |
| N10 | GND | - | | |
| N11 | GND | - | | |
| N12 | GND | - | | |
| N13 | GND | - | | |
| N15 | GND | - | | |
| N20 | GND | - | | |
| N3 | GND | - | | |
| N8 | GND | - | | |
| P14 | GND | - | | |
| P9 | GND | - | | |
| R10 | GND | - | | |
| R13 | GND | - | | |
| T19 | GND | - | | |
| T4 | GND | - | | |
| W16 | GND | - | | |
| W2 | GND | - | | |
| W21 | GND | - | | |
| W7 | GND | - | | |
| Y10 | GND | - | | |
| Y13 | GND | - | | |
| Y15 | NC | - | | |
| W15 | NC | - | | |
| AB20 | NC | - | | |
| AB21 | NC | - | | |
| AA21 | NC | - | | |
| AA20 | NC | - | | |
| AB19 | NC | - | | |
| AB18 | NC | - | | |
| Y22 | NC | - | | |
| Y21 | NC | - | | |
| Y17 | NC | - | | |
| Y18 | NC | - | | |
| Y16 | NC | - | | |
| W17 | NC | - | | |
| Y19 | NC | - | | |
| Y20 | NC | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AJ30 | LRC_SQ_VCCIB0 | 13 | | |
| AK29 | LRC_SQ_HDINP0 | 13 | | T |
| AH30 | LRC_SQ_VCCRX0 | 13 | | |
| AG27 | CFG2 | 8 | | |
| AD25 | CFG1 | 8 | | |
| AG28 | CFG0 | 8 | | |
| AG30 | PROGRAMN | 8 | | |
| AG29 | CCLK | 8 | | |
| AC24 | INITN | 8 | | |
| AF27 | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | |
| AF28 | WRITEN*** | 8 | | |
| AE26 | CS1N*** | 8 | | |
| AB23 | CSN*** | 8 | | |
| AF29 | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| AF30 | D1*** | 8 | | |
| AD26 | D2*** | 8 | | |
| AE29 | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | |
| AE30 | D4*** | 8 | | |
| AD29 | D5*** | 8 | | |
| AC25 | D6*** | 8 | | |
| AD30 | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | |
| AA22 | DI/CSSPI0N*** | 8 | | |
| AC26 | DOUT/CSON/CSSPI1N*** | 8 | | |
| AA23 | BUSY/SISPI*** | 8 | | |
| AB22 | RLM0_PLLCAP | 3 | | |
| AC27 | PR102B | 3 | RLM0_GDLLC_FB_A/RDQ99 | C |
| GNDIO | GNDIO3 | - | | |
| AC28 | PR102A | 3 | RLM0_GDLLT_FB_A/RDQ99 | T |
| AC29 | PR101B | 3 | RLM0_GDLLC_IN_A**/RDQ99 | C (LVDS)* |
| AC30 | PR101A | 3 | RLM0_GDLLT_IN_A**/RDQ99 | T (LVDS)* |
| AB30 | PR100B | 3 | RLM0_GPLLC_IN_A**/RDQ99 | C |
| VCCIO | VCCIO3 | 3 | | |
| AA30 | PR100A | 3 | RLM0_GPLLT_IN_A**/RDQ99 | T |
| AB29 | PR99B | 3 | RLM0_GPLLC_FB_A/RDQ99 | C (LVDS)* |
| AB28 | PR99A | 3 | RLM0_GPLLT_FB_A/RDQS99 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| Y22 | PR98B | 3 | RDQ99 | C |
| Y23 | PR98A | 3 | RDQ99 | T |
| AB26 | PR97B | 3 | RDQ99 | C (LVDS)* |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| M19 | VCC | - | | |
| M20 | VCC | - | | |
| N11 | VCC | - | | |
| N12 | VCC | - | | |
| N19 | VCC | - | | |
| N20 | VCC | - | | |
| P12 | VCC | - | | |
| P19 | VCC | - | | |
| R12 | VCC | - | | |
| R19 | VCC | - | | |
| T12 | VCC | - | | |
| T19 | VCC | - | | |
| U12 | VCC | - | | |
| U19 | VCC | - | | |
| V11 | VCC | - | | |
| V12 | VCC | - | | |
| V19 | VCC | - | | |
| V20 | VCC | - | | |
| W11 | VCC | - | | |
| W12 | VCC | - | | |
| W13 | VCC | - | | |
| W14 | VCC | - | | |
| W15 | VCC | - | | |
| W16 | VCC | - | | |
| W17 | VCC | - | | |
| W18 | VCC | - | | |
| W19 | VCC | - | | |
| W20 | VCC | - | | |
| Y12 | VCC | - | | |
| Y13 | VCC | - | | |
| Y18 | VCC | - | | |
| Y19 | VCC | - | | |
| D14 | VCCIO0 | 0 | | |
| E6 | VCCIO0 | 0 | | |
| E9 | VCCIO0 | 0 | | |
| F12 | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | |
| K13 | VCCIO0 | 0 | | |
| D17 | VCCIO1 | 1 | | |
| E22 | VCCIO1 | 1 | | |
| E25 | VCCIO1 | 1 | | |
| F19 | VCCIO1 | 1 | | |
| K18 | VCCIO1 | 1 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AE27 | GND | - | | |
| AE4 | GND | - | | |
| AE9 | GND | - | | |
| AF14 | GND | - | | |
| AF17 | GND | - | | |
| AF25 | GND | - | | |
| AF6 | GND | - | | |
| AJ10 | GND | - | | |
| AJ21 | GND | - | | |
| AJ27 | GND | - | | |
| AJ4 | GND | - | | |
| AK1 | GND | - | | |
| AK13 | GND | - | | |
| AK18 | GND | - | | |
| AK24 | GND | - | | |
| AK30 | GND | - | | |
| AK7 | GND | - | | |
| B10 | GND | - | | |
| B21 | GND | - | | |
| B27 | GND | - | | |
| B4 | GND | - | | |
| D25 | GND | - | | |
| D6 | GND | - | | |
| E14 | GND | - | | |
| E17 | GND | - | | |
| F22 | GND | - | | |
| F27 | GND | - | | |
| F4 | GND | - | | |
| F9 | GND | - | | |
| G12 | GND | - | | |
| G19 | GND | - | | |
| J24 | GND | - | | |
| J7 | GND | - | | |
| K14 | GND | - | | |
| K15 | GND | - | | |
| K16 | GND | - | | |
| K17 | GND | - | | |
| K27 | GND | - | | |
| K4 | GND | - | | |
| L14 | GND | - | | |
| L15 | GND | - | | |
| L16 | GND | - | | |
| L17 | GND | - | | |

# LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| V18 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** These sysCONFIG pins are dedicated I/O pins for configuration. The outpus are actively driven during normal device operation.
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W30 | PR53A | 3 | RDQ55 | T (LVDS)* | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| U27 | PR52B | 3 | VREF2_3/RDQ55 | C | PR60B | 3 | VREF2_3/RDQ63 | C |
| V29 | PR52A | 3 | VREF1_3/RDQ55 | T | PR60A | 3 | VREF1_3/RDQ63 | T |
| V31 | PR51B | 3 | PCLKC3_0/RDQ55 | C (LVDS)* | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| V32 | PR51A | 3 | PCLKT3_0/RDQ55 | T (LVDS)* | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| V33 | PR49B | 2 | PCLKC2_0/RDQ46 | C | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| V34 | PR49A | 2 | PCLKT2_0/RDQ46 | T | PR57A | 2 | PCLKT2_0/RDQ54 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| U24 | PR48B | 2 | RDQ46 | C (LVDS)* | PR56B | 2 | RDQ54 | C (LVDS)* |
| U25 | PR48A | 2 | RDQ46 | T (LVDS)* | PR56A | 2 | RDQ54 | T (LVDS)* |
| V30 | PR47B | 2 | RDQ46 | C | PR55B | 2 | RDQ54 | C |
| Y32 | PR47A | 2 | RDQ46 | T | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| U28 | PR46B | 2 | RDQ46 | C (LVDS)* | PR54B | 2 | RDQ54 | C (LVDS)* |
| U29 | PR46A | 2 | RDQS46 | T (LVDS)* | PR54A | 2 | RDQS54 | T (LVDS)* |
| U33 | PR45B | 2 | RDQ46 | C | PR53B | 2 | RDQ54 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| U34 | PR45A | 2 | RDQ46 | T | PR53A | 2 | RDQ54 | T |
| T30 | PR44B | 2 | RDQ46 | C (LVDS)* | PR52B | 2 | RDQ54 | C (LVDS)* |
| U30 | PR44A | 2 | RDQ46 | T (LVDS)* | PR52A | 2 | RDQ54 | T (LVDS)* |
| T29 | PR43B | 2 | RUM3_SPLLC_FB_A/RDQ46 | C | PR51B | 2 | RUM3_SPLLC_FB_A/RDQ54 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T28 | PR43A | 2 | RUM3_SPLLT_FB_A/RDQ46 | T | PR51A | 2 | RUM3_SPLLT_FB_A/RDQ54 | T |
| U31 | PR42B | 2 | RUM3_SPLLC_IN_A/RDQ46 | C (LVDS)* | PR50B | 2 | RUM3_SPLLC_IN_A/RDQ54 | C (LVDS)* |
| U32 | PR42A | 2 | RUM3_SPLLT_IN_A/RDQ46 | T (LVDS)* | PR50A | 2 | RUM3_SPLLT_IN_A/RDQ54 | T (LVDS)* |
| T33 | PR40B | 2 | RDQ37 | C | PR48B | 2 | RDQ45 | C |
| T34 | PR40A | 2 | RDQ37 | T | PR48A | 2 | RDQ45 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| R27 | PR39B | 2 | RDQ37 | C (LVDS)* | PR47B | 2 | RDQ45 | C (LVDS)* |
| R28 | PR39A | 2 | RDQ37 | T (LVDS)* | PR47A | 2 | RDQ45 | T (LVDS)* |
| R29 | PR38B | 2 | RDQ37 | C | PR46B | 2 | RDQ45 | C |
| R30 | PR38A | 2 | RDQ37 | T | PR46A | 2 | RDQ45 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| R33 | PR37B | 2 | RDQ37 | C (LVDS)* | PR45B | 2 | RDQ45 | C (LVDS)* |
| R34 | PR37A | 2 | RDQS37 | T (LVDS)* | PR45A | 2 | RDQS45 | T (LVDS)* |
| R32 | PR36B | 2 | RDQ37 | C | PR44B | 2 | RDQ45 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| R31 | PR36A | 2 | RDQ37 | T | PR44A | 2 | RDQ45 | T |
| P34 | PR35B | 2 | RDQ37 | C (LVDS)* | PR43B | 2 | RDQ45 | C (LVDS)* |
| P33 | PR35A | 2 | RDQ37 | T (LVDS)* | PR43A | 2 | RDQ45 | T (LVDS)* |
| R26 | PR34B | 2 | RDQ37 | C | PR42B | 2 | RDQ45 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| T25 | PR34A | 2 | RDQ37 | T | PR42A | 2 | RDQ45 | T |
| P28 | PR33B | 2 | RDQ37 | C (LVDS)* | PR41B | 2 | RDQ45 | C (LVDS)* |
| P27 | PR33A | 2 | RDQ37 | T (LVDS)* | PR41A | 2 | RDQ45 | T (LVDS)* |
| P30 | NC | - | | | PR40B | 2 | | C |
| - | - | - | | | GNDIO2 | - | | |
| P29 | NC | - | | | PR40A | 2 | | T |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20SE-5QN208I | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | Ind | 20 |
| LFE2-20SE-6QN208I | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | Ind | 20 |
| LFE2-20SE-5FN256I | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | Ind | 20 |
| LFE2-20SE-6FN256I | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | Ind | 20 |
| LFE2-20SE-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2-20SE-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 20 |
| LFE2-20SE-5FN672I | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 20 |
| LFE2-20SE-6FN672I | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5FN484I | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2-35SE-6FN484I | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 35 |
| LFE2-35SE-5FN672I | 450 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 35 |
| LFE2-35SE-6FN672I | 450 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5FN484I | 339 | 1.2V | -5 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2-50SE-6FN484I | 339 | 1.2V | -6 | Lead-Free fpBGA | 484 | Ind | 50 |
| LFE2-50SE-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 50 |
| LFE2-50SE-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5FN672I | 500 | 1.2V | -5 | Lead-Free fpBGA | 672 | Ind | 70 |
| LFE2-70SE-6FN672I | 500 | 1.2V | -6 | Lead-Free fpBGA | 672 | Ind | 70 |
| LFE2-70SE-5FN900I | 583 | 1.2V | -5 | Lead-Free fpBGA | 900 | Ind | 70 |
| LFE2-70SE-6FN900I | 583 | 1.2V | -6 | Lead-Free fpBGA | 900 | Ind | 70 |