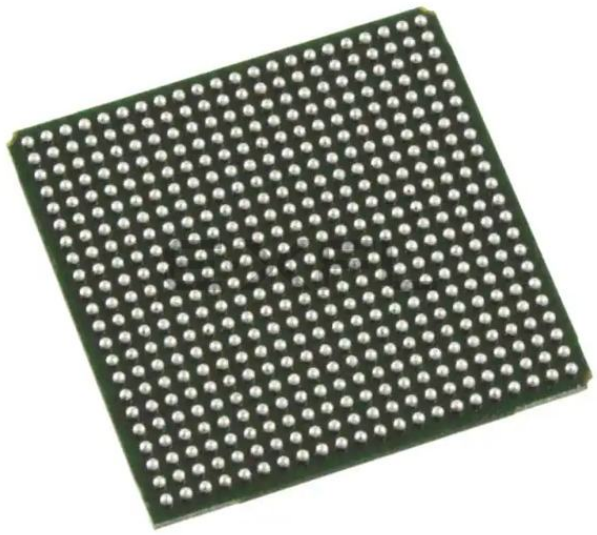
# Lattice Semiconductor Corporation - LFE2-35SE-5F484C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4000 |
| Number of Logic Elements/Cells | 32000 |
| Total RAM Bits | 339968 |
| Number of I/O | 331 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-5f484c |

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

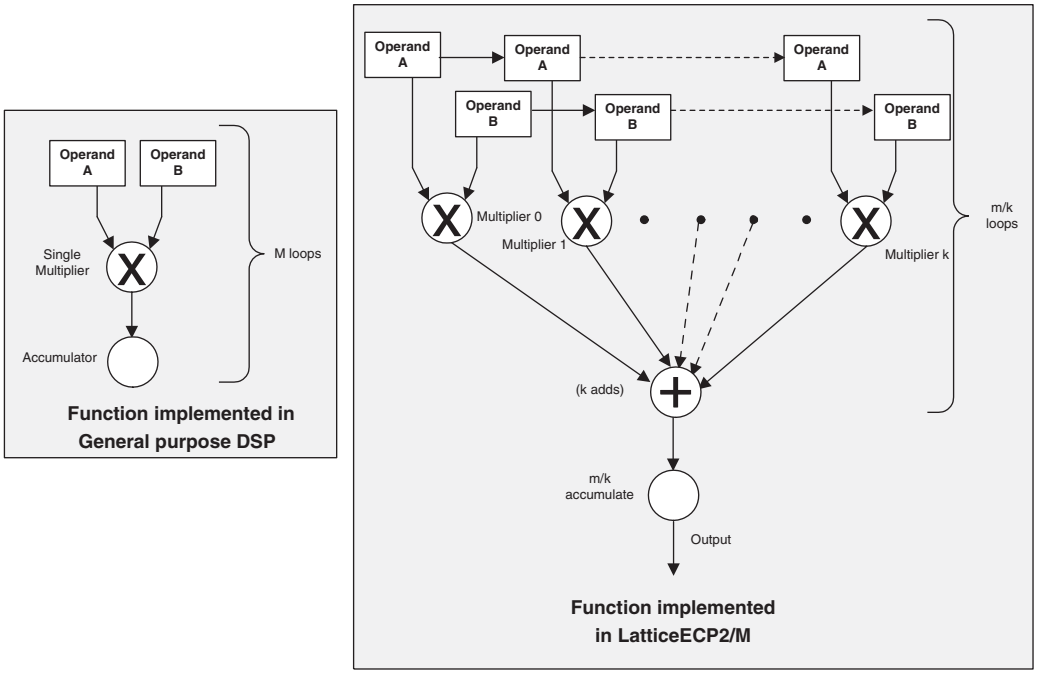
# sysDSP™ Block

The LatticeECP2/M family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

## sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2/M, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-22 compares the fully serial and the mixed parallel and serial implementations.

***Figure 2-22. Comparison of General DSP and LatticeECP2/M Approaches***




## sysDSP Block Capabilities

The sysDSP block in the LatticeECP2/M family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2/M family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In the LatticeECP2/M family the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following elements:

## MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-23 shows the MULT sysDSP element.

***Figure 2-23. MULT sysDSP Element***

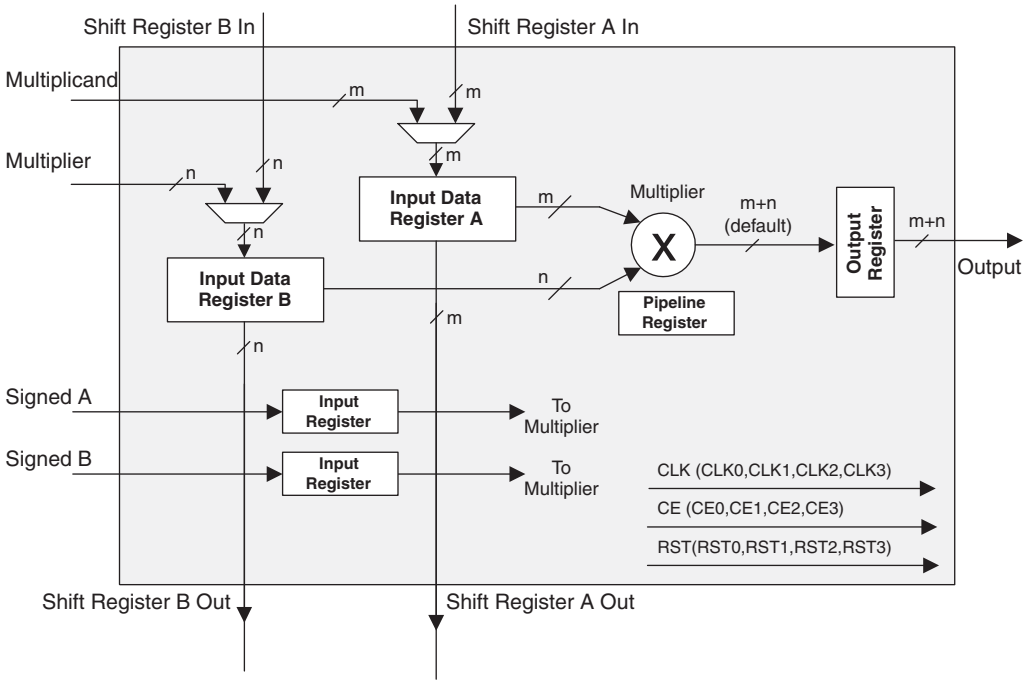
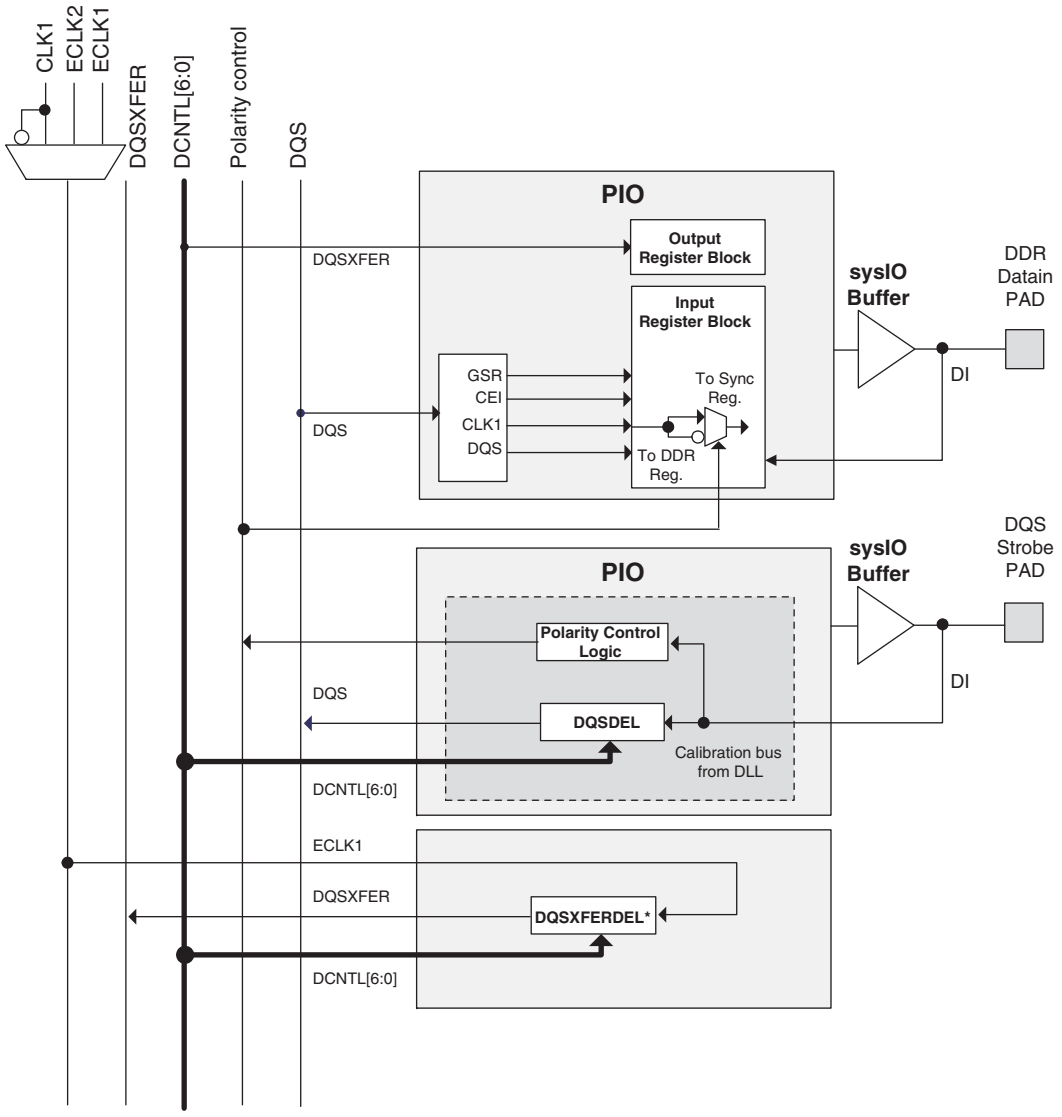


*Figure 2-36. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

## sysCLOCK SPLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[5, 6] | 2 | — | 420 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[5] | 5 | — | 50 | MHz |
| $f_{OUT2}$ | K-Divider Output Frequency (CLKOK) | Without external capacitor | 0.258 | — | 210 | MHz |
| | | With external capacitor[5] | 0.039 | — | 25 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 640 | — | 1280 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | Without external capacitor | 33 | — | 420 | MHz |
| | | With external capacitor[6] | 2 | — | 50 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default Duty Cycle Selected[3] | 45 | 50 | 55 | % |
| $t_{PH}$[4] | Output Phase Accuracy | | — | — | ±0.05 | UI |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | $f_{OUT} \geq 100$ MHz | — | — | ±125 | ps |
| | | $50 \leq f_{OUT} < 100$ MHz | — | — | 0.025 | UIPP |
| | | $f_{OUT} < 50$ MHz | — | — | 0.04 | UIPP |
| $t_{SK}$ | Input Clock to Output Clock Skew | Divider Ratio = Integer | — | — | ±250 | ps |
| $t_W$ | Output Clock Pulse Width | At 90% or 10% | 1 | — | — | ns |
| $t_{LOCK}$[2] | PLL Lock-in Time | Without external capacitor | — | — | 150 | µs |
| | | With external capacitor[5] | — | — | 500 | µs |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | ±200 | ps |
| $t_{FBKDLY}$ | External Feedback Delay | | — | — | 10 | ns |
| $t_{HI}$ | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| $t_{LO}$ | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| $t_{RST}$ | RST Pulse Width (RSTK) | | 15 | — | — | ns |
| | Reset Signal Pulse Width (RST) | Without external capacitor | 500 | — | — | ns |
| | | With external capacitor[5] | 20 | — | — | µs |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Phase accuracy of CLKOS compared to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. $f_{OUT}$ (max) = $f_{IN}$ * 10 for $f_{IN}$ < 5MHz.

## LatticeECP2M Power Supply and NC

| Signal | 256 fpBGA | 484 fpBGA |
|---|---|---|
| $V_{CC}$ | G7, G9, H7, J10, K10, K8 | J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 |
| $V_{CCIO0}$ | E7 | B5, B9, E7, H9 |
| $V_{CCIO1}$ | E10 | D13, E16, H14 |
| $V_{CCIO2}$ | E14, G12 | E21, G18, J15, K19 |
| $V_{CCIO3}$ | K12, M14 | N19, P15, T18, V21 |
| $V_{CCIO4}$ | M10, P12 | AA18, R14, V16, W13 |
| $V_{CCIO5}$ | M7, P5 | AA5, R9, V7, W10 |
| $V_{CCIO6}$ | K5, M3 | N4, P8, T5, V2 |
| $V_{CCIO7}$ | E3, G5 | E2, G5, J8, K4 |
| $V_{CCIO8}$ | T15 | AA22, U19 |
| $V_{CCJ}$ | K7 | W4 |
| $V_{CCAUX}$ | G8, H10, J7, K9 | H11, H12, L15, L8, M15, M8, R11, R12 |
| $V_{CCPLL}$ | G10 | R8, H15, H8, R15 |
| SERDES Power[3] | C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3 | C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10 |
| GND[1] | A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16 | A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13 |
| NC[2] | D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9 | **LFE2M20:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15<br>**LFE2M35:** D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15, U6<br>**LFE2M50:** Y15, W15, AB20, AB21, AA20, AB19, AB18, Y22, Y21, Y17, Y18, Y16, W17, Y19, Y20, W19, W18, V17, V18, D15, G14, G15, D14, E15, E14, F15, F14, F13, G12, G13 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 46 | PL28B | 6 | LDQ28 | C (LVDS)* | PL42B | 6 | LDQ42 | C (LVDS)* |
| 47 | PL30A | 6 | LDQ28 | | PL44A | 6 | LDQ42 | |
| 48 | TCK | - | | | TCK | - | | |
| 49 | TDI | - | | | TDI | - | | |
| 50 | TDO | - | | | TDO | - | | |
| 51 | VCCJ | - | | | VCCJ | - | | |
| 52 | TMS | - | | | TMS | - | | |
| 53 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| 54 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| 55 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 56 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| 57 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| 58 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| 59 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| 60 | GND | - | | | GND | - | | |
| 61 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| 62 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| 63 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 64 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| 65 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| 66 | PB18A | 5 | BDQ15 | T | PB18A | 5 | BDQ15 | T |
| 67 | PB18B | 5 | BDQ15 | C | PB18B | 5 | BDQ15 | C |
| 68 | GND | - | | | GND | - | | |
| 69 | PB20A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| 70 | VCCAUX | - | | | VCCAUX | - | | |
| 71 | PB20B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| 72 | PB22A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| 73 | PB22B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| 74 | VCC | - | | | VCC | - | | |
| 75 | PB26A | 5 | PCLKT5_0/BDQ24 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| 76 | PB26B | 5 | PCLKC5_0/BDQ24 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| 77 | GND | - | | | GND | - | | |
| 78 | PB31A | 4 | PCLKT4_0/BDQ33 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| 79 | PB31B | 4 | PCLKC4_0/BDQ33 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| 80 | VCC | - | | | VCC | - | | |
| 81 | GND | - | | | GND | - | | |
| 82 | PB34A | 4 | BDQ33 | T | PB42A | 4 | BDQS42 | T |
| 83 | PB34B | 4 | BDQ33 | C | PB42B | 4 | BDQ42 | C |
| 84 | PB36A | 4 | BDQ33 | T | PB44A | 4 | BDQ42 | T |
| 85 | PB36B | 4 | BDQ33 | C | PB44B | 4 | BDQ42 | C |
| 86 | VCCAUX | - | | | VCCAUX | - | | |
| 87 | PB40A | 4 | BDQ42 | T | PB50A | 4 | BDQ51 | T |
| 88 | PB40B | 4 | BDQ42 | C | PB50B | 4 | BDQ51 | C |
| 89 | GND | - | | | GND | - | | |
| 90 | PB42A | 4 | BDQS42 | T | PB52A | 4 | BDQ51 | T |
| 91 | PB42B | 4 | BDQ42 | C | PB52B | 4 | BDQ51 | C |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| L11 | L11 | PB61B | 4 | BDQ60 | C |
| T13 | T13 | PB62A | 4 | BDQ60 | T |
| R13 | R13 | PB63A | 4 | BDQ60 | T |
| VCCIO | VCCIO | VCCIO4 | 4 | | |
| T14 | T14 | PB62B | 4 | BDQ60 | C |
| P13 | P13 | PB63B | 4 | BDQ60 | C |
| GND | GND | GNDIO4 | - | | |
| N12 | N12 | PB64A | 4 | VREF2_4/BDQ60 | T |
| M12 | M12 | PB64B | 4 | VREF1_4/BDQ60 | C |
| R15 | R15 | CFG2 | 8 | | |
| N14 | N14 | CFG1 | 8 | | |
| N13 | N13 | PROGRAMN | 8 | | |
| N15 | N15 | CFG0 | 8 | | |
| P15 | P15 | PR44B | 8 | WRITEN | C |
| L12 | L12 | INITN | 8 | | |
| N16 | N16 | PR43B | 8 | CSN | C |
| GND | GND | GNDIO8 | - | | |
| R14 | R14 | CCLK | 8 | | |
| P14 | P14 | PR44A | 8 | CS1N | T |
| M13 | M13 | DONE | 8 | | |
| R16 | R16 | PR42B | 8 | D1 | C |
| VCCIO | VCCIO | VCCIO8 | 8 | | |
| M16 | M16 | PR43A | 8 | D0/SPIFASTN | T |
| P16 | P16 | PR42A | 8 | D2 | T |
| L15 | L15 | PR41B | 8 | D3 | C |
| GND | GND | GNDIO8 | - | | |
| L14 | L14 | PR40A | 8 | D6 | T |
| L16 | L16 | PR41A | 8 | D4 | T |
| L10 | L10 | PR39B | 8 | D7/SPID0 | C |
| L13 | L13 | PR40B | 8 | D5 | C |
| VCCIO | VCCIO | VCCIO8 | 8 | | |
| K11 | K11 | PR39A | 8 | DI/CSSPI0N | T |
| K14 | K14 | PR38B | 8 | DOUT/CSON | C |
| K13 | K13 | PR38A | 8 | BUSY/SISPI | T |
| GND | GND | GNDIO8 | - | | |
| K15 | K15 | PR31B | 3 | RLM0_GPLLC_FB_A/RDQ34 | C |
| VCCIO | VCCIO | VCCIO3 | 3 | | |
| K16 | K16 | PR31A | 3 | RLM0_GPLLT_FB_A/RDQ34 | T |
| GND | GND | GNDIO3 | - | | |
| J16 | J16 | PR30B | 3 | RLM0_GPLLC_IN_A**/RDQ34 | C (LVDS)* |
| J15 | J15 | PR30A | 3 | RLM0_GPLLT_IN_A**/RDQ34 | T (LVDS)* |
| J14 | J14 | RLM0_PLLCAP | 3 | | |

## LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-20E/SE | | | | | |
|---|---|---|---|---|---|
| Ball Number | Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| A5 | A5 | PT36B | 0 | | C |
| A3 | A3 | PT35B | 0 | | C |
| A4 | A4 | PT36A | 0 | | T |
| VCCIO | VCCIO | VCCIO0 | 0 | | |
| B3 | B3 | PT35A | 0 | | T |
| A2 | A2 | PT34B | 0 | | C |
| C7 | C7 | PT33B | 0 | | C |
| B2 | B2 | PT34A | 0 | | T |
| D7 | D7 | PT33A | 0 | | T |
| D6 | D6 | PT32B | 0 | | C |
| GND | GND | GNDIO0 | - | | |
| F7 | F7 | PT31B | 0 | | C |
| C6 | C6 | PT32A | 0 | | T |
| VCCIO | VCCIO | VCCIO0 | 0 | | |
| F6 | F6 | PT31A | 0 | | T |
| C4 | C4 | PT30B | 0 | | C |
| B4 | B4 | PT30A | 0 | | T |
| - | GND | GNDIO0 | 0 | | |
| - | VCC | VCCIO | 0 | | |
| D5 | D5 | PT2B | 0 | VREF2_0 | C |
| E5 | E5 | PT2A | 0 | VREF1_0 | T |
| G7 | G7 | VCC | - | | |
| G9 | G9 | VCC | - | | |
| H7 | H7 | VCC | - | | |
| J10 | J10 | VCC | - | | |
| K10 | K10 | VCC | - | | |
| K8 | K8 | VCC | - | | |
| G8 | G8 | VCCAUX | - | | |
| H10 | H10 | VCCAUX | - | | |
| J7 | J7 | VCCAUX | - | | |
| K9 | K9 | VCCAUX | - | | |
| C5 | C5 | VCCIO0 | 0 | | |
| E7 | E7 | VCCIO0 | 0 | | |
| C12 | C12 | VCCIO1 | 1 | | |
| E10 | E10 | VCCIO1 | 1 | | |
| E14 | E14 | VCCIO2 | 2 | | |
| G12 | G12 | VCCIO2 | 2 | | |
| K12 | K12 | VCCIO3 | 3 | | |
| M14 | M14 | VCCIO3 | 3 | | |
| M10 | M10 | VCCIO4 | 4 | | |
| P12 | P12 | VCCIO4 | 4 | | |
| M7 | M7 | VCCIO5 | 5 | | |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C20 | PT75B | 1 | | C | PT93B | 1 | | C |
| D20 | PT75A | 1 | | T | PT93A | 1 | | T |
| A22 | PT74B | 1 | | C | PT92B | 1 | | C |
| A21 | PT74A | 1 | | T | PT92A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E19 | PT71B | 1 | | C | PT85B | 1 | | C |
| C19 | PT71A | 1 | | T | PT85A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B21 | PT70B | 1 | | C | PT79B | 1 | | C |
| B20 | PT70A | 1 | | T | PT79A | 1 | | T |
| D19 | PT69B | 1 | | C | PT78B | 1 | | C |
| B19 | PT69A | 1 | | T | PT78A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | PT68B | 1 | | C | PT77B | 1 | | C |
| E18 | PT68A | 1 | | T | PT77A | 1 | | T |
| G19 | PT67B | 1 | | C | PT76B | 1 | | C |
| F17 | PT67A | 1 | | T | PT76A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| A20 | PT66B | 1 | | C | PT75B | 1 | | C |
| A19 | PT66A | 1 | | T | PT75A | 1 | | T |
| E17 | PT65B | 1 | | C | PT74B | 1 | | C |
| D18 | PT65A | 1 | | T | PT74A | 1 | | T |
| B18 | PT64B | 1 | | C | PT73B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| A18 | PT64A | 1 | | T | PT73A | 1 | | T |
| E16 | PT63B | 1 | | C | PT72B | 1 | | C |
| G16 | PT63A | 1 | | T | PT72A | 1 | | T |
| F16 | PT62B | 1 | | C | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H18 | PT62A | 1 | | T | PT71A | 1 | | T |
| A17 | PT61B | 1 | | C | PT70B | 1 | | C |
| B17 | PT61A | 1 | | T | PT70A | 1 | | T |
| C18 | PT60B | 1 | | C | PT69B | 1 | | C |
| B16 | PT60A | 1 | | T | PT69A | 1 | | T |
| C17 | PT59B | 1 | | C | PT68B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D17 | PT59A | 1 | | T | PT68A | 1 | | T |
| E15 | PT58B | 1 | | C | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G15 | PT58A | 1 | | T | PT67A | 1 | | T |
| A16 | PT57B | 1 | | C | PT66B | 1 | | C |
| B15 | PT57A | 1 | | T | PT66A | 1 | | T |
| D15 | PT56B | 1 | | C | PT65B | 1 | | C |
| F15 | PT56A | 1 | | T | PT65A | 1 | | T |
| A14 | PT55B | 1 | | C | PT64B | 1 | | C |
| B14 | PT55A | 1 | | T | PT64A | 1 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| D25 | PT99A | 1 | | T |
| J22 | PT98B | 1 | | C |
| J21 | PT98A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| B25 | PT97B | 1 | | C |
| A25 | PT97A | 1 | | T |
| E24 | PT96B | 1 | | C |
| F24 | PT96A | 1 | | T |
| GND | GNDIO1 | - | | |
| F23 | PT95B | 1 | | C |
| H22 | PT95A | 1 | | T |
| D24 | PT94B | 1 | | C |
| C24 | PT94A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| E23 | PT93B | 1 | | C |
| G23 | PT93A | 1 | | T |
| B24 | PT92B | 1 | | C |
| A24 | PT92A | 1 | | T |
| C27 | PT91B | 1 | | C |
| GND | GNDIO1 | - | | |
| D27 | PT91A | 1 | | T |
| C26 | PT90B | 1 | | C |
| D26 | PT90A | 1 | | T |
| A27 | PT89B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | |
| B27 | PT89A | 1 | | T |
| A28 | PT88B | 1 | | C |
| B28 | PT88A | 1 | | T |
| A29 | PT87B | 1 | | C |
| B29 | PT87A | 1 | | T |
| GND | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| H21 | PT80B | 1 | | C |
| F22 | PT80A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| B23 | PT79B | 1 | | C |
| A23 | PT79A | 1 | | T |
| G24 | PT78B | 1 | | C |
| E22 | PT78A | 1 | | T |
| GND | GNDIO1 | - | | |
| D22 | PT77B | 1 | | C |
| C22 | PT77A | 1 | | T |
| G22 | PT76B | 1 | | C |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA15 | PB42B | 4 | BDQ42 | C | PB60B | 4 | BDQ60 | C |
| V15 | PB43A | 4 | BDQ42 | T | PB61A | 4 | BDQ60 | T |
| U15 | PB43B | 4 | BDQ42 | C | PB61B | 4 | BDQ60 | C |
| AB16 | PB44A | 4 | BDQ42 | T | PB62A | 4 | BDQ60 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA16 | PB44B | 4 | BDQ42 | C | PB62B | 4 | BDQ60 | C |
| AB17 | PB45A | 4 | BDQ42 | T | PB63A | 4 | BDQ60 | T |
| AA17 | PB45B | 4 | BDQ42 | C | PB63B | 4 | BDQ60 | C |
| Y15 | PB46A | 4 | BDQ42 | T | PB64A | 4 | BDQ60 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W15 | PB46B | 4 | BDQ42 | C | PB64B | 4 | BDQ60 | C |
| AB20 | PB47A | 4 | BDQ51 | T | PB65A | 4 | BDQ69 | T |
| AB21 | PB47B | 4 | BDQ51 | C | PB65B | 4 | BDQ69 | C |
| AA21 | PB48A | 4 | BDQ51 | T | PB66A | 4 | BDQ69 | T |
| AA20 | PB48B | 4 | BDQ51 | C | PB66B | 4 | BDQ69 | C |
| AB19 | PB49A | 4 | BDQ51 | T | PB67A | 4 | BDQ69 | T |
| AB18 | PB49B | 4 | BDQ51 | C | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y22 | PB50A | 4 | BDQ51 | T | PB68A | 4 | BDQ69 | T |
| Y21 | PB50B | 4 | BDQ51 | C | PB68B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y17 | PB51A | 4 | BDQS51 | T | PB69A | 4 | BDQS69 | T |
| Y18 | PB51B | 4 | BDQ51 | C | PB69B | 4 | BDQ69 | C |
| Y16 | PB52A | 4 | BDQ51 | T | PB70A | 4 | BDQ69 | T |
| W17 | PB52B | 4 | BDQ51 | C | PB70B | 4 | BDQ69 | C |
| Y19 | PB53A | 4 | BDQ51 | T | PB71A | 4 | BDQ69 | T |
| Y20 | PB53B | 4 | BDQ51 | C | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| W19 | PB54A | 4 | BDQ51 | T | PB72A | 4 | BDQ69 | T |
| W18 | PB54B | 4 | BDQ51 | C | PB72B | 4 | BDQ69 | C |
| V17 | PB55A | 4 | BDQ51 | T | PB73A | 4 | BDQ69 | T |
| V18 | PB55B | 4 | BDQ51 | C | PB73B | 4 | BDQ69 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W20 | CFG2 | 8 | | | CFG2 | 8 | | |
| V20 | CFG1 | 8 | | | CFG1 | 8 | | |
| V19 | CFG0 | 8 | | | CFG0 | 8 | | |
| V22 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| W22 | CCLK | 8 | | | CCLK | 8 | | |
| U18 | INITN | 8 | | | INITN | 8 | | |
| U22 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| U20 | PR53B | 8 | WRITEN*** | C | PR68B | 8 | WRITEN*** | C |
| U21 | PR53A | 8 | CS1N*** | T | PR68A | 8 | CS1N*** | T |
| U17 | PR52B | 8 | CSN*** | C | PR67B | 8 | CSN*** | C |
| U16 | PR52A | 8 | D0/SPIFASTN*** | T | PR67A | 8 | D0/SPIFASTN*** | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| T16 | PR51B | 8 | D1*** | C | PR66B | 8 | D1*** | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| W19 | NC | - | | |
| W18 | NC | - | | |
| V17 | NC | - | | |
| V18 | NC | - | | |
| D15 | NC | - | | |
| G14 | NC | - | | |
| G15 | NC | - | | |
| D14 | NC | - | | |
| E15 | NC | - | | |
| E14 | NC | - | | |
| F15 | NC | - | | |
| F14 | NC | - | | |
| F13 | NC | - | | |
| G12 | NC | - | | |
| G13 | NC | - | | |
| H8 | VCCPLL | - | | |
| H15 | VCCPLL | - | | |
| R8 | VCCPLL | - | | |
| R15 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J13 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 1 | | |
| D18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V13 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T6 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| G2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AC24 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| U17 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J12 | VCCAUX | - | | | VCCAUX | - | | |
| J15 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| M18 | VCCAUX | - | | | VCCAUX | - | | |
| M9 | VCCAUX | - | | | VCCAUX | - | | |
| R18 | VCCAUX | - | | | VCCAUX | - | | |
| R9 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L16 | GND | - | | | GND | - | | |
| L17 | GND | - | | | GND | - | | |
| L2 | GND | - | | | GND | - | | |
| L20 | GND | - | | | GND | - | | |
| L25 | GND | - | | | GND | - | | |
| L7 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M14 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N14 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T2 | GND | - | | | GND | - | | |
| T20 | GND | - | | | GND | - | | |
| T25 | GND | - | | | GND | - | | |
| T7 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| V22 | GND | - | | | GND | - | | |
| V5 | GND | - | | | GND | - | | |
| Y11 | GND | - | | | GND | - | | |
| Y16 | GND | - | | | GND | - | | |
| AB3 | NC | - | | | NC | - | | |
| AB4 | NC | - | | | NC | - | | |
| AC1 | NC | - | | | NC | - | | |
| AC2 | NC | - | | | NC | - | | |
| B4 | NC | - | | | NC | - | | |
| B5 | NC | - | | | NC | - | | |
| C26 | NC | - | | | NC | - | | |
| D20 | NC | - | | | NC | - | | |
| D21 | NC | - | | | NC | - | | |
| D22 | NC | - | | | NC | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L5 | PL23A | 7 | LDQ27 | T (LVDS)* | PL33A | 7 | LDQ37 | T (LVDS)* |
| L4 | PL23B | 7 | LDQ27 | C (LVDS)* | PL33B | 7 | LDQ37 | C (LVDS)* |
| N9 | PL24A | 7 | LDQ27 | T | PL34A | 7 | LDQ37 | T |
| N7 | PL24B | 7 | LDQ27 | C | PL34B | 7 | LDQ37 | C |
| K2 | PL25A | 7 | LDQ27 | T (LVDS)* | PL35A | 7 | LDQ37 | T (LVDS)* |
| K1 | PL25B | 7 | LDQ27 | C (LVDS)* | PL35B | 7 | LDQ37 | C (LVDS)* |
| P9 | PL26A | 7 | LDQ27 | T | PL36A | 7 | LDQ37 | T |
| P7 | PL26B | 7 | LDQ27 | C | PL36B | 7 | LDQ37 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M6 | PL27A | 7 | LDQS27 | T (LVDS)* | PL37A | 7 | LDQS37 | T (LVDS)* |
| M5 | PL27B | 7 | LDQ27 | C (LVDS)* | PL37B | 7 | LDQ37 | C (LVDS)* |
| N5 | PL28A | 7 | LDQ27 | T | PL38A | 7 | LDQ37 | T |
| N6 | PL28B | 7 | LDQ27 | C | PL38B | 7 | LDQ37 | C |
| M4 | PL29A | 7 | LDQ27 | T (LVDS)* | PL39A | 7 | LDQ37 | T (LVDS)* |
| M3 | PL29B | 7 | LDQ27 | C (LVDS)* | PL39B | 7 | LDQ37 | C (LVDS)* |
| P6 | PL30A | 7 | LDQ27 | T | PL40A | 7 | LDQ37 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P8 | PL30B | 7 | LDQ27 | C | PL40B | 7 | LDQ37 | C |
| L3 | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T (LVDS)* | PL42A | 7 | LUM3_SPLLT_IN_A/LDQ46 | T (LVDS)* |
| L2 | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C (LVDS)* | PL42B | 7 | LUM3_SPLLC_IN_A/LDQ46 | C (LVDS)* |
| P5 | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T | PL43A | 7 | LUM3_SPLLT_FB_A/LDQ46 | T |
| P4 | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C | PL43B | 7 | LUM3_SPLLC_FB_A/LDQ46 | C |
| L1 | PL34A | 7 | LDQ36 | T (LVDS)* | PL44A | 7 | LDQ46 | T (LVDS)* |
| M2 | PL34B | 7 | LDQ36 | C (LVDS)* | PL44B | 7 | LDQ46 | C (LVDS)* |
| R5 | PL35A | 7 | LDQ36 | T | PL45A | 7 | LDQ46 | T |
| R4 | PL35B | 7 | LDQ36 | C | PL45B | 7 | LDQ46 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| M1 | PL36A | 7 | LDQS36 | T (LVDS)* | PL46A | 7 | LDQS46 | T (LVDS)* |
| N2 | PL36B | 7 | LDQ36 | C (LVDS)* | PL46B | 7 | LDQ46 | C (LVDS)* |
| R8 | PL37A | 7 | LDQ36 | T | PL47A | 7 | LDQ46 | T |
| T9 | PL37B | 7 | LDQ36 | C | PL47B | 7 | LDQ46 | C |
| P3 | PL38A | 7 | LDQ36 | T (LVDS)* | PL48A | 7 | LDQ46 | T (LVDS)* |
| P2 | PL38B | 7 | LDQ36 | C (LVDS)* | PL48B | 7 | LDQ46 | C (LVDS)* |
| N1 | PL39A | 7 | PCLKT7_0/LDQ36 | T | PL49A | 7 | PCLKT7_0/LDQ46 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| P1 | PL39B | 7 | PCLKC7_0/LDQ36 | C | PL49B | 7 | PCLKC7_0/LDQ46 | C |
| T5 | PL41A | 6 | PCLKT6_0 | T (LVDS)* | PL51A | 6 | PCLKT6_0/LDQ55 | T (LVDS)* |
| T4 | PL41B | 6 | PCLKC6_0 | C (LVDS)* | PL51B | 6 | PCLKC6_0/LDQ55 | C (LVDS)* |
| U7 | PL42A | 6 | VREF2_6 | T | PL52A | 6 | VREF2_6/LDQ55 | T |
| T8 | PL42B | 6 | VREF1_6 | C | PL52B | 6 | VREF1_6/LDQ55 | C |
| R3 | PL43A | 6 | | T (LVDS)* | PL53A | 6 | LDQ55 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | PL43B | 6 | | C (LVDS)* | PL53B | 6 | LDQ55 | C (LVDS)* |
| R1 | PL44A | 6 | | T | PL54A | 6 | LDQ55 | T |
| T1 | PL44B | 6 | | C | PL54B | 6 | LDQ55 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| - | - | - | | | VCCIO6 | 6 | | |
| T3 | PL45A | 6 | LLM3_SPLLT_IN_A | T (LVDS)* | PL57A | 6 | LLM3_SPLLT_IN_A/LDQ55 | T (LVDS)* |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P16 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| P18 | GND | - | | | GND | - | | |
| P20 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R11 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| R15 | GND | - | | | GND | - | | |
| R16 | GND | - | | | GND | - | | |
| R17 | GND | - | | | GND | - | | |
| R18 | GND | - | | | GND | - | | |
| R20 | GND | - | | | GND | - | | |
| R21 | GND | - | | | GND | - | | |
| R24 | GND | - | | | GND | - | | |
| R7 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T13 | GND | - | | | GND | - | | |
| T14 | GND | - | | | GND | - | | |
| T15 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T18 | GND | - | | | GND | - | | |
| T20 | GND | - | | | GND | - | | |
| T21 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T7 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U15 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U18 | GND | - | | | GND | - | | |
| U20 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V15 | GND | - | | | GND | - | | |
| V16 | GND | - | | | GND | - | | |
| V17 | GND | - | | | GND | - | | |
| V27 | GND | - | | | GND | - | | |
| V4 | GND | - | | | GND | - | | |
| W23 | GND | - | | | GND | - | | |
| W8 | GND | - | | | GND | - | | |
| Y14 | GND | - | | | GND | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| M23 | GND | - | | |
| M8 | GND | - | | |
| N14 | GND | - | | |
| N15 | GND | - | | |
| N16 | GND | - | | |
| N17 | GND | - | | |
| N27 | GND | - | | |
| N4 | GND | - | | |
| P11 | GND | - | | |
| P13 | GND | - | | |
| P14 | GND | - | | |
| P15 | GND | - | | |
| P16 | GND | - | | |
| P17 | GND | - | | |
| P18 | GND | - | | |
| P20 | GND | - | | |
| R10 | GND | - | | |
| R11 | GND | - | | |
| R13 | GND | - | | |
| R14 | GND | - | | |
| R15 | GND | - | | |
| R16 | GND | - | | |
| R17 | GND | - | | |
| R18 | GND | - | | |
| R20 | GND | - | | |
| R21 | GND | - | | |
| R24 | GND | - | | |
| R7 | GND | - | | |
| T10 | GND | - | | |
| T11 | GND | - | | |
| T13 | GND | - | | |
| T14 | GND | - | | |
| T15 | GND | - | | |
| T16 | GND | - | | |
| T17 | GND | - | | |
| T18 | GND | - | | |
| T20 | GND | - | | |
| T21 | GND | - | | |
| T24 | GND | - | | |
| T7 | GND | - | | |
| U11 | GND | - | | |
| U13 | GND | - | | |
| U14 | GND | - | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E4 | NC | - | | | NC | - | | |
| E9 | NC | - | | | NC | - | | |
| F10 | NC | - | | | NC | - | | |
| F25 | NC | - | | | NC | - | | |
| F26 | NC | - | | | NC | - | | |
| F27 | NC | - | | | NC | - | | |
| F28 | NC | - | | | NC | - | | |
| F29 | NC | - | | | NC | - | | |
| F30 | NC | - | | | NC | - | | |
| F31 | NC | - | | | NC | - | | |
| F32 | NC | - | | | NC | - | | |
| F33 | NC | - | | | NC | - | | |
| F34 | NC | - | | | NC | - | | |
| F5 | NC | - | | | NC | - | | |
| F6 | NC | - | | | NC | - | | |
| F7 | NC | - | | | NC | - | | |
| F8 | NC | - | | | NC | - | | |
| F9 | NC | - | | | NC | - | | |
| G10 | NC | - | | | NC | - | | |
| G11 | NC | - | | | NC | - | | |
| G24 | NC | - | | | NC | - | | |
| G25 | NC | - | | | NC | - | | |
| G26 | NC | - | | | NC | - | | |
| G27 | NC | - | | | NC | - | | |
| G28 | NC | - | | | NC | - | | |
| G29 | NC | - | | | NC | - | | |
| G30 | NC | - | | | NC | - | | |
| G33 | NC | - | | | NC | - | | |
| G34 | NC | - | | | NC | - | | |
| G7 | NC | - | | | NC | - | | |
| G8 | NC | - | | | NC | - | | |
| G9 | NC | - | | | NC | - | | |
| H10 | NC | - | | | NC | - | | |
| H11 | NC | - | | | NC | - | | |
| H24 | NC | - | | | NC | - | | |
| H25 | NC | - | | | NC | - | | |
| H26 | NC | - | | | NC | - | | |
| H27 | NC | - | | | NC | - | | |
| H28 | NC | - | | | NC | - | | |
| H29 | NC | - | | | NC | - | | |
| H8 | NC | - | | | NC | - | | |
| H9 | NC | - | | | NC | - | | |
| J10 | NC | - | | | NC | - | | |
| J11 | NC | - | | | NC | - | | |
| J24 | NC | - | | | NC | - | | |
| J25 | NC | - | | | NC | - | | |
| J26 | NC | - | | | NC | - | | |
| J9 | NC | - | | | NC | - | | |
| K10 | NC | - | | | NC | - | | |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5FN1152C | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-6FN1152C | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-7FN1152C | 520 | 1.2V | -7 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 100 |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2006 (cont.) | 01.1 (cont.) | Pinout Information (cont.) | Added Information on: Available Device Resources per Packaged Device table. |
| | | Ordering Information | Updated ordering part number table to include ECP2-12. |
| | | | Updated topside mark drawing. |
| September 2006 | 02.0 | Multiple | Added information regarding LatticeECP2M support throughout. |
| September 2006 | 02.1 | DC and Switching Characteristics | Added Receiver Total Jitter Tolerance Specification table. |
| | | | Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table. |
| December 2006 | 02.2 | Introduction | LatticeECP2M Selection Guide table has been updated. |
| | | Architecture | Figure 2-16. Per Region Secondary Clock Selection has been updated. |
| | | | Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated. |
| | | DC and Switching | Footnotes have been added to Recommended Operating Conditions. |
| | | | DC Electrical Characteristics table has been updated. |
| | | | Supply Current (Standby) tables have been updated. |
| | | | Initialization Supply Current table have been updated. |
| | | | Updated timing numbers to include LFE2-12E (rev A 0.08). |
| | | Pinout Information | Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E. |
| | | Ordering Information | Updated to include the entire ECP2 and ECP2M device ordering information. |
| February 2007 | 02.3 | Architecture | Updated EBR Asynchronous Reset section. |
| March 2007 | 02.4 | DC and Switching Characteristics | Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz. |
| March 2007 | 02.5 | Introduction | Added “Security Series” to the LatticeECP2 and LatticeECP2M families. |
| | | Architecture | Enhanced Configuration Option section updated. |
| | | DC and Switching | Recommended Operating Conditions table - footnote 4 updated. |
| | | Ordering Information | “Security Series” ordering part numbers added. |
| April 2007 | 02.6 | Introduction | LatticeECP2M family table has been updated for user I/O counts. |
| | | Ordering Information | LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100. |
| July 2007 | 02.7 | Architecture | Updated text in Ripple Mode section. |
| | | DC and Switching | ECP2/M Supply Current information has been updated.<br>Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10).<br>SERDES timing information has been updated.<br>PCI Express timing information has been updated. |
| | | Pinout Information | Added LatticeECP2M20 pinout information. |
| August 2007 | 02.8 | Introduction | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| | | Architecture | Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated. |
| | | DC and Switching | Supply Current (Standby) table has been updated. |
| | | | DSP Function timing has been updated. |