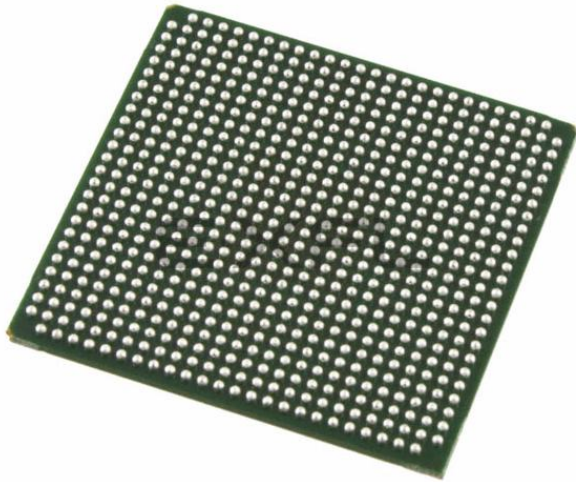




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

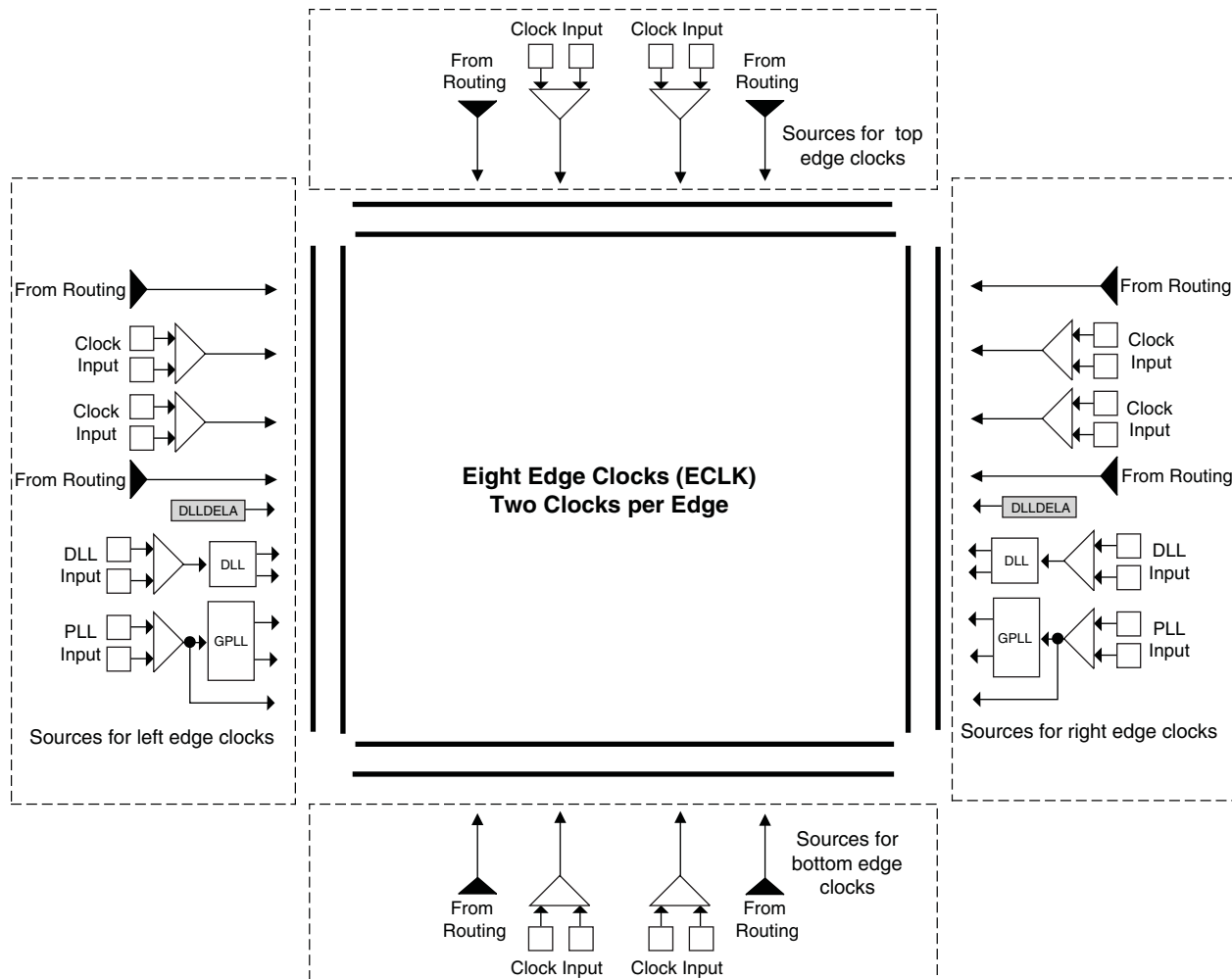
Details

Product Status	Obsolete
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-5f672i

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

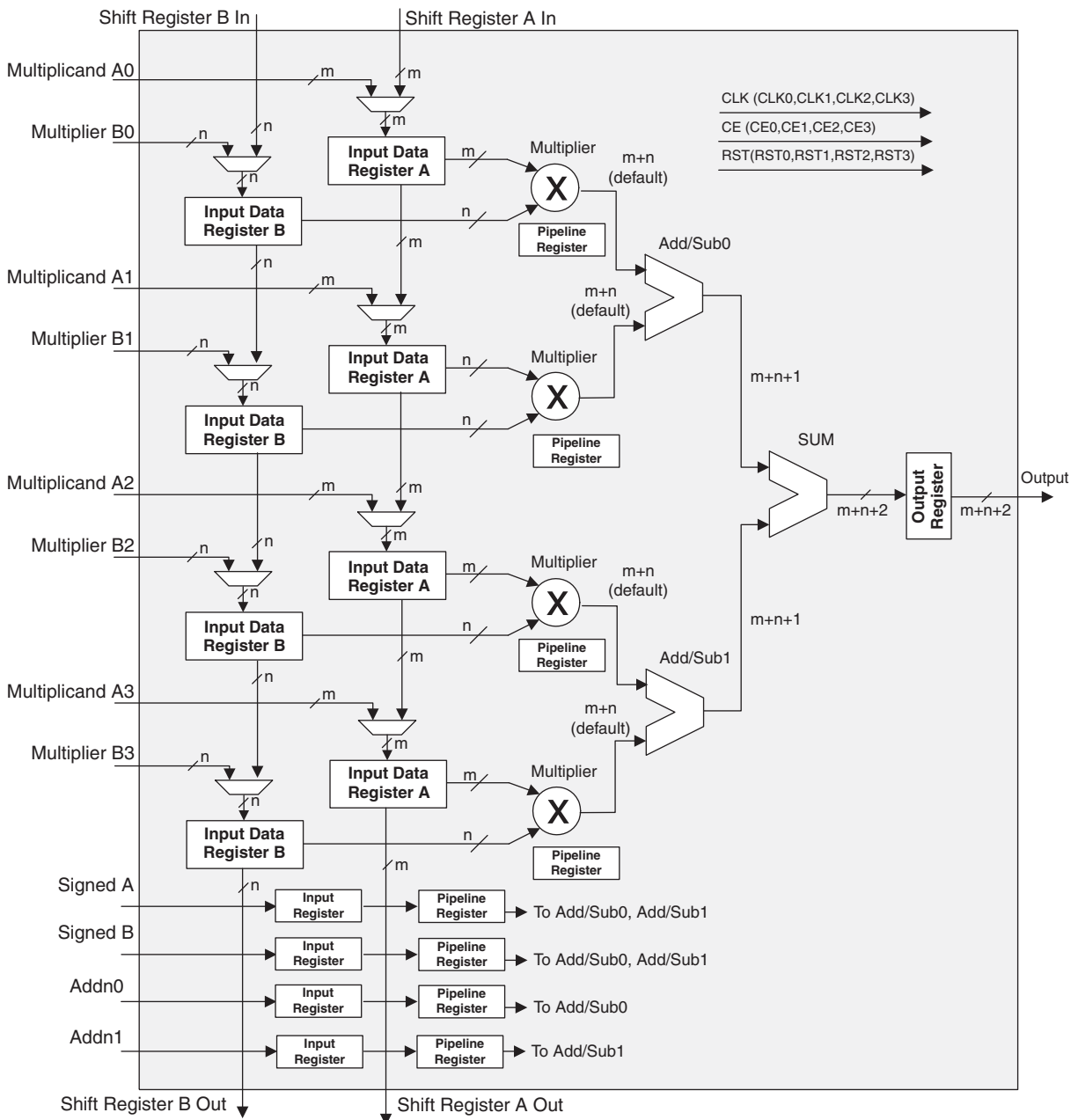
Figure 2-12. Edge Clock Sources



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

Figure 2-26. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

LatticeECP2 Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply Current	ECP2-6	10	mA
		ECP2-12	20	mA
		ECP2-20	30	mA
		ECP2-35	50	mA
		ECP2-50	70	mA
		ECP2-70	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	24	mA
		ECP2-12	24	mA
		ECP2-20	24	mA
		ECP2-35	24	mA
		ECP2-50	24	mA
		ECP2-70	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2-6	2	mA
		ECP2-12	2	mA
		ECP2-20	2	mA
		ECP2-35	2	mA
		ECP2-50	2	mA
		ECP2-70	2	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a "blank" configuration data file.
5. $T_J = 25^\circ\text{C}$, power supplies at normal voltage.

sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3 ²	3.135	3.3	3.465	—	—	—
LVC MOS 2.5 ²	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2 ²	1.14	1.2	1.26	—	—	—
LVTTL ²	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 ² Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 ² Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 ² Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL ² 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL ² 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS ²	2.375	2.5	2.625	—	—	—
MLVDS25 ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1,2}	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1,2}	2.375	2.5	2.625	—	—	—
RSDS ^{1,2}	2.375	2.5	2.625	—	—	—
SSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of V_{CCIO}.

LatticeECP2/M External Switching Characteristics⁹

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL) ¹									
t _{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

LatticeECP2 Power Supply and NC

Signals	144 TQFP ³	208 PQFP ³	256 fpBGA ⁴	484 fpBGA ⁴
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	LFE2-6: G7, G9, G10, H7, J10, K10, K8 LFE2-12/LFE2-20: G7, G9, G10, H7, J10, K10, K8	LFE2-12/LFE2-20: N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 LFE2-35/LFE2-50: J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	LFE2-12/LFE2-20: None LFE2-35: N6, N18 LFE2-50: N6, N18, K6, J16
GND ¹	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC ²	LFE2-6: 45, 46, 124, 127 LFE2-12: 127	None	LFE2-6: K6, R3, P4 LFE2-12/LFE2-20: None	LFE2-12: E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-20/LFE2-35: K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-50: None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
136	PT6B	0		C	PT16B	0		C
137	PT6A	0		T	PT16A	0		T
138	GND	-			GND	-		
139	VCCIO0	0			VCCIO0	0		
140	PT4B	0		C	PT6B	0		C
141	PT4A	0		T	PT6A	0		T
142	VCCAUX	-			VCCAUX	-		
143	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
144	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one-to-one connection with a package ball or pin.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO6	-			GNDIO6	-		
L2	PL24A	6	LDQ28	T (LVDS)*	PL24A	6	LDQ28	T (LVDS)*
K2	PL25A	6	LDQ28	T	PL25A	6	LDQ28	T
L3	PL24B	6	LDQ28	C (LVDS)*	PL24B	6	LDQ28	C (LVDS)*
K1	PL25B	6	LDQ28	C	PL25B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
L4	PL26A	6	LDQ28	T (LVDS)*	PL26A	6	LDQ28	T (LVDS)*
L1	PL27A	6	LDQ28	T	PL27A	6	LDQ28	T
L5	PL26B	6	LDQ28	C (LVDS)*	PL26B	6	LDQ28	C (LVDS)*
M1	PL27B	6	LDQ28	C	PL27B	6	LDQ28	C
GND	GNDIO6	-			GNDIO6	-		
N1	PL29A	6	LDQ28	T	PL29A	6	LDQ28	T
N2	PL28A	6	LDQS28	T (LVDS)*	PL28A	6	LDQS28	T (LVDS)*
P1	PL29B	6	LDQ28	C	PL29B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL28B	6	LDQ28	C (LVDS)*	PL28B	6	LDQ28	C (LVDS)*
R1	PL30A	6	LDQ28	T (LVDS)*	PL30A	6	LDQ28	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
R2	PL30B	6	LDQ28	C (LVDS)*	PL30B	6	LDQ28	C (LVDS)*
N4	TDI	-			TDI	-		
M4	TCK	-			TCK	-		
P3	TDO	-			TDO	-		
N3	TMS	-			TMS	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
K6	NC	-			PB3A	5	BDQ6	
M6	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
R3	NC	-			PB5A	5	BDQ6	T
P4	NC	-			PB5B	5	BDQ6	C
-	-	-			VCCIO	5		
-	-	-			GNDIO5	5		
N5	PB3A	5	BDQ6	T	PB21A	5	BDQ24	T
N6	PB3B	5	BDQ6	C	PB21B	5	BDQ24	C
T2	PB4A	5	BDQ6	T	PB22A	5	BDQ24	T
P6	PB5A	5	BDQ6	T	PB23A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB4B	5	BDQ6	C	PB22B	5	BDQ24	C
R6	PB5B	5	BDQ6	C	PB23B	5	BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
R4	PB6A	5	BDQS6	T	PB24A	5	BDQS24	T
L6	PB7A	5	BDQ6	T	PB25A	5	BDQ24	T
T4	PB6B	5	BDQ6	C	PB24B	5	BDQ24	C
L7	PB7B	5	BDQ6	C	PB25B	5	BDQ24	C
N7	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P5	P5	VCCIO5	5		
K5	K5	VCCIO6	6		
M3	M3	VCCIO6	6		
E3	E3	VCCIO7	7		
G5	G5	VCCIO7	7		
T15	T15	VCCIO8	8		
A1	A1	GND	-		
A16	A16	GND	-		
B12	B12	GND	-		
B5	B5	GND	-		
C8	C8	GND	-		
E15	E15	GND	-		
E2	E2	GND	-		
H14	H14	GND	-		
H8	H8	GND	-		
H9	H9	GND	-		
J3	J3	GND	-		
J8	J8	GND	-		
J9	J9	GND	-		
M15	M15	GND	-		
M2	M2	GND	-		
P9	P9	GND	-		
R12	R12	GND	-		
R5	R5	GND	-		
T1	T1	GND	-		
T16	T16	GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
AB19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AE19	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AA17	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	
AF18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T	
AF19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T	
W17	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C	
Y19	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
Y17	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
AF20	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
AA20	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
W18	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
AD20	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
GND	GNDIO4	-			GNDIO4	-			
AE21	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
AF21	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
AF22	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T	
AD22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C	
AF23	PB75A	4	BDQ78	T	PB93A	4	BDQ96	T	
AE23	PB75B	4	BDQ78	C	PB93B	4	BDQ96	C	
AD23	PB76A	4	BDQ78	T	PB94A	4	BDQ96	T	
AC23	PB76B	4	BDQ78	C	PB94B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T	
AC20	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T	
AC22	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C	
W19	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T	
AA21	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C	
AF24	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T	
AE24	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T	
AB22	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AH12	PB45A	5	BDQ42	T
AF14	PB45B	5	BDQ42	C
AJ13	PB46A	5	BDQ42	T
GND	GNDIO5	-		
AK13	PB46B	5	BDQ42	C
AB15	PB47A	5	BDQ51	T
AD15	PB47B	5	BDQ51	C
AE15	PB48A	5	BDQ51	T
AF15	PB48B	5	BDQ51	C
AG15	PB49A	5	BDQ51	T
AG14	PB49B	5	BDQ51	C
VCCIO	VCCIO5	5		
AH15	PB50A	5	BDQ51	T
AH14	PB50B	5	BDQ51	C
GND	GNDIO5	-		
AJ14	PB51A	5	BDQS51	T
AK14	PB51B	5	BDQ51	C
AD16	PB52A	5	BDQ51	T
AF16	PB52B	5	BDQ51	C
AJ15	PB53A	5	PCLKT5_0/BDQ51	T
AK15	PB53B	5	PCLKC5_0/BDQ51	C
VCCIO	VCCIO5	5		
GND	GNDIO5	-		
AE16	PB58A	4	PCLKT4_0/BDQ60	T
VCCIO	VCCIO4	4		
AC15	PB58B	4	PCLKC4_0/BDQ60	C
AJ16	PB59A	4	BDQ60	T
AK16	PB59B	4	BDQ60	C
AC16	PB60A	4	BDQS60	T
GND	GNDIO4	-		
AB16	PB60B	4	BDQ60	C
AH17	PB61A	4	BDQ60	T
AG17	PB61B	4	BDQ60	C
AF17	PB62A	4	BDQ60	T
VCCIO	VCCIO4	4		
AD17	PB62B	4	BDQ60	C
AE17	PB63A	4	BDQ60	T
AC17	PB63B	4	BDQ60	C
AJ17	PB64A	4	BDQ60	T
GND	GNDIO4	-		
AK17	PB64B	4	BDQ60	C
AK18	PB65A	4	BDQ69	T
AJ18	PB65B	4	BDQ69	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
V23	PR70A	3	RDQ71	T
W27	PR69B	3	RDQ71	C (LVDS)*
W28	PR69A	3	RDQ71	T (LVDS)*
V26	PR68B	3	RDQ71	C
VCCIO	VCCIO3	3		
V24	PR68A	3	RDQ71	T
W29	PR67B	3	RDQ71	C (LVDS)*
W30	PR67A	3	RDQ71	T (LVDS)*
U25	PR66B	3	RDQ63	C
GND	GNDIO3	-		
U23	PR66A	3	RDQ63	T
V29	PR65B	3	RDQ63	C (LVDS)*
V30	PR65A	3	RDQ63	T (LVDS)*
U26	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
U24	PR64A	3	RDQ63	T
U27	PR63B	3	RDQ63	C (LVDS)*
U28	PR63A	3	RDQS63	T (LVDS)*
GND	GNDIO3	-		
T23	PR62B	3	RDQ63	C
T25	PR62A	3	RDQ63	T
U29	PR61B	3	RDQ63	C (LVDS)*
U30	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
T24	PR60B	3	VREF2_3/RDQ63	C
T26	PR60A	3	VREF1_3/RDQ63	T
T27	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
T28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
R24	PR57B	2	PCLKC2_0/RDQ54	C
R26	PR57A	2	PCLKT2_0/RDQ54	T
GND	GNDIO2	-		
T29	PR56B	2	RDQ54	C (LVDS)*
T30	PR56A	2	RDQ54	T (LVDS)*
R23	PR55B	2	RDQ54	C
R25	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
R27	PR54B	2	RDQ54	C (LVDS)*
R28	PR54A	2	RDQS54	T (LVDS)*
P26	PR53B	2	RDQ54	C
GND	GNDIO2	-		
P24	PR53A	2	RDQ54	T
R29	PR52B	2	RDQ54	C (LVDS)*
R30	PR52A	2	RDQ54	T (LVDS)*

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A2	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*	
B2	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C (LVDS)*	
D3	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T	
C2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C	
E4	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
E5	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C (LVDS)*	
B1	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T	
C1	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C	
D2	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO7	-			
D1	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C (LVDS)*	
E1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T	
F1	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F3	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*	
F2	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C (LVDS)*	
F6	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T	
F5	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C	
GNDIO	GNDIO7	-			GNDIO7	-			
G4	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	
G3	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	
G1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	
G2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	
H1	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
J1	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*	
H2	PL14A	7		T	PL14A	7	LDQ15	T	
H3	PL14B	7		C	PL14B	7	LDQ15	C	
GNDIO	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
G6	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*	
H6	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*	
J2	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T	
GNDIO	GNDIO7	-			GNDIO7	-			
K1	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C	
H4	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*	
H5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*	
J4	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T	
K4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C	
VCCIO	VCCIO6	6			VCCIO6	6			
J6	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
J5	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*	
K3	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T	
K2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
T1	PL65A	6	LLM0_GDLLT_FB_A	T
T2	PL65B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	-		
R7	LLM0_PLLCAP	6		
T6	PL67A	6	LDQ71	T (LVDS)*
T7	PL67B	6	LDQ71	C (LVDS)*
U1	PL68A	6	LDQ71	T
U2	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
T3	PL69A	6	LDQ71	T (LVDS)*
U3	PL69B	6	LDQ71	C (LVDS)*
U6	PL70A	6	LDQ71	T
U5	PL70B	6	LDQ71	C
GNDIO	GNDIO6	-		
V5	PL71A	6	LDQS71	T (LVDS)*
U4	PL71B	6	LDQ71	C (LVDS)*
V1	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		
V3	PL72B	6	LDQ71	C
W1	PL73A	6	LDQ71	T (LVDS)*
Y1	PL73B	6	LDQ71	C (LVDS)*
AA1	PL74A	6	LDQ71	T
GNDIO	GNDIO6	-		
AA2	PL74B	6	LDQ71	C
V4	TCK	-		
Y2	TDI	-		
Y3	TMS	-		
W3	TDO	-		
W4	VCCJ	-		
W5	PB2A	5	BDQ6	T
Y4	PB2B	5	BDQ6	C
W6	PB3A	5	BDQ6	T
V6	PB3B	5	BDQ6	C
AA3	PB4A	5	BDQ6	T
AB2	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5		
T8	PB5A	5	BDQ6	T
U7	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-		
U8	PB6A	5	BDQS6	T
T9	PB6B	5	BDQ6	C
V8	PB7A	5	BDQ6	T
W8	PB7B	5	BDQ6	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J11	VCC	-		
J12	VCC	-		
J13	VCC	-		
K14	VCC	-		
K9	VCC	-		
L14	VCC	-		
L9	VCC	-		
M14	VCC	-		
M9	VCC	-		
N14	VCC	-		
N9	VCC	-		
P10	VCC	-		
P11	VCC	-		
P12	VCC	-		
P13	VCC	-		
B5	VCCIO0	0		
B9	VCCIO0	0		
E7	VCCIO0	0		
H9	VCCIO0	0		
D13	VCCIO1	1		
E16	VCCIO1	1		
H14	VCCIO1	1		
E21	VCCIO2	2		
G18	VCCIO2	2		
J15	VCCIO2	2		
K19	VCCIO2	2		
N19	VCCIO3	3		
P15	VCCIO3	3		
T18	VCCIO3	3		
V21	VCCIO3	3		
AA18	VCCIO4	4		
R14	VCCIO4	4		
V16	VCCIO4	4		
W13	VCCIO4	4		
AA5	VCCIO5	5		
R9	VCCIO5	5		
V7	VCCIO5	5		
W10	VCCIO5	5		
N4	VCCIO6	6		
P8	VCCIO6	6		
T5	VCCIO6	6		
V2	VCCIO6	6		
E2	VCCIO7	7		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			VCCIO2	2			
H23	NC	-			PR15B	2	RDQ15	C (LVDS)*	
H24	NC	-			PR15A	2	RDQS15	T (LVDS)*	
D28	NC	-			PR14B	2	RDQ15	C	
-	-	-			GNDIO2	-			
E28	NC	-			PR14A	2	RDQ15	T	
G24	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
H25	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
D27	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
GNDIO	GNDIO2	-			VCCIO2	2			
E27	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	
G25	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
F24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
VCCIO	VCCIO2	-			-	-			
GNDIO	GNDIO2	-			GNDIO2	-			
F25	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G23	XRES	-			XRES	1			
C30	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A29	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B30	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B29	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C27	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A26	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A27	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B26	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C26	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B25	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C25	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A25	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C29	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B28	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C28	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A28	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B24	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E24	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D24	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C24	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A20	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	
C20	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B20	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C19	URC_SQ_VCCR_X2	12			URC_SQ_VCCR_X2	12			
A23	URC_SQ_HDOUT_P2	12		T	URC_SQ_HDOUT_P2	12		T	
C23	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B23	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C22	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B22	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E13	PT28A	0		T	PT37A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
GNDIO	GNDIO0	-			GNDIO0	-			
J12	PT5B	0		C	PT31B	0		C	
GNDIO	GNDIO0	-			-	-			
VCCIO	VCCIO0	0			VCCIO0	0			
H10	PT5A	0		T	PT31A	0		T	
E12	PT4B	0		C	PT30B	0		C	
D11	PT4A	0		T	PT30A	0		T	
H11	PT3B	0		C	PT29B	0		C	
F11	PT3A	0		T	PT29A	0		T	
C13	VCC	-			ULC_SQ_VCCR0	11			
A12	PT19A	0		T	ULC_SQ_HDINP0	11		T	
B13	NC	-			ULC_SQ_VCCIB0	11			
B12	PT19B	0		C	ULC_SQ_HDINN0	11		C	
C10	VCC	-			ULC_SQ_VCCTX0	11			
A9	PT17A	0		T	ULC_SQ_HDOUTP0	11		T	
A10	NC	-			ULC_SQ_VCCOB0	11			
B9	PT17B	0		C	ULC_SQ_HDOUTN0	11		C	
C9	VCC	-			ULC_SQ_VCCTX1	11			
B8	PT18B	0		C	ULC_SQ_HDOUTN1	11		C	
C8	NC	-			ULC_SQ_VCCOB1	11			
A8	PT18A	0		T	ULC_SQ_HDOUTP1	11		T	
C12	VCC	-			ULC_SQ_VCCR1	11			
B11	PT16B	0		C	ULC_SQ_HDINN1	11		C	
C11	NC	-			ULC_SQ_VCCIB1	11			
A11	PT16A	0		T	ULC_SQ_HDINP1	11		T	
B7	VCCAUX	-			ULC_SQ_VCCAUX33	11			
E7	PT15B	0		C	ULC_SQ_REFCLKN	11		C	
D7	PT15A	0		T	ULC_SQ_REFCLKP	11		T	
C7	VCC	-			ULC_SQ_VCCP	11			
A3	PT12A	0		T	ULC_SQ_HDINP2	11		T	
C3	NC	-			ULC_SQ_VCCIB2	11			
B3	PT12B	0		C	ULC_SQ_HDINN2	11		C	
C2	VCC	-			ULC_SQ_VCCR2	11			
A6	PT14A	0		T	ULC_SQ_HDOUTP2	11		T	
C6	NC	-			ULC_SQ_VCCOB2	11			
B6	PT14B	0		C	ULC_SQ_HDOUTN2	11		C	
C5	VCC	-			ULC_SQ_VCCTX2	11			
B5	PT13B	0		C	ULC_SQ_HDOUTN3	11		C	
A4	NC	-			ULC_SQ_VCCOB3	11			
A5	PT13A	0		T	ULC_SQ_HDOUTP3	11		T	
C4	VCC	-			ULC_SQ_VCCTX3	11			
B2	PT11B	0		C	ULC_SQ_HDINN3	11		C	
B1	NC	-			ULC_SQ_VCCIB3	11			
A2	PT11A	0		T	ULC_SQ_HDINP3	11		T	
C1	VCC	-			ULC_SQ_VCCR3	11			
L12	VCC	-			VCC	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K13	VCCIO0	0			VCCIO0	0			
D17	VCCIO1	1			VCCIO1	1			
E22	VCCIO1	1			VCCIO1	1			
E25	VCCIO1	1			VCCIO1	1			
F19	VCCIO1	1			VCCIO1	1			
K18	VCCIO1	1			VCCIO1	1			
K19	VCCIO1	1			VCCIO1	1			
F28	VCCIO2	2			VCCIO2	2			
J25	VCCIO2	2			VCCIO2	2			
K28	VCCIO2	2			VCCIO2	2			
M21	VCCIO2	2			VCCIO2	2			
M24	VCCIO2	2			VCCIO2	2			
N21	VCCIO2	2			VCCIO2	2			
N28	VCCIO2	2			VCCIO2	2			
P21	VCCIO2	2			VCCIO2	2			
R25	VCCIO2	2			VCCIO2	2			
AA28	VCCIO3	3			VCCIO3	3			
AB25	VCCIO3	3			VCCIO3	3			
AE28	VCCIO3	3			VCCIO3	3			
T25	VCCIO3	3			VCCIO3	3			
U21	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
V28	VCCIO3	3			VCCIO3	3			
W21	VCCIO3	3			VCCIO3	3			
W24	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
AA19	VCCIO4	4			VCCIO4	4			
AE19	VCCIO4	4			VCCIO4	4			
AF22	VCCIO4	4			VCCIO4	4			
AG17	VCCIO4	4			VCCIO4	4			
AG25	VCCIO4	4			VCCIO4	4			
AA12	VCCIO5	5			VCCIO5	5			
AA13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AF9	VCCIO5	5			VCCIO5	5			
AG14	VCCIO5	5			VCCIO5	5			
AG6	VCCIO5	5			VCCIO5	5			
AA3	VCCIO6	6			VCCIO6	6			
AB6	VCCIO6	6			VCCIO6	6			
AE3	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
U10	VCCIO6	6			VCCIO6	6			
V10	VCCIO6	6			VCCIO6	6			
V3	VCCIO6	6			VCCIO6	6			
W10	VCCIO6	6			VCCIO6	6			
W7	VCCIO6	6			VCCIO6	6			
F3	VCCIO7	7			VCCIO7	7			
J6	VCCIO7	7			VCCIO7	7			

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK12	NC	-			NC	-		
AK24	NC	-			NC	-		
AK25	NC	-			NC	-		
AK26	NC	-			NC	-		
AK4	NC	-			NC	-		
AK9	NC	-			NC	-		
AL11	NC	-			NC	-		
AL12	NC	-			NC	-		
AL34	NC	-			NC	-		
AM10	NC	-			NC	-		
AM11	NC	-			NC	-		
AM13	NC	-			NC	-		
AM25	NC	-			NC	-		
AN10	NC	-			NC	-		
AN11	NC	-			NC	-		
AN12	NC	-			NC	-		
AN13	NC	-			NC	-		
AN24	NC	-			NC	-		
AN25	NC	-			NC	-		
AP11	NC	-			NC	-		
AP12	NC	-			NC	-		
AP24	NC	-			NC	-		
B10	NC	-			NC	-		
B11	NC	-			NC	-		
B12	NC	-			NC	-		
B13	NC	-			NC	-		
B22	NC	-			NC	-		
B23	NC	-			NC	-		
B24	NC	-			NC	-		
B25	NC	-			NC	-		
C10	NC	-			NC	-		
C11	NC	-			NC	-		
C13	NC	-			NC	-		
C22	NC	-			NC	-		
C24	NC	-			NC	-		
C25	NC	-			NC	-		
D1	NC	-			NC	-		
D15	NC	-			NC	-		
D24	NC	-			NC	-		
D34	NC	-			NC	-		
E10	NC	-			NC	-		
E24	NC	-			NC	-		
E25	NC	-			NC	-		
E26	NC	-			NC	-		
E3	NC	-			NC	-		
E31	NC	-			NC	-		
E32	NC	-			NC	-		
E33	NC	-			NC	-		
E34	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484C	304	1.2V	-5	fpBGA	484	Com	20
LFE2M20SE-6F484C	304	1.2V	-6	fpBGA	484	Com	20
LFE2M20SE-7F484C	304	1.2V	-7	fpBGA	484	Com	20
LFE2M20SE-5F256C	140	1.2V	-5	fpBGA	256	Com	20
LFE2M20SE-6F256C	140	1.2V	-6	fpBGA	256	Com	20
LFE2M20SE-7F256C	140	1.2V	-7	fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672C	410	1.2V	-5	fpBGA	672	Com	35
LFE2M35SE-6F672C	410	1.2V	-6	fpBGA	672	Com	35
LFE2M35SE-7F672C	410	1.2V	-7	fpBGA	672	Com	35
LFE2M35SE-5F484C	303	1.2V	-5	fpBGA	484	Com	35
LFE2M35SE-6F484C	303	1.2V	-6	fpBGA	484	Com	35
LFE2M35SE-7F484C	303	1.2V	-7	fpBGA	484	Com	35
LFE2M35SE-5F256C	140	1.2V	-5	fpBGA	256	Com	35
LFE2M35SE-6F256C	140	1.2V	-6	fpBGA	256	Com	35
LFE2M35SE-7F256C	140	1.2V	-7	fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900C	410	1.2V	-5	fpBGA	900	Com	50
LFE2M50SE-6F900C	410	1.2V	-6	fpBGA	900	Com	50
LFE2M50SE-7F900C	410	1.2V	-7	fpBGA	900	Com	50
LFE2M50SE-5F672C	372	1.2V	-5	fpBGA	672	Com	50
LFE2M50SE-6F672C	372	1.2V	-6	fpBGA	672	Com	50
LFE2M50SE-7F672C	372	1.2V	-7	fpBGA	672	Com	50
LFE2M50SE-5F484C	270	1.2V	-5	fpBGA	484	Com	50
LFE2M50SE-6F484C	270	1.2V	-6	fpBGA	484	Com	50
LFE2M50SE-7F484C	270	1.2V	-7	fpBGA	484	Com	50