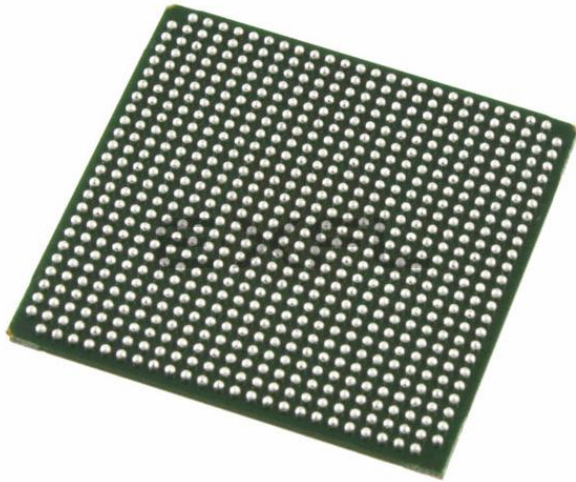




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

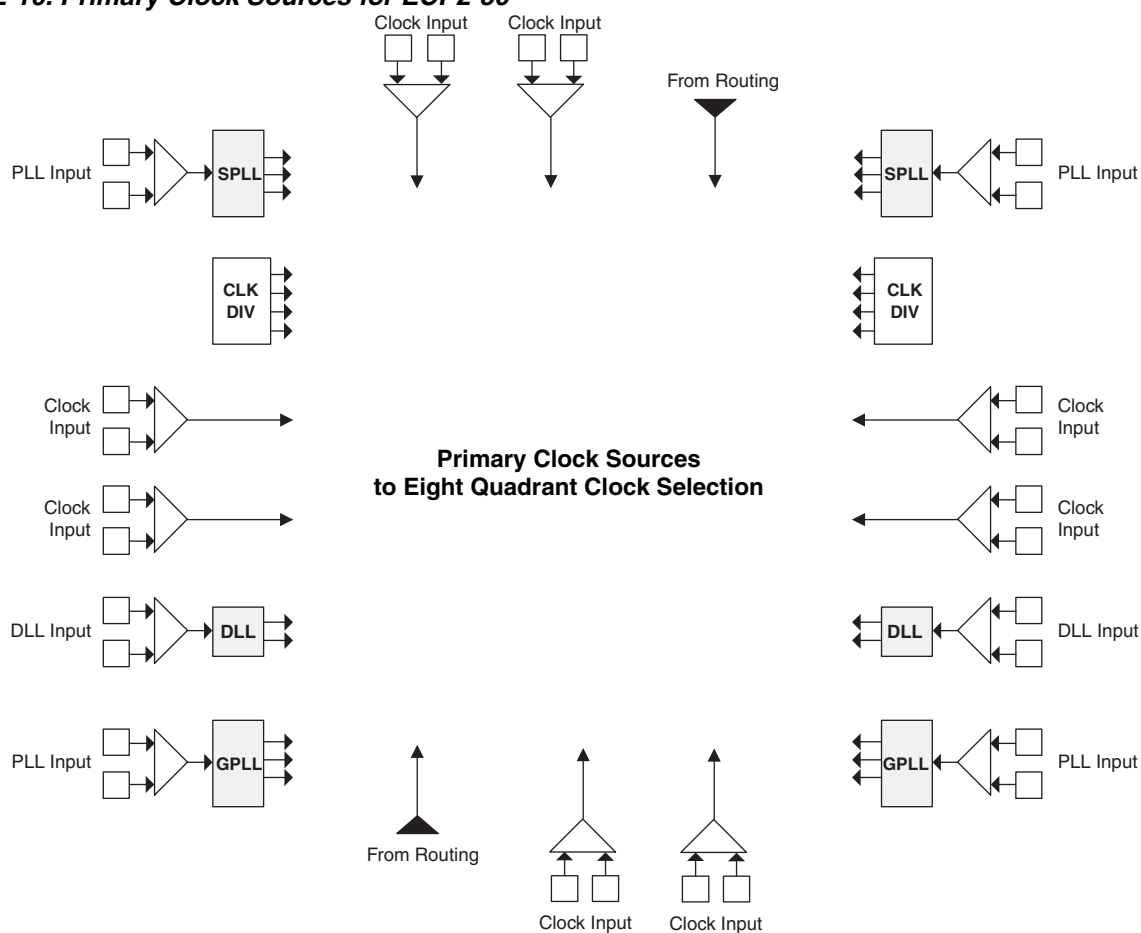
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-5fn672c

Figure 2-10. Primary Clock Sources for ECP2-50

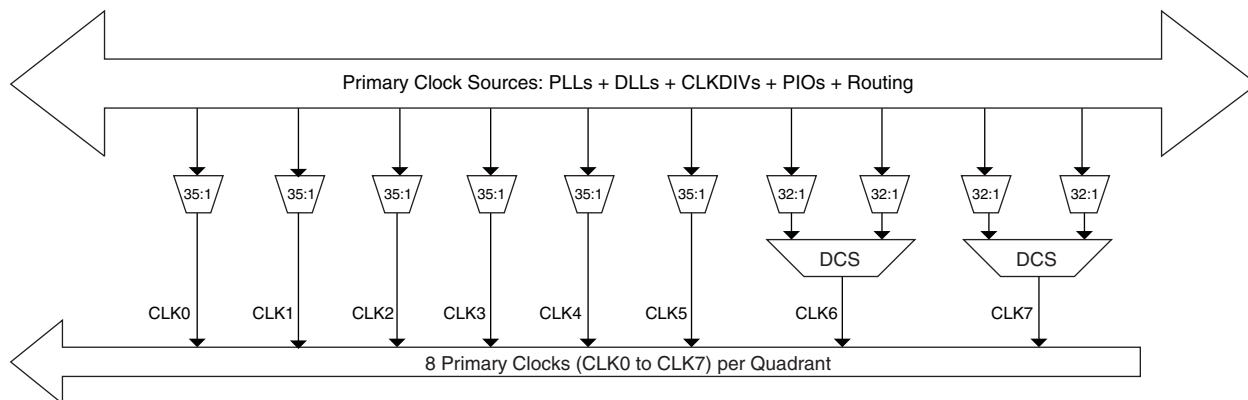


Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

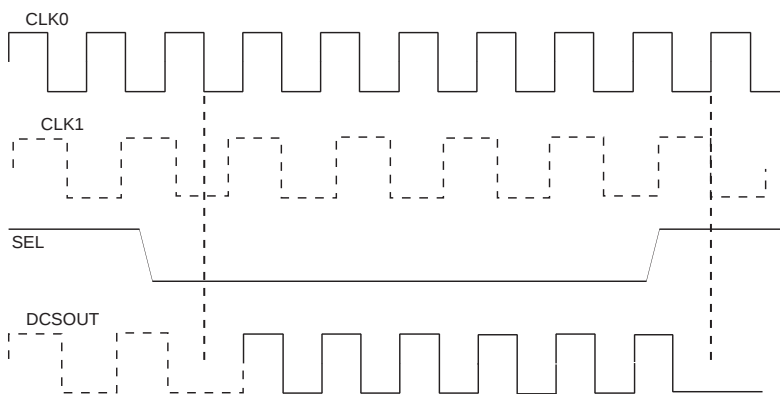


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

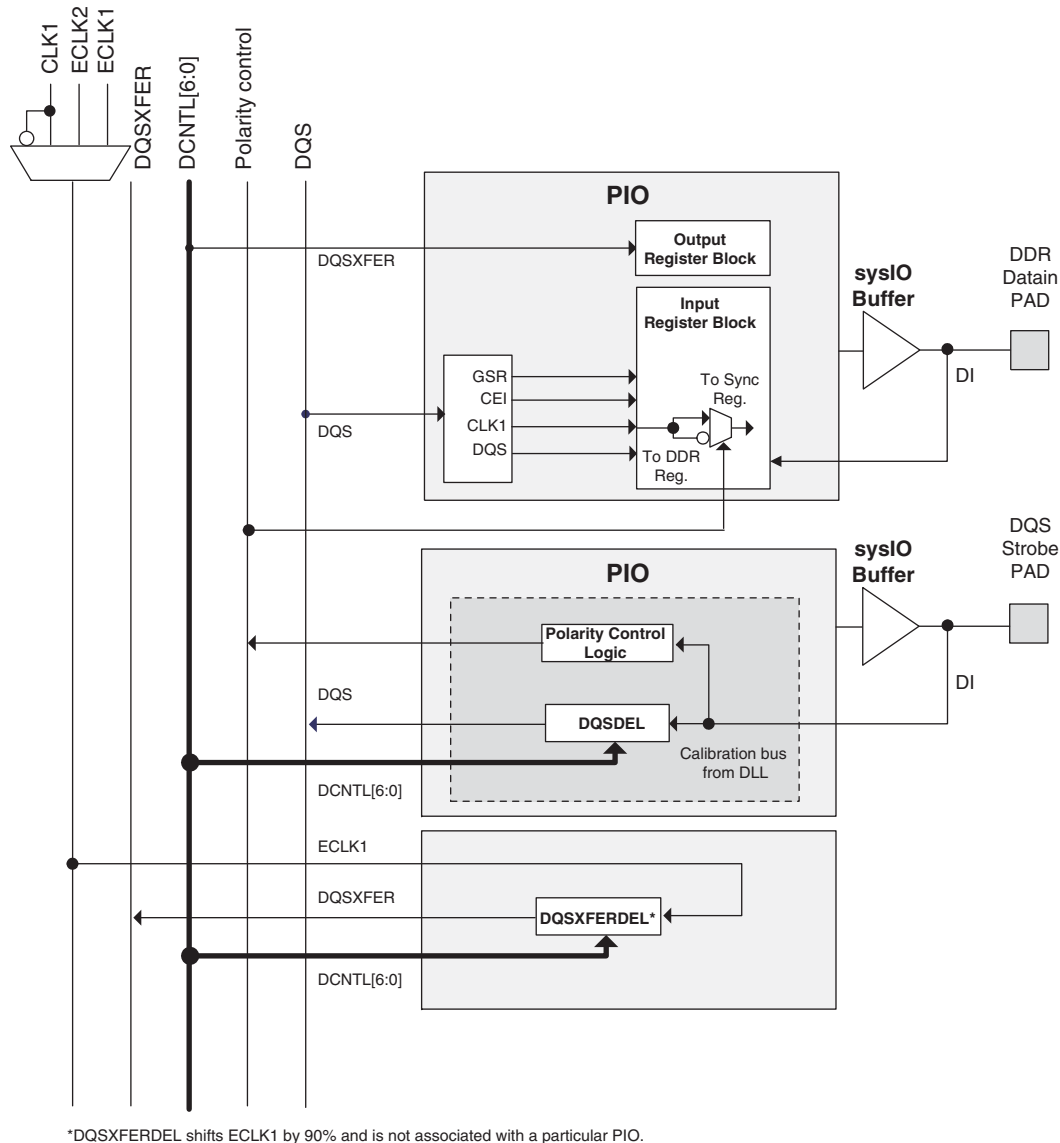
Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

Figure 2-36. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90° and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.



LatticeECP2/M Family Data Sheet

DC and Switching Characteristics

September 2013

Data Sheet DS1006

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage V_{CC} -0.5 to 1.32V

Supply Voltage V_{CCAUX} -0.5 to 3.75V

Supply Voltage V_{CCJ} -0.5 to 3.75V

Output Supply Voltage V_{CCIO} -0.5 to 3.75V

Input or I/O Tristate Voltage Applied⁴ -0.5 to 3.75V

Storage Temperature (Ambient) -65 to 150°C

Junction Temperature (T_j) +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20ns.

Recommended Operating Conditions⁷

Symbol	Parameter	Min.	Max.	Units
$V_{CC}^{1, 4, 5}$	Core Supply Voltage	1.14	1.26	V
$V_{CCAUX}^{1, 3, 4, 5}$	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
$V_{CCIO}^{1, 2, 4}$	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}^1	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply (For LatticeECP2M Family Only)				
V_{CCIB}	Input Buffer Power Supply (1.2V)	1.14	1.26	V
	Input Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2V)	1.14	1.26	V
	Output Buffer Power Supply (1.5V)	1.425	1.575	V
$V_{CCAUX33}$	Termination Resistor Switching Power Supply	3.135	3.465	V
V_{CCR}^6	Receive Power Supply	1.14	1.26	V
V_{CCT}^6	Transmit Power Supply	1.14	1.26	V

LatticeECP2/M Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t _{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t _{RSTREC_SPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t _{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t _{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t _{HP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t _{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t _{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
t _{SUADDSUB}	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
t _{HADDSUB}	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

LatticeECP2 Power Supply and NC

Signals	144 TQFP ³	208 PQFP ³	256 fpBGA ⁴	484 fpBGA ⁴
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	LFE2-6: G7, G9, G10, H7, J10, K10, K8 LFE2-12/LFE2-20: G7, G9, G10, H7, J10, K10, K8	LFE2-12/LFE2-20: N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 LFE2-35/LFE2-50: J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	LFE2-12/LFE2-20: None LFE2-35: N6, N18 LFE2-50: N6, N18, K6, J16
GND ¹	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC ²	LFE2-6: 45, 46, 124, 127 LFE2-12: 127	None	LFE2-6: K6, R3, P4 LFE2-12/LFE2-20: None	LFE2-12: E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-20/LFE2-35: K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-50: None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
138	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	
139	GND	-			GND	-			
140	VCC	-			VCC	-			
141	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C	
142	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T	
143	VCCIO2	2			VCCIO2	2			
144	PR12A	2	RDQ10		PR16A	2	RDQS16		
145	GND	-			GND	-			
146	VCC	-			VCC	-			
147	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*	
148	VCCIO2	2			VCCIO2	2			
149	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*	
150	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*	
151	VCCAUX	-			VCCAUX	-			
152	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*	
153	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*	
154	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
155	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
156	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
157	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
158	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
159	GND	-			GND	-			
160	PT54B	1		C	PT62B	1		C	
161	PT54A	1		T	PT62A	1		T	
162	VCCIO1	1			VCCIO1	1			
163	PT52B	1		C	PT60B	1		C	
164	PT52A	1		T	PT60A	1		T	
165	PT50B	1		C	PT58B	1		C	
166	PT50A	1		T	PT58A	1		T	
167	PT48B	1		C	PT56B	1		C	
168	PT48A	1		T	PT56A	1		T	
169	GND	-			GND	-			
170	VCCIO1	1			VCCIO1	1			
171	VCC	-			VCC	-			
172	PT40B	1		C	PT50B	1		C	
173	PT40A	1		T	PT50A	1		T	
174	VCCAUX	-			VCCAUX	-			
175	GND	-			GND	-			
176	PT36B	1		C	PT44B	1		C	
177	PT36A	1		T	PT44A	1		T	
178	PT34B	1		C	PT42B	1		C	
179	PT34A	1		T	PT42A	1		T	
180	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C	
181	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T	
182	XRES	1			XRES	1			
183	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
B15	PT40B	1		C	PT49B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
A15	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A14	PT39A	1		T	PT48A	1		T
B14	PT39B	1		C	PT48B	1		C
D14	PT37B	1		C	PT46B	1		C
E14	PT36B	1		C	PT45B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
C13	PT37A	1		T	PT46A	1		T
F14	PT36A	1		T	PT45A	1		T
A13	PT35B	1		C	PT44B	1		C
E13	PT34B	1		C	PT43B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B13	PT35A	1		T	PT44A	1		T
D13	PT34A	1		T	PT43A	1		T
E12	PT33B	1		C	PT42B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
D12	PT33A	1		T	PT42A	1		T
A12	PT31B	1		C	PT40B	1		C
B12	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C
VCCIO	VCCIO1	1			VCCIO1	1		
A11	PT31A	1		T	PT40A	1		T
C12	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T
F12	XRES	1			XRES	1		
B10	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
B11	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
C11	PT26B	0		C	PT35B	0		C
A10	PT27B	0		C	PT36B	0		C
C10	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
A9	PT27A	0		T	PT36A	0		T
A8	PT24B	0		C	PT33B	0		C
E11	PT25B	0		C	PT34B	0		C
A7	PT24A	0		T	PT33A	0		T
F11	PT25A	0		T	PT34A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
B8	PT23B	0		C	PT32B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B9	PT23A	0		T	PT32A	0		T
C8	PT20B	0		C	PT29B	0		C
B7	PT21B	0		C	PT30B	0		C
D8	PT20A	0		T	PT29A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W5	PL71B	6	LDQ75	C (LVDS)*	PL84B	6	LDQ88	C (LVDS)*	
AC1	PL72A	6	LDQ75	T	PL85A	6	LDQ88	T	
AD1	PL72B	6	LDQ75	C	PL85B	6	LDQ88	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y6	PL73A	6	LDQ75	T (LVDS)*	PL86A	6	LDQ88	T (LVDS)*	
Y5	PL73B	6	LDQ75	C (LVDS)*	PL86B	6	LDQ88	C (LVDS)*	
AE2	PL74A	6	LDQ75	T	PL87A	6	LDQ88	T	
AD2	PL74B	6	LDQ75	C	PL87B	6	LDQ88	C	
GND	GNDIO6	-			GNDIO6	-			
AB3	PL75A	6	LDQS75	T (LVDS)*	PL88A	6	LDQS88	T (LVDS)*	
AB2	PL75B	6	LDQ75	C (LVDS)*	PL88B	6	LDQ88	C (LVDS)*	
W7	PL76A	6	LDQ75	T	PL89A	6	LDQ88	T	
VCCIO	VCCIO6	6			VCCIO6	6			
W8	PL76B	6	LDQ75	C	PL89B	6	LDQ88	C	
Y7	PL77A	6	LDQ75	T (LVDS)*	PL90A	6	LDQ88	T (LVDS)*	
Y8	PL77B	6	LDQ75	C (LVDS)*	PL90B	6	LDQ88	C (LVDS)*	
AC2	PL78A	6	LDQ75	T	PL91A	6	LDQ88	T	
GND	GNDIO6	-			GNDIO6	-			
AD3	PL78B	6	LDQ75	C	PL91B	6	LDQ88	C	
AC3	TCK	-			TCK	-			
AA8	TDI	-			TDI	-			
AB4	TMS	-			TMS	-			
AA5	TDO	-			TDO	-			
AB5	VCCJ	-			VCCJ	-			
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
GND	GNDIO5	-			GNDIO5	-			
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB82A	4	VREF2_4/BDQ78	T	PB100A	4	VREF2_4/BDQ96	T
AB23	PB82B	4	VREF1_4/BDQ78	C	PB100B	4	VREF1_4/BDQ96	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR77B	8	WRITEN	C	PR90B	8	WRITEN	C
Y22	PR77A	8	CS1N	T	PR90A	8	CS1N	T
AC25	PR76B	8	CSN	C	PR89B	8	CSN	C
AB25	PR76A	8	D0/SPIFASTN	T	PR89A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR75B	8	D1	C	PR88B	8	D1	C
AC26	PR75A	8	D2	T	PR88A	8	D2	T
Y23	PR74B	8	D3	C	PR87B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR74A	8	D4	T	PR87A	8	D4	T
AA25	PR73B	8	D5	C	PR86B	8	D5	C
AB26	PR73A	8	D6	T	PR86A	8	D6	T
W23	PR72B	8	D7/SPID0	C	PR85B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR72A	8	DI/CSSPI0N	T	PR85A	8	DI/CSSPI0N	T
Y24	PR71B	8	DOUT/CSON	C	PR84B	8	DOUT/CSON	C
Y25	PR71A	8	BUSY/SISPI	T	PR84A	8	BUSY/SISPI	T
W24	PR70B	3	RDQ67	C	PR83B	3	RDQ80	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR70A	3	RDQ67	T	PR83A	3	RDQ80	T
AA26	PR69B	3	RDQ67	C (LVDS)*	PR82B	3	RDQ80	C (LVDS)*
Y26	PR69A	3	RDQ67	T (LVDS)*	PR82A	3	RDQ80	T (LVDS)*
U21	PR68B	3	RDQ67	C	PR81B	3	RDQ80	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR68A	3	RDQ67	T	PR81A	3	RDQ80	T
W25	PR67B	3	RDQ67	C (LVDS)*	PR80B	3	RDQ80	C (LVDS)*
W26	PR67A	3	RDQS67	T (LVDS)*	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR66B	3	RDQ67	C	PR79B	3	RDQ80	C
V25	PR66A	3	RDQ67	T	PR79A	3	RDQ80	T
V26	PR65B	3	RDQ67	C (LVDS)*	PR78B	3	RDQ80	C (LVDS)*
U26	PR65A	3	RDQ67	T (LVDS)*	PR78A	3	RDQ80	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR64B	3	RLM0_GPLL_C_FB_A/RDQ67	C	PR77B	3	RLM0_GPLL_C_FB_A/RDQ80	C
U23	PR64A	3	RLM0_GPLL_T_FB_A/RDQ67	T	PR77A	3	RLM0_GPLL_T_FB_A/RDQ80	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AB24	PR87B	8	D3	C
GND	GNDIO4	-		
AB23	PR87A	8	D4	T
AB25	PR86B	8	D5	C
AB26	PR86A	8	D6	T
AC27	PR85B	8	D7/SPID0	C
VCCIO	VCCIO8	8		
AB27	PR85A	8	DI/CSSPION	T
AD29	PR84B	8	DOUT/CSON	C
AD30	PR84A	8	BUSY/SISPI	T
AA25	PR83B	3	RDQ80	C
GND	GNDIO3	-		
AA23	PR83A	3	RDQ80	T
AC29	PR82B	3	RDQ80	C (LVDS)*
AC30	PR82A	3	RDQ80	T (LVDS)*
AA26	PR81B	3	RDQ80	C
VCCIO	VCCIO3	3		
AA24	PR81A	3	RDQ80	T
AB29	PR80B	3	RDQ80	C (LVDS)*
AB30	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	-		
Y23	PR79B	3	RDQ80	C
Y25	PR79A	3	RDQ80	T
AA27	PR78B	3	RDQ80	C (LVDS)*
AA28	PR78A	3	RDQ80	T (LVDS)*
VCCIO	VCCIO3	3		
Y24	PR77B	3	RLM0_GPLL_C_FB_A/RDQ80	C
Y26	PR77A	3	RLM0_GPLLT_FB_A/RDQ80	T
AA29	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*
AA30	PR76A	3	RLM0_GPLLT_IN_A**/RDQ80	T (LVDS)*
R22	RLM0_PLLCAP	3		
W23	PR74B	3	RLM0_GDLL_C_FB_A/RDQ71	C
W25	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T
GND	GNDIO3	-		
Y27	PR73B	3	RLM0_GDLL_C_IN_A**/RDQ71	C (LVDS)*
Y28	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*
W24	PR72B	3	RDQ71	C
W26	PR72A	3	RDQ71	T
VCCIO	VCCIO3	3		
Y29	PR71B	3	RDQ71	C (LVDS)*
Y30	PR71A	3	RDQS71	T (LVDS)*
V25	PR70B	3	RDQ71	C
GND	GNDIO3	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C12	URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCR2	12		
A15	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCR3	12		
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
E13	PT55B	1		C
D12	PT55A	1		T
GNDIO	GNDIO1	-		
A9	PT54B	1		C
A8	PT54A	1		T
A7	PT53B	1		C
A6	PT53A	1		T
VCCIO	VCCIO1	1		
E12	PT52B	1		C
F12	PT52A	1		T
A5	PT51B	1		C
A4	PT51A	1		T
GNDIO	GNDIO1	-		
B7	PT50B	1		C
B8	PT50A	1		T
G11	PT49B	1		C
E11	PT49A	1		T
VCCIO	VCCIO1	1		
D11	PT48B	1	VREF2_1	C
D10	PT48A	1	VREF1_1	T
G10	PT47B	1	PCLKC1_0	C
F11	PT47A	1	PCLKT1_0	T
G9	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
F9	PT46A	0	PCLKT0_0	T
C9	PT45B	0	VREF2_0	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L16	GND	-			GND	-			
L17	GND	-			GND	-			
L2	GND	-			GND	-			
L20	GND	-			GND	-			
L25	GND	-			GND	-			
L7	GND	-			GND	-			
M13	GND	-			GND	-			
M14	GND	-			GND	-			
N10	GND	-			GND	-			
N12	GND	-			GND	-			
N13	GND	-			GND	-			
N14	GND	-			GND	-			
N15	GND	-			GND	-			
N17	GND	-			GND	-			
P10	GND	-			GND	-			
P12	GND	-			GND	-			
P13	GND	-			GND	-			
P14	GND	-			GND	-			
P15	GND	-			GND	-			
P17	GND	-			GND	-			
R13	GND	-			GND	-			
R14	GND	-			GND	-			
T10	GND	-			GND	-			
T11	GND	-			GND	-			
T16	GND	-			GND	-			
T17	GND	-			GND	-			
T2	GND	-			GND	-			
T20	GND	-			GND	-			
T25	GND	-			GND	-			
T7	GND	-			GND	-			
U11	GND	-			GND	-			
U13	GND	-			GND	-			
U14	GND	-			GND	-			
U16	GND	-			GND	-			
V22	GND	-			GND	-			
V5	GND	-			GND	-			
Y11	GND	-			GND	-			
Y16	GND	-			GND	-			
AB3	NC	-			NC	-			
AB4	NC	-			NC	-			
AC1	NC	-			NC	-			
AC2	NC	-			NC	-			
B4	NC	-			NC	-			
B5	NC	-			NC	-			
C26	NC	-			NC	-			
D20	NC	-			NC	-			
D21	NC	-			NC	-			
D22	NC	-			NC	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L5	PL23A	7	LDQ27	T (LVDS)*	PL33A	7	LDQ37	T (LVDS)*	
L4	PL23B	7	LDQ27	C (LVDS)*	PL33B	7	LDQ37	C (LVDS)*	
N9	PL24A	7	LDQ27	T	PL34A	7	LDQ37	T	
N7	PL24B	7	LDQ27	C	PL34B	7	LDQ37	C	
K2	PL25A	7	LDQ27	T (LVDS)*	PL35A	7	LDQ37	T (LVDS)*	
K1	PL25B	7	LDQ27	C (LVDS)*	PL35B	7	LDQ37	C (LVDS)*	
P9	PL26A	7	LDQ27	T	PL36A	7	LDQ37	T	
P7	PL26B	7	LDQ27	C	PL36B	7	LDQ37	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M6	PL27A	7	LDQS27	T (LVDS)*	PL37A	7	LDQS37	T (LVDS)*	
M5	PL27B	7	LDQ27	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
N5	PL28A	7	LDQ27	T	PL38A	7	LDQ37	T	
N6	PL28B	7	LDQ27	C	PL38B	7	LDQ37	C	
M4	PL29A	7	LDQ27	T (LVDS)*	PL39A	7	LDQ37	T (LVDS)*	
M3	PL29B	7	LDQ27	C (LVDS)*	PL39B	7	LDQ37	C (LVDS)*	
P6	PL30A	7	LDQ27	T	PL40A	7	LDQ37	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P8	PL30B	7	LDQ27	C	PL40B	7	LDQ37	C	
L3	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	
L2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	
P5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	
P4	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	
L1	PL34A	7	LDQ36	T (LVDS)*	PL44A	7	LDQ46	T (LVDS)*	
M2	PL34B	7	LDQ36	C (LVDS)*	PL44B	7	LDQ46	C (LVDS)*	
R5	PL35A	7	LDQ36	T	PL45A	7	LDQ46	T	
R4	PL35B	7	LDQ36	C	PL45B	7	LDQ46	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M1	PL36A	7	LDQS36	T (LVDS)*	PL46A	7	LDQS46	T (LVDS)*	
N2	PL36B	7	LDQ36	C (LVDS)*	PL46B	7	LDQ46	C (LVDS)*	
R8	PL37A	7	LDQ36	T	PL47A	7	LDQ46	T	
T9	PL37B	7	LDQ36	C	PL47B	7	LDQ46	C	
P3	PL38A	7	LDQ36	T (LVDS)*	PL48A	7	LDQ46	T (LVDS)*	
P2	PL38B	7	LDQ36	C (LVDS)*	PL48B	7	LDQ46	C (LVDS)*	
N1	PL39A	7	PCLKT7_0/LDQ36	T	PL49A	7	PCLKT7_0/LDQ46	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P1	PL39B	7	PCLKC7_0/LDQ36	C	PL49B	7	PCLKC7_0/LDQ46	C	
T5	PL41A	6	PCLKT6_0	T (LVDS)*	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	
T4	PL41B	6	PCLKC6_0	C (LVDS)*	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	
U7	PL42A	6	VREF2_6	T	PL52A	6	VREF2_6/LDQ55	T	
T8	PL42B	6	VREF1_6	C	PL52B	6	VREF1_6/LDQ55	C	
R3	PL43A	6		T (LVDS)*	PL53A	6	LDQ55	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
R2	PL43B	6		C (LVDS)*	PL53B	6	LDQ55	C (LVDS)*	
R1	PL44A	6		T	PL54A	6	LDQ55	T	
T1	PL44B	6		C	PL54B	6	LDQ55	C	
GNDIO	GNDIO6	-			GNDIO6	-			
-	-	-			VCCIO6	6			
T3	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AA1	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-		
AA2	PL81B	6	LDQ81	C (LVDS)*
Y3	PL82A	6	LDQ81	T
AB1	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6		
Y9	PL83A	6	LDQ81	T (LVDS)*
Y8	PL83B	6	LDQ81	C (LVDS)*
Y7	PL84A	6	LDQ81	T
AA7	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-		
VCCIO	VCCIO6	6		
AB2	PL95A	6	LDQ99	T (LVDS)*
AB3	PL95B	6	LDQ99	C (LVDS)*
AA5	PL96A	6	LDQ99	T
AA6	PL96B	6	LDQ99	C
AB4	PL97A	6	LDQ99	T (LVDS)*
VCCIO	VCCIO6	6		
AB5	PL97B	6	LDQ99	C (LVDS)*
AA8	PL98A	6	LDQ99	T
AA9	PL98B	6	LDQ99	C
AC1	PL99A	6	LLM0_GPLLT_IN_A**/LDQS99	T (LVDS)*
GNDIO	GNDIO6	-		
AC2	PL99B	6	LLM0_GPLLC_IN_A**/LDQ99	C (LVDS)*
AC4	PL100A	6	LLM0_GPLLT_FB_A/LDQ99	T
AC3	PL100B	6	LLM0_GPLLC_FB_A/LDQ99	C
VCCIO	VCCIO6	6		
AC7	PL101A	6	LLM0_GDLLT_IN_A**/LDQ99	T (LVDS)*
AC6	PL101B	6	LLM0_GDLLC_IN_A**/LDQ99	C (LVDS)*
AC5	PL102A	6	LLM0_GDLLT_FB_A/LDQ99	T
AD3	PL102B	6	LLM0_GDLLC_FB_A/LDQ99	C
GNDIO	GNDIO6	-		
AB8	LLM0_PLLCAP	6		
AD2	PL104A	6		T
AD1	PL104B	6		C
AE2	TCK	-		
AE1	TDI	-		
AF2	TMS	-		
AF1	TDO	-		
AG1	VCCJ	-		
AH1	LLC_SQ_VCCR3	14		
AK2	LLC_SQ_HDINP3	14		T
AJ1	LLC_SQ_VCCIB3	14		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D19	PT93B	1		C
E18	PT93A	1		T
D18	PT92B	1		C
C17	PT92A	1		T
A17	PT91B	1		C
B17	PT91A	1		T
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
J18	PT75B	1		C
J19	PT75A	1		T
H17	PT74B	1		C
J17	PT74A	1		T
F18	PT73B	1		C
F17	PT73A	1		T
GNDIO	GNDIO1	-		
A16	PT72B	1		C
B16	PT72A	1		T
G17	PT71B	1		C
G16	PT71A	1		T
VCCIO	VCCIO1	1		
H16	PT70B	1		C
F16	PT70A	1		T
J16	PT69B	1		C
G15	PT69A	1		T
GNDIO	GNDIO1	-		
C16	PT68B	1		C
D16	PT68A	1		T
J15	PT67B	1		C
H15	PT67A	1		T
VCCIO	VCCIO1	1		
A15	PT66B	1	VREF2_1	C
B15	PT66A	1	VREF1_1	T
F15	PT65B	1	PCLKC1_0	C
E16	PT65A	1	PCLKT1_0	T
C15	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
D15	PT64A	0	PCLKT0_0	T
C14	PT63B	0	VREF2_0	C
E15	PT63A	0	VREF1_0	T
G14	PT62B	0		C
VCCIO	VCCIO0	0		
J14	PT62A	0		T
F14	PT61B	0		C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U22	GND	-			GND	-		
U23	GND	-			GND	-		
V12	GND	-			GND	-		
V13	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V18	GND	-			GND	-		
V19	GND	-			GND	-		
V20	GND	-			GND	-		
V22	GND	-			GND	-		
V23	GND	-			GND	-		
W12	GND	-			GND	-		
W13	GND	-			GND	-		
W15	GND	-			GND	-		
W16	GND	-			GND	-		
W17	GND	-			GND	-		
W18	GND	-			GND	-		
W19	GND	-			GND	-		
W20	GND	-			GND	-		
W22	GND	-			GND	-		
W23	GND	-			GND	-		
W26	GND	-			GND	-		
W31	GND	-			GND	-		
W4	GND	-			GND	-		
W9	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
Y18	GND	-			GND	-		
Y19	GND	-			GND	-		
A11	NC	-			NC	-		
A12	NC	-			NC	-		
A23	NC	-			NC	-		
A24	NC	-			NC	-		
AA11	NC	-			NC	-		
AB11	NC	-			NC	-		
AC26	NC	-			NC	-		
AC30	NC	-			NC	-		
AD11	NC	-			NC	-		
AD12	NC	-			NC	-		
AD13	NC	-			NC	-		
AD14	NC	-			NC	-		
AD15	NC	-			NC	-		
AD19	NC	-			NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD23	NC	-			NC	-		
AE10	NC	-			NC	-		
AE11	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	20
LFE2-20SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	20
LFE2-20SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	20
LFE2-20SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	20
LFE2-20SE-5F484I	331	1.2V	-5	fpBGA	484	Ind	20
LFE2-20SE-6F484I	331	1.2V	-6	fpBGA	484	Ind	20
LFE2-20SE-5F672I	402	1.2V	-5	fpBGA	672	Ind	20
LFE2-20SE-6F672I	402	1.2V	-6	fpBGA	672	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484I	331	1.2V	-5	fpBGA	484	Ind	35
LFE2-35SE-6F484I	331	1.2V	-6	fpBGA	484	Ind	35
LFE2-35SE-5F672I	450	1.2V	-5	fpBGA	672	Ind	35
LFE2-35SE-6F672I	450	1.2V	-6	fpBGA	672	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484I	339	1.2V	-5	fpBGA	484	Ind	50
LFE2-50SE-6F484I	339	1.2V	-6	fpBGA	484	Ind	50
LFE2-50SE-5F672I	500	1.2V	-5	fpBGA	672	Ind	50
LFE2-50SE-6F672I	500	1.2V	-6	fpBGA	672	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672I	500	1.2V	-5	fpBGA	672	Ind	70
LFE2-70SE-6F672I	500	1.2V	-6	fpBGA	672	Ind	70
LFE2-70SE-5F900I	583	1.2V	-5	fpBGA	900	Ind	70
LFE2-70SE-6F900I	583	1.2V	-6	fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2-35SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2-35SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2-35SE-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2-35SE-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2-35SE-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2-50SE-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2-50SE-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	Com	50
LFE2-50SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2-50SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2-50SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	70
LFE2-70SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	70
LFE2-70SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	70
LFE2-70SE-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2-70SE-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2-70SE-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	Ind	6
LFE2-6SE-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	Ind	6
LFE2-6SE-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	Ind	6
LFE2-6SE-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	Ind	12
LFE2-12SE-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	Ind	12
LFE2-12SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	12
LFE2-12SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	12
LFE2-12SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	Ind	12
LFE2-12SE-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	Ind	12



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For Further Information

A variety of technical notes for the LatticeECP2/M family are available on the Lattice web site at www.latticesemi.com.

- TN1102, [LatticeECP2/M sysIO Usage Guide](#)
- TN1103, [LatticeECP2/M sysCLOCK PLL Design and Usage Guide](#)
- TN1104, [LatticeECP2/M Memory Usage Guide](#)
- TN1105, [LatticeECP2/M High-Speed I/O Interface](#)
- TN1106, [Power Estimation and Management for LatticeECP2/M Devices](#)
- TN1107, [LatticeECP2/M sysDSP Usage Guide](#)
- TN1108, [LatticeECP2/M sysCONFIG Usage Guide](#)
- TN1109, [LatticeECP2/M Configuration Encryption Usage Guide](#)
- TN1113, [LatticeECP2/M Soft Error Detection \(SED\) Usage Guide](#)
- TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#)
- TN1162, [LatticeECP2/M Hardware Checklist](#)

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com