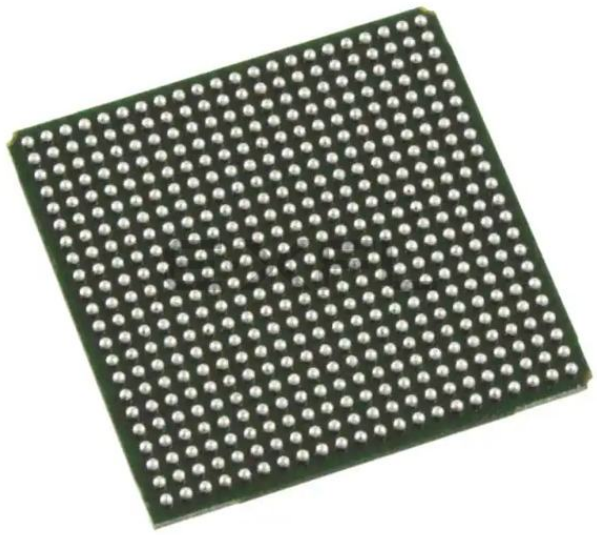
Lattice Semiconductor Corporation - LFE2-35SE-6F484I Datasheet



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Details	
Product Status	Obsolete
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	331
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-6f484i

LatticeECP2/M Family Data Sheet Architecture

September 2013 **Data Sheet DS1006**

Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing blocks, as shown in Figure 2-1. In addition, the LatticeECP2M family contains SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP2/M devices are arranged in eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as SPI4.2, along with memory interfaces including DDR2.

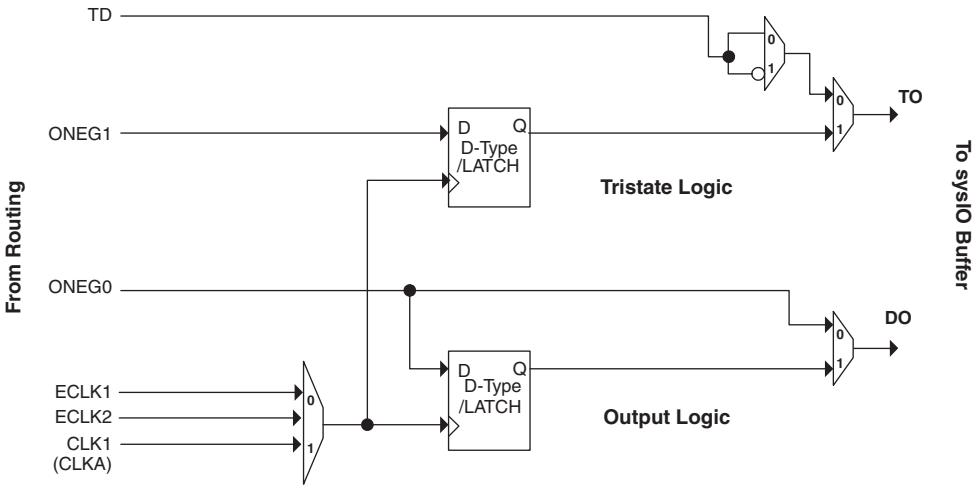
The LatticeECP2/M registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block is located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. The Ball Grid Array (BGA) package devices in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator. The LatticeECP2/M devices use 1.2V as their core voltage.

Figure 2-32. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-31 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-32 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 16 PIOs. Figure 2-33 shows the assignment of DQS pins in each set of 16 PIOs.

Bottom Edge

PICs on the bottom edge have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-34 shows the assignment of DQS pins in each set of 18 PIOs.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	-210	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1[4]	I/O Capacitance	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	5	8	pf
C2[4]	Dedicated Input Capacitance	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	5	6	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as V_{REF}, maximum leakage = 25uA
3. Applicable to general purpose I/Os in top and bottom banks.
4. T_A 25°C, f = 1.0MHz.

sysCLOCK SPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	33	—	420	MHz
		With external capacitor[5, 6]	2	—	420	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	33	—	420	MHz
		With external capacitor[5]	5	—	50	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.258	—	210	MHz
		With external capacitor[5]	0.039	—	25	MHz
f_{VCO}	PLL VCO Frequency		640	—	1280	MHz
f_{PFD}	Phase Detector Input Frequency	Without external capacitor	33	—	420	MHz
		With external capacitor[6]	2	—	50	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Selected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—	±0.05	UI
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 100$ MHz	—	—	±125	ps
		$50 \leq f_{OUT} < 100$ MHz	—	—	0.025	UIPP
		$f_{OUT} < 50$ MHz	—	—	0.04	UIPP
t_{SK}	Input Clock to Output Clock Skew	Divider Ratio = Integer	—	—	±250	ps
t_W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—	150	µs
		With external capacitor[5]	—	—	500	µs
t_{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width (RSTK)		15	—	—	ns
	Reset Signal Pulse Width (RST)	Without external capacitor	500	—	—	ns
		With external capacitor[5]	20	—	—	µs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Phase accuracy of CLKOS compared to CLKOP.
5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.
6. f_{OUT} (max) = f_{IN} * 10 for f_{IN} < 5MHz.

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70 (Cont.)

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	2	3	3	4
	Bank3	0	3	3	3
	Bank4	3	4	4	4
	Bank5	3	4	4	5
	Bank6	1	4	4	4
	Bank7	2	3	3	4
	Bank8	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	0	0	0	0
	Bank3	0	0	0	0
	Bank4	46	62	62	72
	Bank5	46	68	68	80
	Bank6	0	0	0	0
	Bank7	0	0	0	0
	Bank8	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Power Supply and NC (Cont.)

Signal	1152 fpBGA
V_{CC}	AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22
V_{CCIO0}	C12, C16, E14, H12, H16, M14, M15
V_{CCIO1}	C19, C23, E21, H19, H23, M20, M21
V_{CCIO2}	G32, K28, K32, N27, N32, P23, R23, T27, T32
V_{CCIO3}	AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23
V_{CCIO4}	AC20, AC21, AG19, AG23, AK21, AM19, AM23
V_{CCIO5}	AC14, AC15, AG12, AG16, AK14, AM12, AM16
V_{CCIO6}	AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12
V_{CCIO7}	G3, K3, K7, N3, N8, P12, R12, T3, T8
V_{CCIO8}	AD28, AG32
V_{CCJ}	AK3
V_{CCAUX}	AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23
V_{CCPLL}	R15, R20, Y15, Y20
SERDES Power[3]	D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7
GND[1]	A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19
NC[2]	**LFE2M70:** H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 **LFE2M100:** A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11,G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
-	-	-			GNDIO1	1		
-	-	-			VCCIO	1		
D10	PT19B	1		C	PT37B	1		C
C10	PT19A	1		T	PT37A	1		T
GND	GNDIO1	-			GNDIO1	-		
B10	PT18B	1		C	PT36B	1		C
A9	PT17B	1		C	PT35B	1		C
A10	PT18A	1		T	PT36A	1		T
B9	PT17A	1		T	PT35A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A8	PT16B	1		C	PT34B	1		C
D9	PT15B	1		C	PT33B	1		C
B8	PT16A	1		T	PT34A	1		T
C9	PT15A	1		T	PT33A	1		T
GND	GNDIO1	-			GNDIO1	-		
B7	PT14B	1		C	PT32B	1		C
E9	PT13B	1		C	PT31B	1		C
A7	PT14A	1		T	PT32A	1		T
D8	PT13A	1		T	PT31A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A6	PT12B	1	PCLKC1_0	C	PT30B	1	PCLKC1_0	C
B6	PT12A	1	PCLKT1_0	T	PT30A	1	PCLKT1_0	T
E6	XRES	-			XRES	1		
F8	PT10B	0	PCLKC0_0	C	PT28B	0	PCLKC0_0	C
GND	GNDIO0	-			GNDIO0	-		
E8	PT10A	0	PCLKT0_0	T	PT28A	0	PCLKT0_0	T
A5	PT9B	0		C	PT27B	0		C
A3	PT8B	0		C	PT26B	0		C
A4	PT9A	0		T	PT27A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
B3	PT8A	0		T	PT26A	0		T
A2	PT7B	0		C	PT25B	0		C
C7	PT6B	0		C	PT24B	0		C
B2	PT7A	0		T	PT25A	0		T
D7	PT6A	0		T	PT24A	0		T
D6	PT5B	0		C	PT23B	0		C
GND	GNDIO0	-			GNDIO0	-		
F7	PT4B	0		C	PT22B	0		C
C6	PT5A	0		T	PT23A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F6	PT4A	0		T	PT22A	0		T
C4	PT3B	0		C	PT21B	0		C
B4	PT3A	0		T	PT21A	0		T
-	-	-			GNDIO0	0		
-	-	-			VCCIO	0		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	L11	PB61B	4	BDQ60	C
T13	T13	PB62A	4	BDQ60	T
R13	R13	PB63A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
T14	T14	PB62B	4	BDQ60	C
P13	P13	PB63B	4	BDQ60	C
GND	GND	GNDIO4	-		
N12	N12	PB64A	4	VREF2_4/BDQ60	T
M12	M12	PB64B	4	VREF1_4/BDQ60	C
R15	R15	CFG2	8		
N14	N14	CFG1	8		
N13	N13	PROGRAMN	8		
N15	N15	CFG0	8		
P15	P15	PR44B	8	WRITEN	C
L12	L12	INITN	8		
N16	N16	PR43B	8	CSN	C
GND	GND	GNDIO8	-		
R14	R14	CCLK	8		
P14	P14	PR44A	8	CS1N	T
M13	M13	DONE	8		
R16	R16	PR42B	8	D1	C
VCCIO	VCCIO	VCCIO8	8		
M16	M16	PR43A	8	D0/SPIFASTN	T
P16	P16	PR42A	8	D2	T
L15	L15	PR41B	8	D3	C
GND	GND	GNDIO8	-		
L14	L14	PR40A	8	D6	T
L16	L16	PR41A	8	D4	T
L10	L10	PR39B	8	D7/SPID0	C
L13	L13	PR40B	8	D5	C
VCCIO	VCCIO	VCCIO8	8		
K11	K11	PR39A	8	DI/CSSPI0N	T
K14	K14	PR38B	8	DOUT/CSON	C
K13	K13	PR38A	8	BUSY/SISPI	T
GND	GND	GNDIO8	-		
K15	K15	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C
VCCIO	VCCIO	VCCIO3	3		
K16	K16	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
GND	GND	GNDIO3	-		
J16	J16	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
J15	J15	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
J14	J14	RLM0_PLLCAP	3		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		
V20	PROGRAMN	8			PROGRAMN	8		
W20	CFG0	8			CFG0	8		
U22	PR28B	8	D1	C	PR42B	8	D1	C
V22	INITN	8			INITN	8		
R16	PR30B	8	WRITEN	C	PR44B	8	WRITEN	C
GNDIO	GNDIO8	-			GNDIO8	-		
W22	CCLK	8			CCLK	8		
R17	PR30A	8	CS1N	T	PR44A	8	CS1N	T
V21	DONE	8			DONE	8		
VCCIO	VCCIO8	8			VCCIO8	8		
U19	PR29B	8	CSN	C	PR43B	8	CSN	C
T17	PR26B	8	D5	C	PR40B	8	D5	C
U20	PR29A	8	D0/SPIFASTN	T	PR43A	8	D0/SPIFASTN	T
U21	PR28A	8	D2	T	PR42A	8	D2	T
GNDIO	GNDIO8	-			GNDIO8	-		
T18	PR26A	8	D6	T	PR40A	8	D6	T
T20	PR27B	8	D3	C	PR41B	8	D3	C
T21	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
T19	PR27A	8	D4	T	PR41A	8	D4	T
VCCIO	VCCIO8	8			VCCIO8	8		
T22	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
R18	PR24B	8	DOUT/CSON	C	PR38B	8	DOUT/CSON	C
R19	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
-	-	-			VCCIO3	3		
GNDIO	GNDIO3	-			GNDIO3	-		
P18	PR22B	3		C (LVDS)*	PR32B	3	RDQ34	C (LVDS)*
R22	PR23B	3		C	PR33B	3	RDQ34	C
P19	PR22A	3		T (LVDS)*	PR32A	3	RDQ34	T (LVDS)*
R21	PR23A	3		T	PR33A	3	RDQ34	T
VCCIO	VCCIO3	3			VCCIO3	3		
R20	PR21B	3	RLM0_GPLLC_FB_A	C	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
P21	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR18B	3	RLM0_GDLLC_FB_A	C	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
M22	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
N19	NC	-			PR26B	3	RDQ25	C
-	-	-			VCCIO3	3		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB64A	4	VREF2_4/BDQ60	T	PB73A	4	VREF2_4/BDQ69	T
AB23	PB64B	4	VREF1_4/BDQ60	C	PB73B	4	VREF1_4/BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR44B	8	WRITEN	C	PR58B	8	WRITEN	C
Y22	PR44A	8	CS1N	T	PR58A	8	CS1N	T
AC25	PR43B	8	CSN	C	PR57B	8	CSN	C
AB25	PR43A	8	D0/SPIFASTN	T	PR57A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR42B	8	D1	C	PR56B	8	D1	C
AC26	PR42A	8	D2	T	PR56A	8	D2	T
Y23	PR41B	8	D3	C	PR55B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR41A	8	D4	T	PR55A	8	D4	T
AA25	PR40B	8	D5	C	PR54B	8	D5	C
AB26	PR40A	8	D6	T	PR54A	8	D6	T
W23	PR39B	8	D7/SPID0	C	PR53B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR39A	8	DI/CSSPI0N	T	PR53A	8	DI/CSSPI0N	T
Y24	PR38B	8	DOUT/CSON	C	PR52B	8	DOUT/CSON	C
Y25	PR38A	8	BUSY/SISPI	T	PR52A	8	BUSY/SISPI	T
W24	PR37B	3	RDQ34	C	PR51B	3	RDQ48	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR37A	3	RDQ34	T	PR51A	3	RDQ48	T
AA26	PR36B	3	RDQ34	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*
Y26	PR36A	3	RDQ34	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*
U21	PR35B	3	RDQ34	C	PR49B	3	RDQ48	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR35A	3	RDQ34	T	PR49A	3	RDQ48	T
W25	PR34B	3	RDQ34	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*
W26	PR34A	3	RDQS34	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR33B	3	RDQ34	C	PR47B	3	RDQ48	C
V25	PR33A	3	RDQ34	T	PR47A	3	RDQ48	T
V26	PR32B	3	RDQ34	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*
U26	PR32A	3	RDQ34	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C	PR45B	3	RLM0_GPLLC_FB_A/RDQ48	C
U23	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T	PR45A	3	RLM0_GPLLT_FB_A/RDQ48	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT57B	1		C	PT66B	1		C
D20	PT57A	1		T	PT66A	1		T
A22	PT56B	1		C	PT65B	1		C
A21	PT56A	1		T	PT65A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	NC	-			NC	-		
C19	NC	-			NC	-		
VCCIO	VCCIO1	1			VCCIO1	1		
B21	NC	-			NC	-		
B20	NC	-			NC	-		
D19	NC	-			NC	-		
B19	NC	-			NC	-		
GND	GNDIO1	-			GNDIO1	-		
G17	NC	-			NC	-		
E18	NC	-			NC	-		
G19	NC	-			NC	-		
F17	NC	-			NC	-		
VCCIO	VCCIO1	1			VCCIO1	1		
A20	NC	-			NC	-		
A19	NC	-			NC	-		
E17	NC	-			NC	-		
D18	NC	-			NC	-		
B18	PT55B	1		C	PT55B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT55A	1		T	PT55A	1		T
E16	PT54B	1		C	PT54B	1		C
G16	PT54A	1		T	PT54A	1		T
F16	PT53B	1		C	PT53B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT53A	1		T	PT53A	1		T
A17	PT52B	1		C	PT52B	1		C
B17	PT52A	1		T	PT52A	1		T
C18	PT51B	1		C	PT51B	1		C
B16	PT51A	1		T	PT51A	1		T
C17	PT50B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT50A	1		T	PT50A	1		T
E15	PT49B	1		C	PT49B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT49A	1		T	PT49A	1		T
A16	PT48B	1		C	PT48B	1		C
B15	PT48A	1		T	PT48A	1		T
D15	PT47B	1		C	PT47B	1		C
F15	PT47A	1		T	PT47A	1		T
A14	PT46B	1		C	PT46B	1		C
B14	PT46A	1		T	PT46A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA14	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C
AE10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T
AF10	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C
W14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T
AB13	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y14	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T
AB14	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C
GND	GNDIO5	-			GNDIO5	-		
AE11	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T
AF11	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C
AD14	PB43A	5	BDQ42	T	PB52A	5	BDQ51	T
AA15	PB43B	5	BDQ42	C	PB52B	5	BDQ51	C
AE12	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T
AF12	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
GND	GNDIO5	-			GNDIO5	-		
AD15	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
AC15	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C
AE13	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AF13	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
AB17	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
GND	GNDIO4	-			GNDIO4	-		
Y15	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AE14	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AF14	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
AA16	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
W15	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
AC17	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
AB16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AE15	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
GND	GNDIO4	-			GNDIO4	-		
AF15	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
AE16	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T
AF16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C
Y16	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T
AB18	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T
AD18	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AC18	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T
AD19	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AC19	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
Y10	VCC	-		
Y11	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
Y20	VCC	-		
J13	VCCIO0	0		
J14	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
K14	VCCIO0	0		
K15	VCCIO0	0		
J17	VCCIO1	1		
J18	VCCIO1	1		
J20	VCCIO1	1		
K17	VCCIO1	1		
K18	VCCIO1	1		
K20	VCCIO1	1		
L21	VCCIO2	2		
M21	VCCIO2	2		
M22	VCCIO2	2		
N21	VCCIO2	2		
N22	VCCIO2	2		
R21	VCCIO2	2		
U21	VCCIO3	3		
U22	VCCIO3	3		
V21	VCCIO3	3		
V22	VCCIO3	3		
W21	VCCIO3	3		
Y22	VCCIO3	3		
AA16	VCCIO4	4		
AA17	VCCIO4	4		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AB17	VCCIO4	4		
AB18	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AA14	VCCIO5	5		
AB12	VCCIO5	5		
AB13	VCCIO5	5		
AB14	VCCIO5	5		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C13	GND	-		
C18	GND	-		
C23	GND	-		
C28	GND	-		
C3	GND	-		
C8	GND	-		
H28	GND	-		
H3	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		
M12	GND	-		
M13	GND	-		
M14	GND	-		
M15	GND	-		
M16	GND	-		
M17	GND	-		
M18	GND	-		
M19	GND	-		
N12	GND	-		
N13	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N18	GND	-		
N19	GND	-		
N28	GND	-		
N3	GND	-		
P11	GND	-		
P12	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P19	GND	-		
P20	GND	-		
R11	GND	-		
R12	GND	-		
R13	GND	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F14	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C(LVDS)*
F13	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
GNDIO	GNDIO2	-			GNDIO2	-		
H11	PR14B	2		C	PR14B	2	RDQ15	C
G11	PR14A	2		T	PR14A	2	RDQ15	T
E13	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C(LVDS)*
F12	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C(LVDS)*
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			VCCIO2	2		
F4	XRES	-			XRES	-		
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y15	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
AA26	NC	-			NC	-		
AB10	PL73B	6	LDQ71	C (LVDS)*	NC	-		
AB11	NC	-			NC	-		
AB12	NC	-			NC	-		
AB13	NC	-			NC	-		
AB14	NC	-			NC	-		
AB15	NC	-			NC	-		
AB16	NC	-			NC	-		
AB17	NC	-			NC	-		
AB19	NC	-			NC	-		
AB20	NC	-			NC	-		
AB21	NC	-			NC	-		
AB9	PL73A	6	LDQ71	T (LVDS)*	NC	-		
AC10	PL74B	6	LDQ71	C	NC	-		
AC11	NC	-			NC	-		
AC21	NC	-			NC	-		
AC22	NC	-			NC	-		
AC8	PL70B	6	LDQ71	C	NC	-		
AC9	PL74A	6	LDQ71	T	NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD4	PL68A	6	LDQ71	T	NC	-		
AD5	PL68B	6	LDQ71	C	NC	-		
AD6	PL71A	6	LDQS71	T (LVDS)*	NC	-		
AD7	PL72A	6	LDQ71	T	NC	-		
AD8	PL72B	6	LDQ71	C	NC	-		
AE23	NC	-			NC	-		
AE5	PL69A	6	LDQ71	T (LVDS)*	NC	-		
AE6	PL70A	6	LDQ71	T	NC	-		
AE7	PL71B	6	LDQ71	C (LVDS)*	NC	-		
AF20	NC	-			NC	-		
AF23	NC	-			NC	-		
AF5	PL69B	6	LDQ71	C (LVDS)*	NC	-		
AG23	NC	-			NC	-		
AG26	NC	-			NC	-		
D10	PT10A	0		T	NC	-		
E10	PT9B	0		C	NC	-		
E11	PT10B	0		C	NC	-		
F10	PT9A	0		T	NC	-		
F20	NC	-			NC	-		
F23	NC	-			NC	-		
F8	PL6B	7	LDQ6	C (LVDS)*	NC	-		
G10	NC	-			NC	-		
G20	NC	-			NC	-		
G21	NC	-			NC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AF11	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AJ14	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4		
AK14	PB67B	4	PCLKC4_0/BDQ69	C
AK15	PB68A	4	VREF2_4/BDQ69	T
AK16	PB68B	4	VREF1_4/BDQ69	C
AF18	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-		
AD16	PB69B	4	BDQ69	C
AJ15	PB70A	4	BDQ69	T
AG16	PB70B	4	BDQ69	C
AE17	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4		
AC17	PB71B	4	BDQ69	C
AH16	PB72A	4	BDQ69	T
AK17	PB72B	4	BDQ69	C
AG20	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-		
AG21	PB73B	4	BDQ69	C
AG18	PB74A	4	BDQ78	T
AJ16	PB74B	4	BDQ78	C
AF21	PB75A	4	BDQ78	T
AG22	PB75B	4	BDQ78	C
AD17	PB76A	4	BDQ78	T
AF19	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
AH17	PB80A	4	BDQ78	T
AJ17	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4		
AF26	PB82A	4	BDQ78	T
AE25	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-		
AD24	PB92A	4	BDQ96	T
AE24	PB92B	4	BDQ96	C
AD18	PB93A	4	BDQ96	T
AC18	PB93B	4	BDQ96	C
AE18	PB94A	4	BDQ96	T
AG19	PB94B	4	BDQ96	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M10	VCCIO7	7		
M7	VCCIO7	7		
N10	VCCIO7	7		
N3	VCCIO7	7		
P10	VCCIO7	7		
R6	VCCIO7	7		
AA25	VCCIO8	8		
AD28	VCCIO8	8		
AA10	VCCAUX	-		
AA11	VCCAUX	-		
AA20	VCCAUX	-		
AA21	VCCAUX	-		
K10	VCCAUX	-		
K11	VCCAUX	-		
K20	VCCAUX	-		
K21	VCCAUX	-		
L10	VCCAUX	-		
L11	VCCAUX	-		
L20	VCCAUX	-		
L21	VCCAUX	-		
Y10	VCCAUX	-		
Y11	VCCAUX	-		
Y20	VCCAUX	-		
Y21	VCCAUX	-		
A1	GND	-		
A13	GND	-		
A18	GND	-		
A24	GND	-		
A30	GND	-		
A7	GND	-		
AA14	GND	-		
AA15	GND	-		
AA16	GND	-		
AA17	GND	-		
AA24	GND	-		
AA27	GND	-		
AA4	GND	-		
AB24	GND	-		
AB7	GND	-		
AD12	GND	-		
AD19	GND	-		
AD27	GND	-		
AE22	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA25	PR74B	3	RDQ73	C	PR82B	3	RDQ81	C
VCCIO	VCCIO3	3			VCCIO3	3		
AC24	PR74A	3	RDQ73	T	PR82A	3	RDQ81	T
AC33	PR73B	3	RDQ73	C (LVDS)*	PR81B	3	RDQ81	C (LVDS)*
AC34	PR73A	3	RDQS73	T (LVDS)*	PR81A	3	RDQS81	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
AB24	PR72B	3	RDQ73	C	PR80B	3	RDQ81	C
Y26	PR72A	3	RDQ73	T	PR80A	3	RDQ81	T
AB33	PR71B	3	RDQ73	C (LVDS)*	PR79B	3	RDQ81	C (LVDS)*
AB34	PR71A	3	RDQ73	T (LVDS)*	PR79A	3	RDQ81	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
Y27	PR70B	3	RDQ73	C	PR78B	3	RDQ81	C
AB29	PR70A	3	RDQ73	T	PR78A	3	RDQ81	T
AA34	PR69B	3	RDQ73	C (LVDS)*	PR77B	3	RDQ81	C (LVDS)*
AA33	PR69A	3	RDQ73	T (LVDS)*	PR77A	3	RDQ81	T (LVDS)*
AA31	PR67B	3	RDQ64	C	PR75B	3	RDQ72	C
AA32	PR67A	3	RDQ64	T	PR75A	3	RDQ72	T
GNDIO	GNDIO3	-			GNDIO3	-		
AA28	PR66B	3	RDQ64	C (LVDS)*	PR74B	3	RDQ72	C (LVDS)*
AA29	PR66A	3	RDQ64	T (LVDS)*	PR74A	3	RDQ72	T (LVDS)*
AA30	PR65B	3	RDQ64	C	PR73B	3	RDQ72	C
AB30	PR65A	3	RDQ64	T	PR73A	3	RDQ72	T
VCCIO	VCCIO3	3			VCCIO3	3		
Y28	PR64B	3	RDQ64	C (LVDS)*	PR72B	3	RDQ72	C (LVDS)*
Y29	PR64A	3	RDQS64	T (LVDS)*	PR72A	3	RDQS72	T (LVDS)*
AA24	PR63B	3	RDQ64	C	PR71B	3	RDQ72	C
GNDIO	GNDIO3	-			GNDIO3	-		
Y25	PR63A	3	RDQ64	T	PR71A	3	RDQ72	T
Y31	PR62B	3	RDQ64	C (LVDS)*	PR70B	3	RDQ72	C (LVDS)*
Y30	PR62A	3	RDQ64	T (LVDS)*	PR70A	3	RDQ72	T (LVDS)*
Y24	PR61B	3	RDQ64	C	PR69B	3	RDQ72	C
VCCIO	VCCIO3	3			VCCIO3	3		
W25	PR61A	3	RDQ64	T	PR69A	3	RDQ72	T
Y33	PR60B	3	RDQ64	C (LVDS)*	PR68B	3	RDQ72	C (LVDS)*
Y34	PR60A	3	RDQ64	T (LVDS)*	PR68A	3	RDQ72	T (LVDS)*
W28	PR58B	3	RLM3_SPLLC_FB_A/RDQ55	C	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-			GNDIO3	-		
V26	PR58A	3	RLM3_SPLLT_FB_A/RDQ55	T	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
V28	PR57B	3	RLM3_SPLLC_IN_A/RDQ55	C (LVDS)*	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
V27	PR57A	3	RLM3_SPLLT_IN_A/RDQ55	T (LVDS)*	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
V25	PR56B	3	RDQ55	C	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3			VCCIO3	3		
W24	PR56A	3	RDQ55	T	PR64A	3	RDQ63	T
W33	PR55B	3	RDQ55	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*
W34	PR55A	3	RDQS55	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
V24	PR54B	3	RDQ55	C	PR62B	3	RDQ63	C
U26	PR54A	3	RDQ55	T	PR62A	3	RDQ63	T
W29	PR53B	3	RDQ55	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*