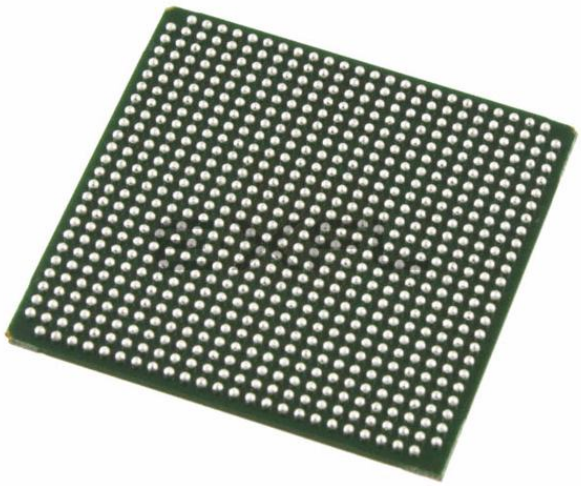

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

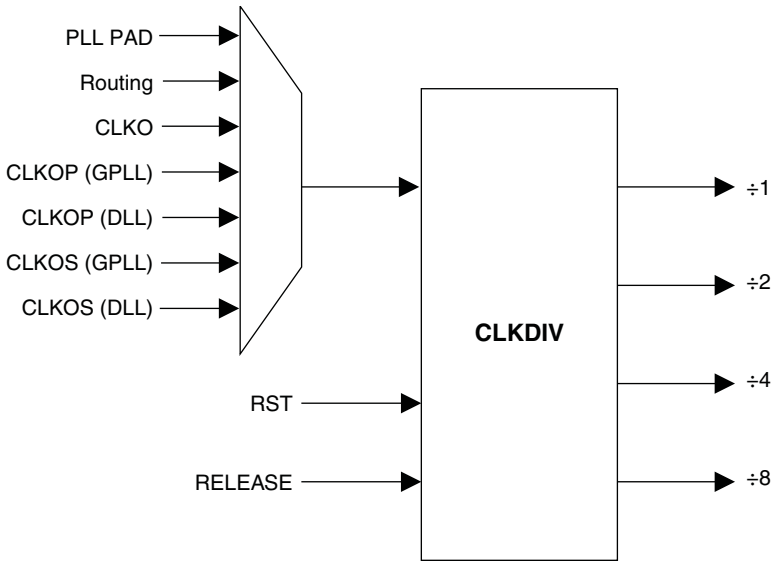
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-6f672c

Figure 2-9. Clock Divider Connections



Clock Distribution Network

LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

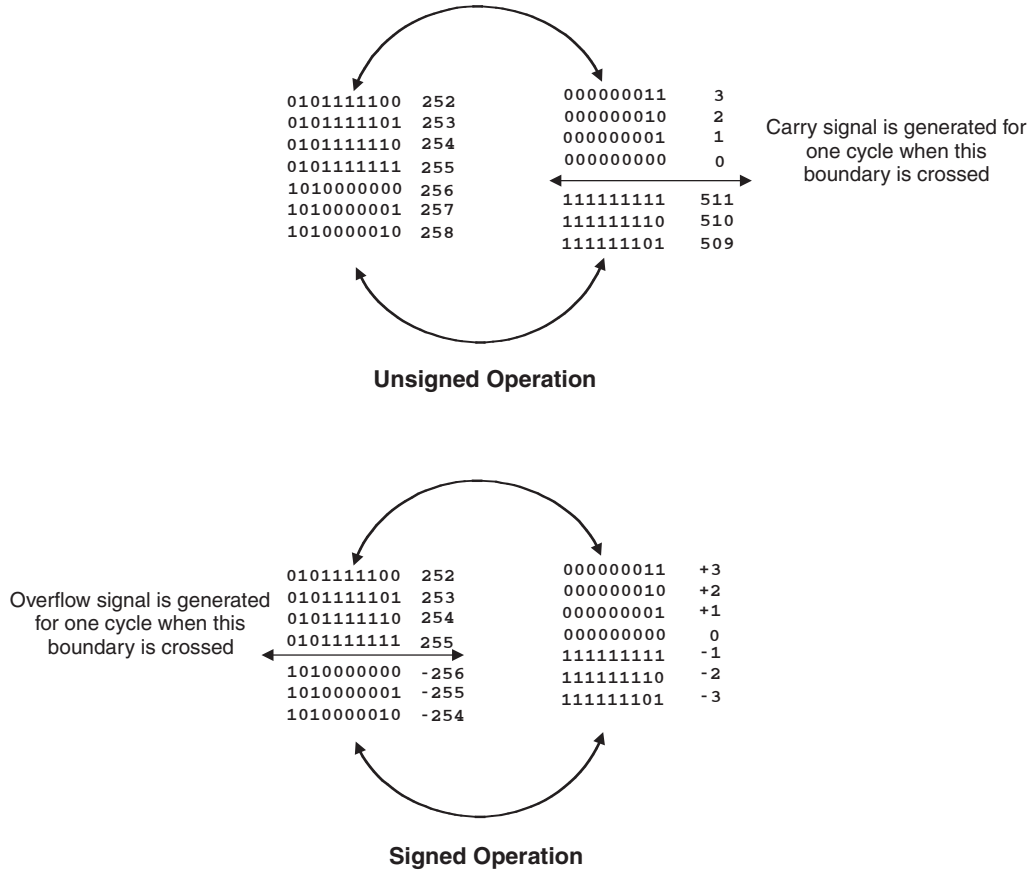
Table 2-8. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	000000000000000101	0101	000000101	000000000000000101
-6	N/A	N/A	N/A	1010	111111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, "roll-over" is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-27.

Figure 2-27. Accumulator Overflow/Underflow



DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysI/O Buffer Banks

LatticeECP2/M devices have nine sysI/O buffer banks: eight banks for user I/Os arranged two per side. The ninth sysI/O buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2}, with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

LatticeECP2 Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5, 6, 7]	Units
I_{CC}	Core Power Supply Current	ECP2-6	34	mA
		ECP2-12	54	mA
		ECP2-20	82	mA
		ECP2-35	135	mA
		ECP2-50	187	mA
		ECP2-70	267	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	30	mA
		ECP2-12	30	mA
		ECP2-20	30	mA
		ECP2-35	30	mA
		ECP2-50	30	mA
		ECP2-70	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.
2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

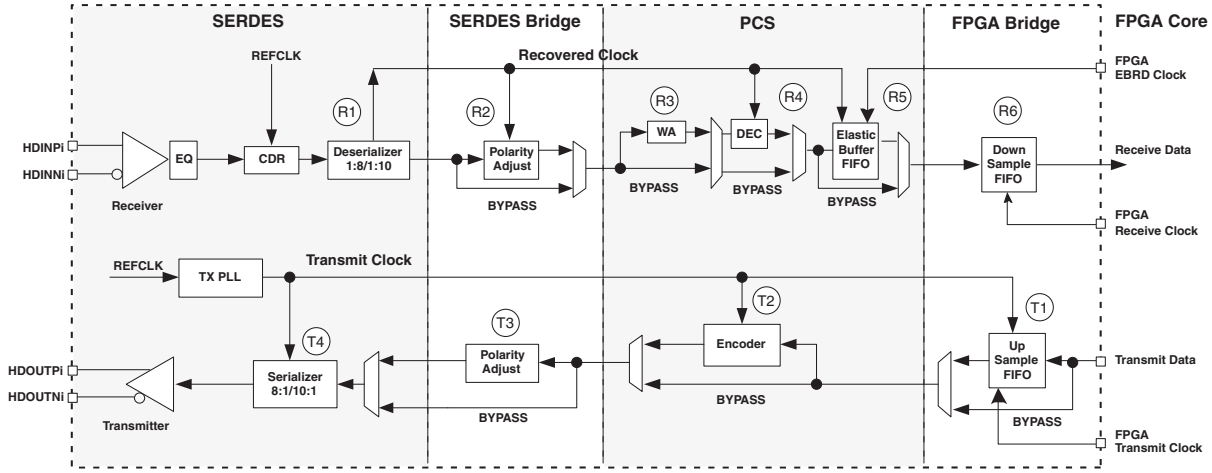
Register-to-Register Performance (Continued)

Function	-7 Timing	Units
36x36 Multiplier (All Registers)	372	MHz
18x18 Multiplier/Accumulate (Input and Output Registers)	295	MHz
18x18 Multiplier-Add/Sub-Sum (All Registers)	420	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	304	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	227	MHz
8x8 Matrix Multiplier	223	MHz

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

Figure 3-12. Transmitter and Receiver Block Diagram



LatticeECP2/M sysCONFIG Port Timing Specifications (Continued)

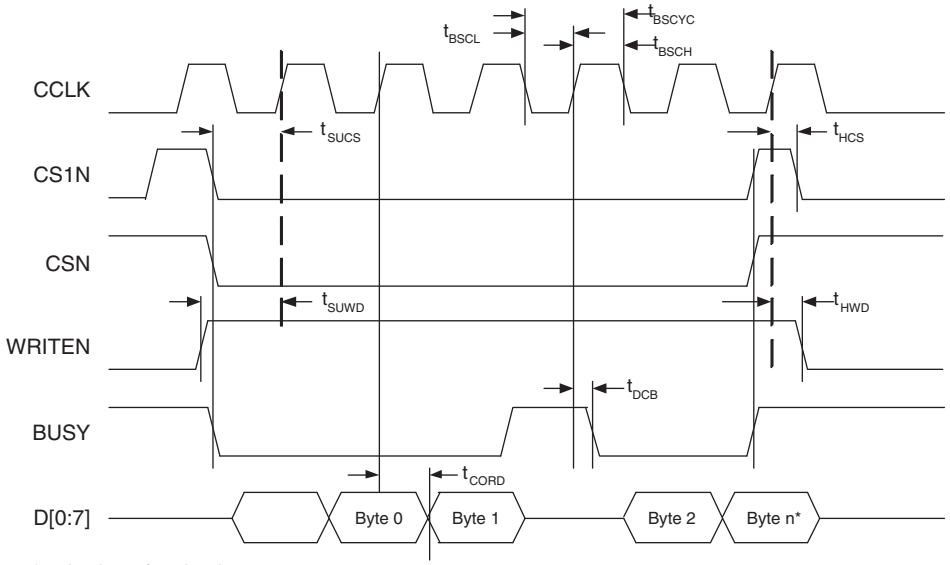
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
f_{MAXSPI}	Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1)	—	20	MHz
	Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0)	—	50	MHz
	Max. CCLK Frequency - Encrypted Bitstream	—	10	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	2	—	ns
t_{SUMCDI}	DI Setup to CCLK	7	—	ns
t_{HMCDI}	DI Hold from CCLK	1	—	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.
2. For SED (Soft Error Detect), the SEDCLKIN operating frequency must be at least 20MHz. SEDCLKIN is derived from Master Clock Frequency that has a +/-30% variation..

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
Duty Cycle	40	60	%

Figure 3-14. sysCONFIG Parallel Port Read Cycle



*n = last byte of read cycle.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See "Typical sysI/O I/O Behavior During Power-up" for more information about I/O behavior during power-up.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{CCPLL}	—	PLL supply pins. Should be tied to V_{CC} even when the corresponding PLL is unused.
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
XRES[4]	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP[4]	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V_{CCPLL}	—	Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A[5]	I	Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A[5]	I	Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70 (Cont.)

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	2	3	3	4
	Bank3	0	3	3	3
	Bank4	3	4	4	4
	Bank5	3	4	4	5
	Bank6	1	4	4	4
	Bank7	2	3	3	4
	Bank8	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0
	Bank1	0	0	0	0
	Bank2	0	0	0	0
	Bank3	0	0	0	0
	Bank4	46	62	62	72
	Bank5	46	68	68	80
	Bank6	0	0	0	0
	Bank7	0	0	0	0
	Bank8	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2 Power Supply and NC (Cont.)

Signals	672 fpBGA[3]	900 fpBGA[3]
VCC	**LFE2-20:** R8, P18, M8, L20, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 **LFE2-35/LFE2-50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 **LFE2-70:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	AA11, AA20, K11, K21, K22, L11, L12, L13, L18, L19, L20, M11, M20, N11, N20, V11, V20, W11, W20, Y10, Y11, Y12, Y13, Y18, Y19, Y20
VCCIO0	D11, D6, G9, J12, K12	J13, J14, K12, K13, K14, K15
VCCIO1	D16, D21, G18, J15, K15	J17, J18, J20, K17, K18, K20
VCCIO2	F23, J20, L23, M17, M18	L21, M21, M22, N21, N22, R21
VCCIO3	AA23, R17, R18, T23, V20	U21, U22, V21, V22, W21, Y22
VCCIO4	AC16, AC21, U15, V15, Y18	AA16, AA17, AA18, AA19, AB17, AB18
VCCIO5	AC11, AC6, U12, V12, Y9	AA12, AA13, AA14, AB12, AB13, AB14
VCCIO6	AA4, R10, R9, T4, V7	U10, U9, V10, W10, W9, Y9
VCCIO7	F4, J7, L4, M10, M9	L10, L9, M10, N10, P10, R10
VCCIO8	AE25, V18	AA21, Y21
VCCJ	AB5	AD3
VCCAUX	J10, J11, J16, J17, K18, L18, T18, U18, V16, V17, V10, V11, T9, U9, K9, L9	AA15, AB11, AB19, AB20, J11, J12, J19, K19, L22, M9, N9, P21, P9, T10, T21, V9, W22
VCCPLL	**LFE2-20:** None **LFE2-35/LFE2-70:** R8, P18 **LFE2-50:** R8, P18, M8, L20	P22, P8, T22, Y7
GND[1]	A2, A25, AA18, AA24, AA3, AA9, AD11, AD16, AD21, AD6, AE1, AE26, AF2, AF25, B1, B26, C11, C16, C21, C6, F18, F24, F3, F9, J13, J14, J21, J6, K10, K11, K13, K14, K16, K17, L10, L11, L16, L17, L24, L3, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T24, T3, U10, U11, U13, U14, U16, U17, V13, V14, V21, V6	A1, A30, AC28, AC3, AH13, AH18, AH23, AH28, AH3, AH8, AK1, AK30, C13, C18, C23, C28, C3, C8, H28, H3, L14, L15, L16, L17, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, N28, N3, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V12, V13, V14, V15, V16, V17, V18, V19, V28, V3, W12, W13, W14, W15, W16, W17, W18, W19, Y14, Y15, Y16, Y17
NC[2]	**LFE2-20:** E4, E3, E2, E1, H6, H5, F2, F1, H8, J9, G4, G3, K3, K2, K1, L2, L1, M2, M1, N2, T1, T2, P8, P6, P5, P4, U1, V1, P3, R3, R4, U2, V2, W2, T6, R5, AA19, W17, Y19, Y17, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, R22, T21, P26, P25, R24, R23, P20, R19, P21, P19, P23, P22, N22, R21, N26, N25, J26, J25, J23, K23, H26, H25, H24, H23, F22, E24, D25, C25, D24, B25, H21, G22, B24, C24, D23, C23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24 **LFE2-35:** K3, K2, K1, L2, L1, M2, M1, N2, M8, P3, R3, R4, U2, V2, W2, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, P26, P25, R24, R23, P20, R19, L20, J26, J25, J23, K23, H26, H25, H24, H23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24 **LFE2-50:** N6, P24, M3 **LFE2-70:** M8, L20, M3, P24, N6	A2, A3, A4, A5, AB28, AC4, AD23, AE1, AE2, AE29, AE3, AE30, AE4, AE5, AE6, AF1, AF2, AF23, AF26, AF27, AF28, AF29, AF3, AF30, AF4, AF5, AG1, AG13, AG16, AG18, AG2, AG26, AG27, AG28, AG29, AG3, AG30, AG4, AG8, AH1, AH16, AH2, AH26, AH27, AH29, AH30, AH4, AJ1, AJ2, AJ27, AJ28, AJ29, AJ3, AJ30, AK2, AK27, AK28, AK29, AK3, B1, B2, B3, B30, B4, B5, C1, C2, C29, C30, C4, D13, D18, D23, D28, D29, D3, D30, D4, E25, E26, E27, E28, E29, E3, E30, E4, E5, E6, F25, F5, F6, G6, G7, K10, K9, N27, N4, R1, R2, V27, V4

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
V_{CC}	**LFE2M35:** AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 **LFE2M50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	**LFE2M50:** AH1, AH4, AH5, AH2, AH7, AH12, AH9, AH10, AH13, C13, C10, C9, C12, C7, C2, C5, C4, C1, L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19 **LFE2M70/LFE2M100:** L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19
V_{CCIO0}	B12, B7, F11, J13, K12	D14, E6, E9, F12, K12, K13
V_{CCIO1}	D18, F16, J14, K15	D17, E22, E25, F19, K18, K19
V_{CCIO2}	G25, L21, M17, M25, N18	F28, J25, K28, M21, M24, N21, N28, P21, R25
V_{CCIO3}	P18, R17, R25, T21, Y25	AA28, AB25, AE28, T25, U21, V21, V28, W21, W24
V_{CCIO4}	AA16, AC18, U15, V14	AA18, AA19, AE19, AF22, AG17, AG25
V_{CCIO5}	AA11, AE12, AE7, U12, V13	AA12, AA13, AE12, AF9, AG14, AG6
V_{CCIO6}	P9, R10, R2, T6, Y2	AA3, AB6, AE3, T6, U10, V10, V3, W10, W7
V_{CCIO7}	G2, L6, M10, M2, N9	F3, J6, K3, M10, M7, N10, N3, P10, R6
V_{CCIO8}	AC24, U17	AA25, AD28
V_{CCJ}	AA7	AG1
V_{CCAUX}	**LFE2M35:** AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16 **LFE2M50:** J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16	**LFE2M50:** AJ7, B7, AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21 **LFE2M70/LFE2M100:** AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21
V_{CCPLL}	H7, K6, P7, R8, V18, P20, J17, G19	N13, N18, V13, V18
SERDES Power[3]	**LFE2M35:** C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13 **LFE2M50:** AD13, AE13, AD16, AF16, AD17, AD18, AD14, AD15, AD19, AE19, AD23, AD24, AD20, AD21, AF22, AD22, AE25, AD25, C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13	**LFE2M50:** AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18 **LFE2M70/LFE2M100:** C13, B13, C10, A10, C9, C8, C12, C11, B7, C7, C3, C2, C6, C5, A4, C4, B1, C1, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18, AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, AH1, AJ1, AH4, AK4, AH5, AH6, AH2, AH3, AH7, AJ7, AH11, AH12, AH8, AH9, AK10, AH10, AJ13, AH13

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M8	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
P7	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
R8	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
VCCIO	VCCIO4	4			VCCIO4	4		
T5	PB14A	4	BDQ15	T	PB32A	4	BDQ33	T
T6	PB14B	4	BDQ15	C	PB32B	4	BDQ33	C
T8	PB15A	4	BDQS15	T	PB33A	4	BDQS33	T
GND	GNDIO4	-			GNDIO4	-		
R7	PB16A	4	BDQ15	T	PB34A	4	BDQ33	T
T9	PB15B	4	BDQ15	C	PB33B	4	BDQ33	C
T7	PB16B	4	BDQ15	C	PB34B	4	BDQ33	C
L8	PB17A	4	BDQ15	T	PB35A	4	BDQ33	T
VCCIO	VCCIO4	4			VCCIO4	4		
P8	PB18A	4	BDQ15	T	PB36A	4	BDQ33	T
L9	PB17B	4	BDQ15	C	PB35B	4	BDQ33	C
N8	PB18B	4	BDQ15	C	PB36B	4	BDQ33	C
R9	PB19A	4	BDQ15	T	PB37A	4	BDQ33	T
GND	GNDIO4	-			GNDIO4	-		
R10	PB19B	4	BDQ15	C	PB37B	4	BDQ33	C
-	-	-			VCCIO	4		
-	-	-			GNDIO4	4		
N9	PB20A	4	BDQ24	T	PB47A	4	BDQ51	T
T10	PB21A	4	BDQ24	T	PB48A	4	BDQ51	T
M9	PB20B	4	BDQ24	C	PB47B	4	BDQ51	C
R11	PB21B	4	BDQ24	C	PB48B	4	BDQ51	C
P10	PB22A	4	BDQ24	T	PB49A	4	BDQ51	T
N11	PB23A	4	BDQ24	T	PB50A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
N10	PB22B	4	BDQ24	C	PB49B	4	BDQ51	C
P11	PB23B	4	BDQ24	C	PB50B	4	BDQ51	C
T11	PB24A	4	BDQS24	T	PB51A	4	BDQS51	T
GND	GNDIO4	-			GNDIO4	-		
M11	PB25A	4	BDQ24	T	PB52A	4	BDQ51	T
T12	PB24B	4	BDQ24	C	PB51B	4	BDQ51	C
L11	PB25B	4	BDQ24	C	PB52B	4	BDQ51	C
T13	PB26A	4	BDQ24	T	PB53A	4	BDQ51	T
R13	PB27A	4	BDQ24	T	PB54A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
T14	PB26B	4	BDQ24	C	PB53B	4	BDQ51	C
P13	PB27B	4	BDQ24	C	PB54B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
N12	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
M12	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
R15	CFG2	8			CFG2	8		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
H16	NC	-			NC	-		
H20	NC	-			NC	-		
H18	NC	-			NC	-		
K6	NC	-			NC	-		
J16	NC	-			NC	-		
N18	VCC	-			VCC	-		
N6	VCC	-			VCC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR18B	2	RDQ16	C (LVDS)*	PR24B	2	RDQ22	C (LVDS)*
K22	PR18A	2	RDQ16	T (LVDS)*	PR24A	2	RDQ22	T (LVDS)*
M24	PR17B	2	RDQ16	C	PR23B	2	RDQ22	C
N23	PR17A	2	RDQ16	T	PR23A	2	RDQ22	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR16B	2	RDQ16	C (LVDS)*	PR22B	2	RDQ22	C (LVDS)*
K25	PR16A	2	RDQS16	T (LVDS)*	PR22A	2	RDQS22	T (LVDS)*
M20	PR15B	2	RDQ16	C	PR21B	2	RDQ22	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR15A	2	RDQ16	T	PR21A	2	RDQ22	T
L22	PR14B	2	RDQ16	C (LVDS)*	PR20B	2	RDQ22	C (LVDS)*
M22	PR14A	2	RDQ16	T (LVDS)*	PR20A	2	RDQ22	T (LVDS)*
K21	PR13B	2	RDQ16	C	PR19B	2	RDQ22	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR13A	2	RDQ16	T	PR19A	2	RDQ22	T
K24	PR12B	2	RDQ16	C (LVDS)*	PR18B	2	RDQ22	C (LVDS)*
J24	PR12A	2	RDQ16	T (LVDS)*	PR18A	2	RDQ22	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	NC	-			NC	-		
J25	NC	-			NC	-		
J23	NC	-			NC	-		
K23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
H26	NC	-			NC	-		
H25	NC	-			NC	-		
H24	NC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
H23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR11B	2	RDQ8	C	PR17B	2	RDQ14	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR11A	2	RDQ8	T	PR17A	2	RDQ14	T
F26	PR10B	2	RDQ8	C (LVDS)*	PR16B	2	RDQ14	C (LVDS)*
F25	PR10A	2	RDQ8	T (LVDS)*	PR16A	2	RDQ14	T (LVDS)*
K20	PR9B	2	RDQ8	C	PR15B	2	RDQ14	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR9A	2	RDQ8	T	PR15A	2	RDQ14	T
E26	PR8B	2	RDQ8	C (LVDS)*	PR14B	2	RDQ14	C (LVDS)*
E25	PR8A	2	RDQS8	T (LVDS)*	PR14A	2	RDQS14	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR7B	2	RDQ8	C	PR13B	2	RDQ14	C
H22	PR7A	2	RDQ8	T	PR13A	2	RDQ14	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C13	GND	-		
C18	GND	-		
C23	GND	-		
C28	GND	-		
C3	GND	-		
C8	GND	-		
H28	GND	-		
H3	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		
M12	GND	-		
M13	GND	-		
M14	GND	-		
M15	GND	-		
M16	GND	-		
M17	GND	-		
M18	GND	-		
M19	GND	-		
N12	GND	-		
N13	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N18	GND	-		
N19	GND	-		
N28	GND	-		
N3	GND	-		
P11	GND	-		
P12	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P19	GND	-		
P20	GND	-		
R11	GND	-		
R12	GND	-		
R13	GND	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
T2	PL45B	6	LLM3_SPLLC_IN_A	C (LVDS)*	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*
U9	PL46A	6	LLM3_SPLLT_FB_A	T	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T
U8	PL46B	6	LLM3_SPLLC_FB_A	C	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C
VCCIO	VCCIO6	6			GNDIO6	-		
U5	PL48A	6	LDQ52	T (LVDS)*	PL60A	6	LDQ64	T (LVDS)*
U4	PL48B	6	LDQ52	C (LVDS)*	PL60B	6	LDQ64	C (LVDS)*
V9	PL49A	6	LDQ52	T	PL61A	6	LDQ64	T
V7	PL49B	6	LDQ52	C	PL61B	6	LDQ64	C
VCCIO	VCCIO6	6			VCCIO6	6		
U3	PL50A	6	LDQ52	T (LVDS)*	PL62A	6	LDQ64	T (LVDS)*
U2	PL50B	6	LDQ52	C (LVDS)*	PL62B	6	LDQ64	C (LVDS)*
V8	PL51A	6	LDQ52	T	PL63A	6	LDQ64	T
U6	PL51B	6	LDQ52	C	PL63B	6	LDQ64	C
GNDIO	GNDIO6	-			GNDIO6	-		
U1	PL52A	6	LDQS52	T (LVDS)*	PL64A	6	LDQS64	T (LVDS)*
V2	PL52B	6	LDQ52	C (LVDS)*	PL64B	6	LDQ64	C (LVDS)*
V5	PL53A	6	LDQ52	T	PL65A	6	LDQ64	T
VCCIO	VCCIO6	6			VCCIO6	6		
V6	PL53B	6	LDQ52	C	PL65B	6	LDQ64	C
V1	PL54A	6	LDQ52	T (LVDS)*	PL66A	6	LDQ64	T (LVDS)*
W1	PL54B	6	LDQ52	C (LVDS)*	PL66B	6	LDQ64	C (LVDS)*
W5	PL55A	6	LDQ52	T	PL67A	6	LDQ64	T
GNDIO	GNDIO6	-			GNDIO6	-		
W6	PL55B	6	LDQ52	C	PL67B	6	LDQ64	C
W3	PL57A	6		T (LVDS)*	PL69A	6	LDQ73	T (LVDS)*
W4	PL57B	6		C (LVDS)*	PL69B	6	LDQ73	C (LVDS)*
W2	PL58A	6		T	PL70A	6	LDQ73	T
Y4	PL58B	6		C	PL70B	6	LDQ73	C
Y1	PL59A	6		T (LVDS)*	PL71A	6	LDQ73	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
Y2	PL59B	6		C (LVDS)*	PL71B	6	LDQ73	C (LVDS)*
Y5	PL60A	6		T	PL72A	6	LDQ73	T
Y6	PL60B	6		C	PL72B	6	LDQ73	C
AA1	NC	-			PL73A	6	LDQS73	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AA2	NC	-			PL73B	6	LDQ73	C (LVDS)*
Y3	NC	-			PL74A	6	LDQ73	T
AB1	NC	-			PL74B	6	LDQ73	C
-	-	-			VCCIO6	6		
Y9	NC	-			PL75A	6	LDQ73	T (LVDS)*
Y8	NC	-			PL75B	6	LDQ73	C (LVDS)*
Y7	NC	-			PL76A	6	LDQ73	T
AA7	NC	-			PL76B	6	LDQ73	C
-	-	-			GNDIO6	-		
-	-	-			-	-		
AB2	NC	-			PL78A	6	LDQ82	T (LVDS)*
AB3	NC	-			PL78B	6	LDQ82	C (LVDS)*
AA5	NC	-			PL79A	6	LDQ82	T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A21	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
D23	PT73B	1		C	PT82B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
E21	PT73A	1		T	PT82A	1		T
D26	PT72B	1		C	PT81B	1		C
E26	PT72A	1		T	PT81A	1		T
E23	PT71B	1		C	PT80B	1		C
-	-	-			VCCIO1	1		
G22	PT71A	1		T	PT80A	1		T
VCCIO	VCCIO1	1			-	-		
D22	PT70B	1		C	PT79B	1		C
F21	PT70A	1		T	PT79A	1		T
G18	PT69B	1		C	PT78B	1		C
H18	PT69A	1		T	PT78A	1		T
D20	PT68B	1		C	PT77B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
D21	PT68A	1		T	PT77A	1		T
E20	PT67B	1		C	PT76B	1		C
E19	PT67A	1		T	PT76A	1		T
D19	PT66B	1		C	PT75B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
E18	PT66A	1		T	PT75A	1		T
D18	PT65B	1		C	PT74B	1		C
C17	PT65A	1		T	PT74A	1		T
A17	PT64B	1		C	PT73B	1		C
B17	PT64A	1		T	PT73A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
J18	NC	-			PT66B	1		C
J19	NC	-			PT66A	1		T
H17	NC	-			PT65B	1		C
J17	NC	-			PT65A	1		T
F18	NC	-			PT64B	1		C
F17	NC	-			PT64A	1		T
-	-	-			GNDIO1	-		
A16	PT54B	1		C	PT63B	1		C
B16	PT54A	1		T	PT63A	1		T
G17	PT53B	1		C	PT62B	1		C
G16	PT53A	1		T	PT62A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
H16	PT52B	1		C	PT61B	1		C
F16	PT52A	1		T	PT61A	1		T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E13	PT28A	0		T	PT37A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
GNDIO	GNDIO0	-			GNDIO0	-		
J12	PT5B	0		C	PT31B	0		C
GNDIO	GNDIO0	-			-	-		
VCCIO	VCCIO0	0			VCCIO0	0		
H10	PT5A	0		T	PT31A	0		T
E12	PT4B	0		C	PT30B	0		C
D11	PT4A	0		T	PT30A	0		T
H11	PT3B	0		C	PT29B	0		C
F11	PT3A	0		T	PT29A	0		T
C13	VCC	-			ULC_SQ_VCCRX0	11		
A12	PT19A	0		T	ULC_SQ_HDINP0	11		T
B13	NC	-			ULC_SQ_VCCIB0	11		
B12	PT19B	0		C	ULC_SQ_HDINN0	11		C
C10	VCC	-			ULC_SQ_VCCTX0	11		
A9	PT17A	0		T	ULC_SQ_HDOUTP0	11		T
A10	NC	-			ULC_SQ_VCCOB0	11		
B9	PT17B	0		C	ULC_SQ_HDOUTN0	11		C
C9	VCC	-			ULC_SQ_VCCTX1	11		
B8	PT18B	0		C	ULC_SQ_HDOUTN1	11		C
C8	NC	-			ULC_SQ_VCCOB1	11		
A8	PT18A	0		T	ULC_SQ_HDOUTP1	11		T
C12	VCC	-			ULC_SQ_VCCRX1	11		
B11	PT16B	0		C	ULC_SQ_HDINN1	11		C
C11	NC	-			ULC_SQ_VCCIB1	11		
A11	PT16A	0		T	ULC_SQ_HDINP1	11		T
B7	VCCAUX	-			ULC_SQ_VCCAUX33	11		
E7	PT15B	0		C	ULC_SQ_REFCLKN	11		C
D7	PT15A	0		T	ULC_SQ_REFCLKP	11		T
C7	VCC	-			ULC_SQ_VCCP	11		
A3	PT12A	0		T	ULC_SQ_HDINP2	11		T
C3	NC	-			ULC_SQ_VCCIB2	11		
B3	PT12B	0		C	ULC_SQ_HDINN2	11		C
C2	VCC	-			ULC_SQ_VCCRX2	11		
A6	PT14A	0		T	ULC_SQ_HDOUTP2	11		T
C6	NC	-			ULC_SQ_VCCOB2	11		
B6	PT14B	0		C	ULC_SQ_HDOUTN2	11		C
C5	VCC	-			ULC_SQ_VCCTX2	11		
B5	PT13B	0		C	ULC_SQ_HDOUTN3	11		C
A4	NC	-			ULC_SQ_VCCOB3	11		
A5	PT13A	0		T	ULC_SQ_HDOUTP3	11		T
C4	VCC	-			ULC_SQ_VCCTX3	11		
B2	PT11B	0		C	ULC_SQ_HDINN3	11		C
B1	NC	-			ULC_SQ_VCCIB3	11		
A2	PT11A	0		T	ULC_SQ_HDINP3	11		T
C1	VCC	-			ULC_SQ_VCCRX3	11		
L12	VCC	-			VCC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		