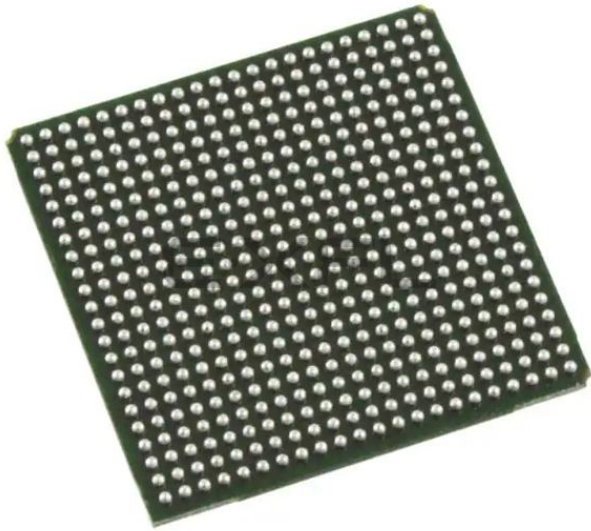




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	331
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-6fn484i

Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing blocks, as shown in Figure 2-1. In addition, the LatticeECP2M family contains SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP2/M devices are arranged in eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as SPI4.2, along with memory interfaces including DDR2.

The LatticeECP2/M registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block is located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. The Ball Grid Array (BGA) package devices in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator. The LatticeECP2/M devices use 1.2V as their core voltage.

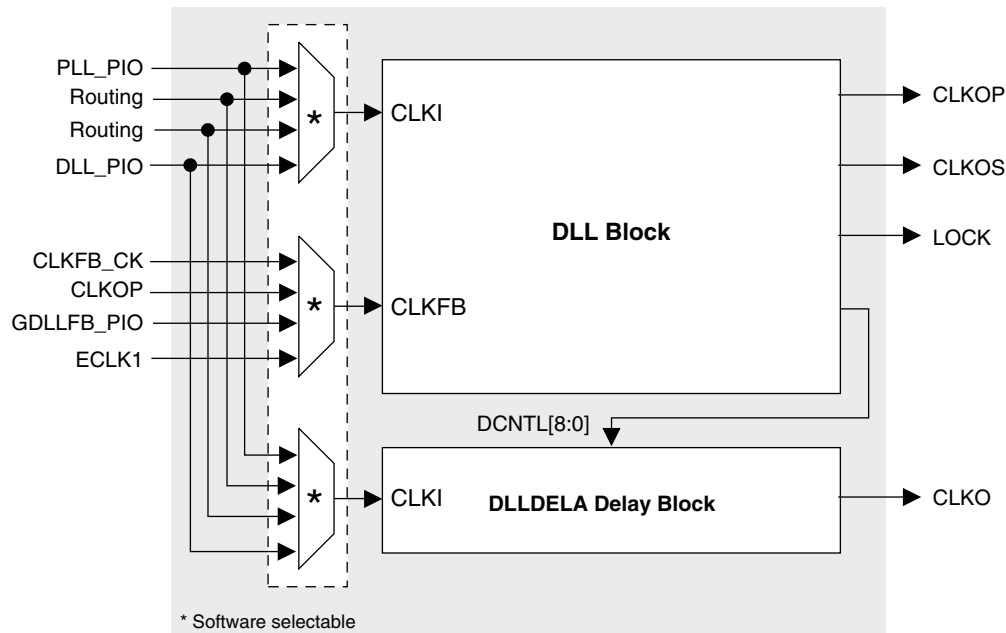
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-7. DLLDELA Delay Block



PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

LatticeECP2/M DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2/M family.

Table 2-11. DSP Performance

Device	DSP Block	DSP Performance GMAC
ECP2-6	3	3.9
ECP2-12	6	7.8
ECP2-20	7	9.1
ECP2-35	8	10.4
ECP2-50	18	23.4
ECP2-70	22	28.6
ECP2M20	6	7.8
ECP2M35	8	10.4
ECP2M50	22	28.6
ECP2M70	24	31.2
ECP2M100	42	54.6

For further information about the sysDSP block, please see the list of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-28. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-12 provides the PIO signal list.

LatticeECP2/M Internal Switching Characteristics¹

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.180	—	0.198	—	0.216	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.331	—	0.358	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.600	—	0.655	—	0.711	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.128	—	0.129	—	0.129	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.051	—	-0.049	—	-0.046	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.071	—	0.081	—	ns
t _{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.285	—	0.309	—	0.333	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.902	—	1.083	—	1.263	ns
t _{SUDATA_PFU}	Data Setup Time	-0.172	—	-0.205	—	-0.238	—	ns
t _{HDATA_PFU}	Data Hold Time	0.199	—	0.235	—	0.271	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.245	—	-0.284	—	-0.323	—	ns
t _{HADDR_PFU}	Address Hold Time	0.246	—	0.285	—	0.324	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.122	—	-0.145	—	-0.168	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.132	—	0.156	—	0.180	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.613	—	0.681	—	0.749	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.115	—	1.343	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.51	—	2.75	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.33	—	0.36	—	0.39	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.157	—	-0.181	—	-0.205	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.173	—	0.195	—	0.217	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.115	—	-0.130	—	-0.145	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.138	—	0.155	—	0.172	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.128	—	-0.149	—	-0.170	—	ns

LatticeECP2/M Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t _{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t _{RSTREC_SPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t _{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t _{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t _{HP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t _{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t _{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
t _{SUADDSUB}	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
t _{HADDSUB}	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Single Ended User I/O		339	500	500	583
Differential Pair User I/O		169	249	249	290
Configuration	TAP Pins	5	5	5	5
	Muxed Pins	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7
Non Configuration	Muxed Pins	68	79	79	89
	Dedicated Pins	3	3	3	3
VCC		16	20	20	26
VCCAUX		16	16	16	17
VCCPLL		4	4	2	4
VCCIO	Bank0	4	5	5	6
	Bank1	4	5	5	6
	Bank2	4	5	5	6
	Bank3	4	5	5	6
	Bank4	4	5	5	6
	Bank5	4	5	5	6
	Bank6	4	5	5	6
	Bank7	4	5	5	6
	Bank8	2	2	2	2
GND, GND0 to GND7		60	72	72	104
NC		0	3	5	101
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	50/25	67/33	67/33	84/42
	Bank1	46/23	66/33	66/33	76/38
	Bank2	38/19	56/28	56/28	74/37
	Bank3	22/11	48/24	48/24	48/24
	Bank4	46/23	62/31	62/31	72/35
	Bank5	46/23	68/34	68/34	80/40
	Bank6	40/20	64/32	64/32	64/32
	Bank7	37/18	55/27	55/27	71/35
	Bank8	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0
	Bank2 (Right Edge)	9	13	13	18
	Bank3 (Right Edge)	5	12	12	12
	Bank4 (Bottom Edge)	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0
	Bank6 (Left Edge)	10	16	16	16
	Bank7 (Left Edge)	8	12	12	16
	Bank8 (Right Edge)	0	0	0	0

LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 (Cont.)

Pin Type		LFE2M50			LFE2M70		LFE2M100	
		484 fpBGA	672 fpBGA	900 fpBGA	900 fpBGA	1152 fpBGA	900 fpBGA	1152 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	2	2	2	4	4	4	4
	Bank3	2	1	1	3	4	3	5
	Bank4	3	1	3	3	3	3	3
	Bank5	2	3	3	2	3	2	3
	Bank6	1	2	2	3	4	3	5
	Bank7	3	3	3	4	4	4	5
	Bank8	0	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	0	0	0	0	72	0	80
	Bank3	0	0	0	0	64	0	80
	Bank4	50	24	48	48	40	48	44
	Bank5	60	60	50	40	40	40	46
	Bank6	52	54	60	62	66	62	82
	Bank7	60	60	68	70	74	70	90
	Bank8	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
V _{CC}	LFE2M35: AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 LFE2M50: L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	LFE2M50: AH1, AH4, AH5, AH2, AH7, AH12, AH9, AH10, AH13, C13, C10, C9, C12, C7, C2, C5, C4, C1, L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19 LFE2M70/LFE2M100: L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19
V _{CCIO0}	B12, B7, F11, J13, K12	D14, E6, E9, F12, K12, K13
V _{CCIO1}	D18, F16, J14, K15	D17, E22, E25, F19, K18, K19
V _{CCIO2}	G25, L21, M17, M25, N18	F28, J25, K28, M21, M24, N21, N28, P21, R25
V _{CCIO3}	P18, R17, R25, T21, Y25	AA28, AB25, AE28, T25, U21, V21, V28, W21, W24
V _{CCIO4}	AA16, AC18, U15, V14	AA18, AA19, AE19, AF22, AG17, AG25
V _{CCIO5}	AA11, AE12, AE7, U12, V13	AA12, AA13, AE12, AF9, AG14, AG6
V _{CCIO6}	P9, R10, R2, T6, Y2	AA3, AB6, AE3, T6, U10, V10, V3, W10, W7
V _{CCIO7}	G2, L6, M10, M2, N9	F3, J6, K3, M10, M7, N10, N3, P10, R6
V _{CCIO8}	AC24, U17	AA25, AD28
V _{CCJ}	AA7	AG1
V _{CCAUX}	LFE2M35: AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16 LFE2M50: J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16	LFE2M50: AJ7, B7, AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21 LFE2M70/LFE2M100: AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21
V _{CCPLL}	H7, K6, P7, R8, V18, P20, J17, G19	N13, N18, V13, V18
SERDES Power ³	LFE2M35: C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13 LFE2M50: AD13, AE13, AD16, AF16, AD17, AD18, AD14, AD15, AD19, AE19, AD23, AD24, AD20, AD21, AF22, AD22, AE25, AD25, C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13	LFE2M50: AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18 LFE2M70/LFE2M100: C13, B13, C10, A10, C9, C8, C12, C11, B7, C7, C3, C2, C6, C5, A4, C4, B1, C1, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18, AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, AH1, AJ1, AH4, AK4, AH5, AH6, AH2, AH3, AH7, AJ7, AH11, AH12, AH8, AH9, AK10, AH10, AJ13, AH13

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A5	A5	PT36B	0		C
A3	A3	PT35B	0		C
A4	A4	PT36A	0		T
VCCIO	VCCIO	VCCIO0	0		
B3	B3	PT35A	0		T
A2	A2	PT34B	0		C
C7	C7	PT33B	0		C
B2	B2	PT34A	0		T
D7	D7	PT33A	0		T
D6	D6	PT32B	0		C
GND	GND	GNDIO0	-		
F7	F7	PT31B	0		C
C6	C6	PT32A	0		T
VCCIO	VCCIO	VCCIO0	0		
F6	F6	PT31A	0		T
C4	C4	PT30B	0		C
B4	B4	PT30A	0		T
-	GND	GNDIO0	0		
-	VCC	VCCIO	0		
D5	D5	PT2B	0	VREF2_0	C
E5	E5	PT2A	0	VREF1_0	T
G7	G7	VCC	-		
G9	G9	VCC	-		
H7	H7	VCC	-		
J10	J10	VCC	-		
K10	K10	VCC	-		
K8	K8	VCC	-		
G8	G8	VCCAUX	-		
H10	H10	VCCAUX	-		
J7	J7	VCCAUX	-		
K9	K9	VCCAUX	-		
C5	C5	VCCIO0	0		
E7	E7	VCCIO0	0		
C12	C12	VCCIO1	1		
E10	E10	VCCIO1	1		
E14	E14	VCCIO2	2		
G12	G12	VCCIO2	2		
K12	K12	VCCIO3	3		
M14	M14	VCCIO3	3		
M10	M10	VCCIO4	4		
P12	P12	VCCIO4	4		
M7	M7	VCCIO5	5		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L2	PL24B	7	LDQ24	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
L1	PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T	PL38A	7	LUM0_SPLLT_IN_A/LDQ37	T	
VCCIO	VCCIO7	7			VCCIO7	7			
M2	PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C	
M1	PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T	PL39A	7	LUM0_SPLLT_FB_A/LDQ37	T	
N2	PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
M8	VCCPLL	7			NC	-			
VCCIO	VCCIO7	7			VCCIO7	7			
GND	GNDIO7	-			GNDIO7	-			
N1	PL37A	7	LDQ41		PL50A	7	LDQ54		
L8	PL38A	7	LDQ41	T	PL51A	7	LDQ54	T	
K8	PL38B	7	LDQ41	C	PL51B	7	LDQ54	C	
VCCIO	VCCIO7	7			VCCIO7	7			
L6	PL39A	7	LDQ41	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*	
K5	PL39B	7	LDQ41	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*	
L7	PL40A	7	LDQ41	T	PL53A	7	LDQ54	T	
L5	PL40B	7	LDQ41	C	PL53B	7	LDQ54	C	
GND	GNDIO7	-			GNDIO7	-			
P1	PL41A	7	LDQS41	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*	
P2	PL41B	7	LDQ41	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*	
M6	PL42A	7	LDQ41	T	PL55A	7	LDQ54	T	
VCCIO	VCCIO7	7			VCCIO7	7			
N8	PL42B	7	LDQ41	C	PL55B	7	LDQ54	C	
R1	PL43A	7	LDQ41	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*	
R2	PL43B	7	LDQ41	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*	
M7	PL44A	7	PCLKT7_0/LDQ41	T	PL57A	7	PCLKT7_0/LDQ54	T	
GND	GNDIO7	-			GNDIO7	-			
N9	PL44B	7	PCLKC7_0/LDQ41	C	PL57B	7	PCLKC7_0/LDQ54	C	
M4	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*	
M5	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*	
N7	PL47A	6	VREF2_6/LDQ50	T	PL60A	6	VREF2_6/LDQ63	T	
P9	PL47B	6	VREF1_6/LDQ50	C	PL60B	6	VREF1_6/LDQ63	C	
N3	PL48A	6	LDQ50	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
N4	PL48B	6	LDQ50	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*	
N5	PL49A	6	LDQ50	T	PL62A	6	LDQ63	T	
P7	PL49B	6	LDQ50	C	PL62B	6	LDQ63	C	
T1	PL50A	6	LDQS50	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
T2	PL50B	6	LDQ50	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*	
P8	PL51A	6	LDQ50	T	PL64A	6	LDQ63	T	
P6	PL51B	6	LDQ50	C	PL64B	6	LDQ63	C	
VCCIO	VCCIO6	6			VCCIO6	6			
P5	PL52A	6	LDQ50	T (LVDS)*	PL65A	6	LDQ63	T (LVDS)*	
P4	PL52B	6	LDQ50	C (LVDS)*	PL65B	6	LDQ63	C (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*	
U25	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLL_T_IN_A**/RDQ80	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCCPLL	3			VCCPLL	-			
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C	
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*	
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*	
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C	
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*	
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*	
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C	
GND	GNDIO3	-			GNDIO3	-			
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T	
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*	
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*	
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T	
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*	
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*	
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C	
GND	GNDIO3	-			GNDIO3	-			
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T	
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*	
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*	
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T	
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*	
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C	
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T	
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*	
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C	
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T	
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*	
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*	
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C	
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A2	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*	
B2	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C (LVDS)*	
D3	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T	
C2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C	
E4	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
E5	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C (LVDS)*	
B1	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T	
C1	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C	
D2	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO7	-			
D1	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C (LVDS)*	
E1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T	
F1	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F3	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*	
F2	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C (LVDS)*	
F6	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T	
F5	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C	
GNDIO	GNDIO7	-			GNDIO7	-			
G4	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	
G3	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	
G1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	
G2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	
H1	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
J1	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*	
H2	PL14A	7		T	PL14A	7	LDQ15	T	
H3	PL14B	7		C	PL14B	7	LDQ15	C	
GNDIO	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
G6	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*	
H6	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*	
J2	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T	
GNDIO	GNDIO7	-			GNDIO7	-			
K1	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C	
H4	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*	
H5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*	
J4	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T	
K4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C	
VCCIO	VCCIO6	6			VCCIO6	6			
J6	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
J5	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*	
K3	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T	
K2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C6	PT12B	0		C	PT12B	0		C	
F10	PT12A	0		T	PT12A	0		T	
D7	PT11B	0		C	PT11B	0		C	
H11	PT11A	0		T	PT11A	0		T	
D5	PT10B	0		C	PT10B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E6	PT10A	0		T	PT10A	0		T	
G10	PT9B	0		C	PT9B	0		C	
F9	PT9A	0		T	PT9A	0		T	
H10	PT8B	0		C	PT8B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
E7	PT8A	0		T	PT8A	0		T	
B3	PT7B	0		C	PT7B	0		C	
C5	PT7A	0		T	PT7A	0		T	
B2	PT6B	0		C	PT6B	0		C	
C4	PT6A	0		T	PT6A	0		T	
G9	PT5B	0		C	PT5B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F7	PT5A	0		T	PT5A	0		T	
C3	PT4B	0		C	PT4B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
D4	PT4A	0		T	PT4A	0		T	
J10	PT3B	0		C	PT3B	0		C	
F8	PT3A	0		T	PT3A	0		T	
G8	PT2B	0		C	PT2B	0		C	
G7	PT2A	0		T	PT2A	0		T	
L12	VCC	-			VCC	-			
L13	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L15	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N16	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P16	VCC	-			VCC	-			
R11	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R15	VCC	-			VCC	-			
R16	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T13	VCC	-			VCC	-			
T14	VCC	-			VCC	-			
T15	VCC	-			VCC	-			
B12	VCCIO0	0			VCCIO0	0			
B7	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K13	VCCIO0	0			VCCIO0	0			
D17	VCCIO1	1			VCCIO1	1			
E22	VCCIO1	1			VCCIO1	1			
E25	VCCIO1	1			VCCIO1	1			
F19	VCCIO1	1			VCCIO1	1			
K18	VCCIO1	1			VCCIO1	1			
K19	VCCIO1	1			VCCIO1	1			
F28	VCCIO2	2			VCCIO2	2			
J25	VCCIO2	2			VCCIO2	2			
K28	VCCIO2	2			VCCIO2	2			
M21	VCCIO2	2			VCCIO2	2			
M24	VCCIO2	2			VCCIO2	2			
N21	VCCIO2	2			VCCIO2	2			
N28	VCCIO2	2			VCCIO2	2			
P21	VCCIO2	2			VCCIO2	2			
R25	VCCIO2	2			VCCIO2	2			
AA28	VCCIO3	3			VCCIO3	3			
AB25	VCCIO3	3			VCCIO3	3			
AE28	VCCIO3	3			VCCIO3	3			
T25	VCCIO3	3			VCCIO3	3			
U21	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
V28	VCCIO3	3			VCCIO3	3			
W21	VCCIO3	3			VCCIO3	3			
W24	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
AA19	VCCIO4	4			VCCIO4	4			
AE19	VCCIO4	4			VCCIO4	4			
AF22	VCCIO4	4			VCCIO4	4			
AG17	VCCIO4	4			VCCIO4	4			
AG25	VCCIO4	4			VCCIO4	4			
AA12	VCCIO5	5			VCCIO5	5			
AA13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AF9	VCCIO5	5			VCCIO5	5			
AG14	VCCIO5	5			VCCIO5	5			
AG6	VCCIO5	5			VCCIO5	5			
AA3	VCCIO6	6			VCCIO6	6			
AB6	VCCIO6	6			VCCIO6	6			
AE3	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
U10	VCCIO6	6			VCCIO6	6			
V10	VCCIO6	6			VCCIO6	6			
V3	VCCIO6	6			VCCIO6	6			
W10	VCCIO6	6			VCCIO6	6			
W7	VCCIO6	6			VCCIO6	6			
F3	VCCIO7	7			VCCIO7	7			
J6	VCCIO7	7			VCCIO7	7			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AE27	GND	-		
AE4	GND	-		
AE9	GND	-		
AF14	GND	-		
AF17	GND	-		
AF25	GND	-		
AF6	GND	-		
AJ10	GND	-		
AJ21	GND	-		
AJ27	GND	-		
AJ4	GND	-		
AK1	GND	-		
AK13	GND	-		
AK18	GND	-		
AK24	GND	-		
AK30	GND	-		
AK7	GND	-		
B10	GND	-		
B21	GND	-		
B27	GND	-		
B4	GND	-		
D25	GND	-		
D6	GND	-		
E14	GND	-		
E17	GND	-		
F22	GND	-		
F27	GND	-		
F4	GND	-		
F9	GND	-		
G12	GND	-		
G19	GND	-		
J24	GND	-		
J7	GND	-		
K14	GND	-		
K15	GND	-		
K16	GND	-		
K17	GND	-		
K27	GND	-		
K4	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U22	GND	-			GND	-		
U23	GND	-			GND	-		
V12	GND	-			GND	-		
V13	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V18	GND	-			GND	-		
V19	GND	-			GND	-		
V20	GND	-			GND	-		
V22	GND	-			GND	-		
V23	GND	-			GND	-		
W12	GND	-			GND	-		
W13	GND	-			GND	-		
W15	GND	-			GND	-		
W16	GND	-			GND	-		
W17	GND	-			GND	-		
W18	GND	-			GND	-		
W19	GND	-			GND	-		
W20	GND	-			GND	-		
W22	GND	-			GND	-		
W23	GND	-			GND	-		
W26	GND	-			GND	-		
W31	GND	-			GND	-		
W4	GND	-			GND	-		
W9	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
Y18	GND	-			GND	-		
Y19	GND	-			GND	-		
A11	NC	-			NC	-		
A12	NC	-			NC	-		
A23	NC	-			NC	-		
A24	NC	-			NC	-		
AA11	NC	-			NC	-		
AB11	NC	-			NC	-		
AC26	NC	-			NC	-		
AC30	NC	-			NC	-		
AD11	NC	-			NC	-		
AD12	NC	-			NC	-		
AD13	NC	-			NC	-		
AD14	NC	-			NC	-		
AD15	NC	-			NC	-		
AD19	NC	-			NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD23	NC	-			NC	-		
AE10	NC	-			NC	-		
AE11	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2-35E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2-35E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2-35E-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2-35E-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2-35E-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2-50E-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2-50E-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	COM	50
LFE2-50E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2-50E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2-50E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	70
LFE2-70E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	70
LFE2-70E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	70
LFE2-70E-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2-70E-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2-70E-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	IND	6
LFE2-6E-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	IND	6
LFE2-6E-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	IND	6
LFE2-6E-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	IND	12
LFE2-12E-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	IND	12
LFE2-12E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	12
LFE2-12E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	12
LFE2-12E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	12
LFE2-12E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	12
LFE2-12E-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	IND	12
LFE2-12E-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	IND	12

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table.
		Ordering Information	Updated ordering part number table to include ECP2-12.
			Updated topside mark drawing.
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions.
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
			Updated timing numbers to include LFE2-12E (rev A 0.08).
		Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.
		Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added "Security Series" to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	"Security Series" ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLN Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.
August 2007	02.8	Introduction	1156-fpBGA package option has been removed from the LatticeECP2M family.
		Architecture	Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated.
		DC and Switching	Supply Current (Standby) table has been updated.
			DSP Function timing has been updated.