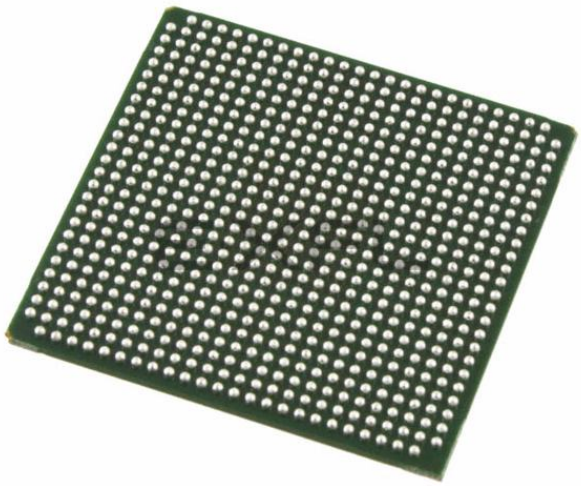
# Lattice Semiconductor Corporation - LFE2-35SE-6FN672I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4000 |
| Number of Logic Elements/Cells | 32000 |
| Total RAM Bits | 339968 |
| Number of I/O | 450 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-6fn672i |

*Figure 2-1. Simplified Block Diagram, ECP2-6 Device (Top Level)*

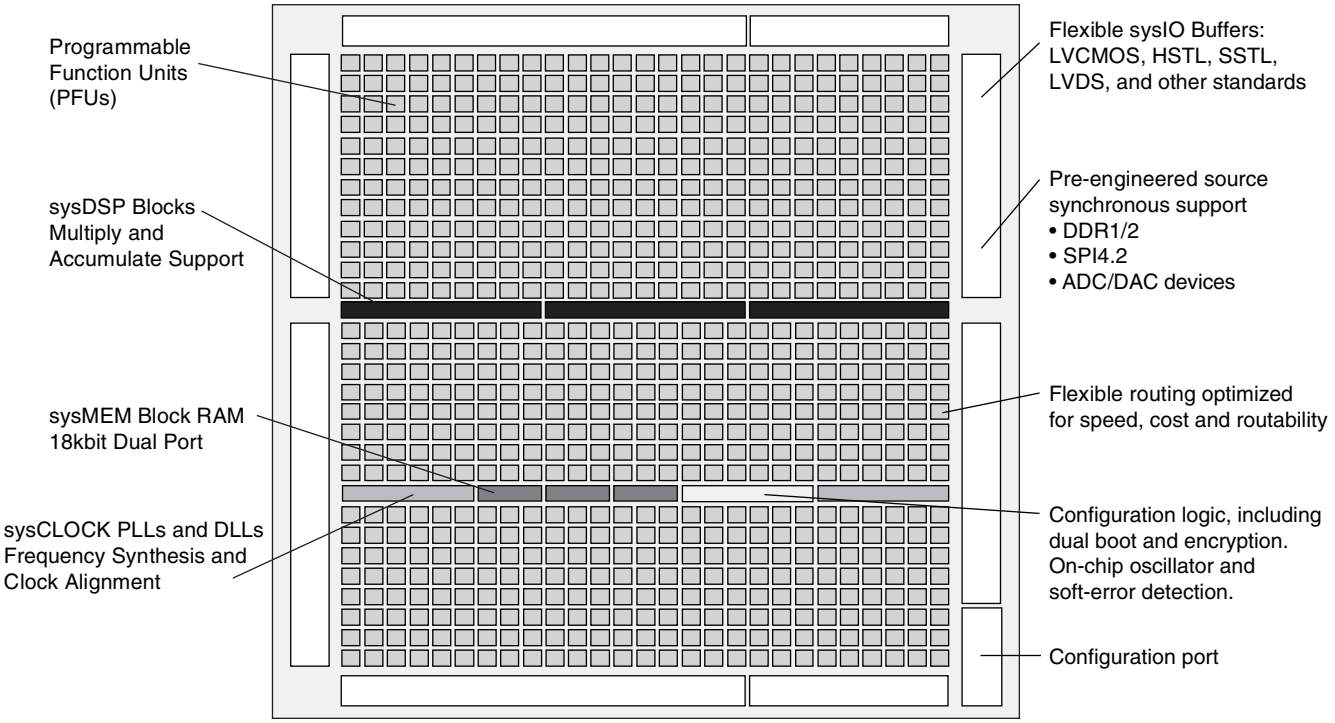



*Figure 2-2. Simplified Block Diagram, ECP2M20 Device (Top Level)*

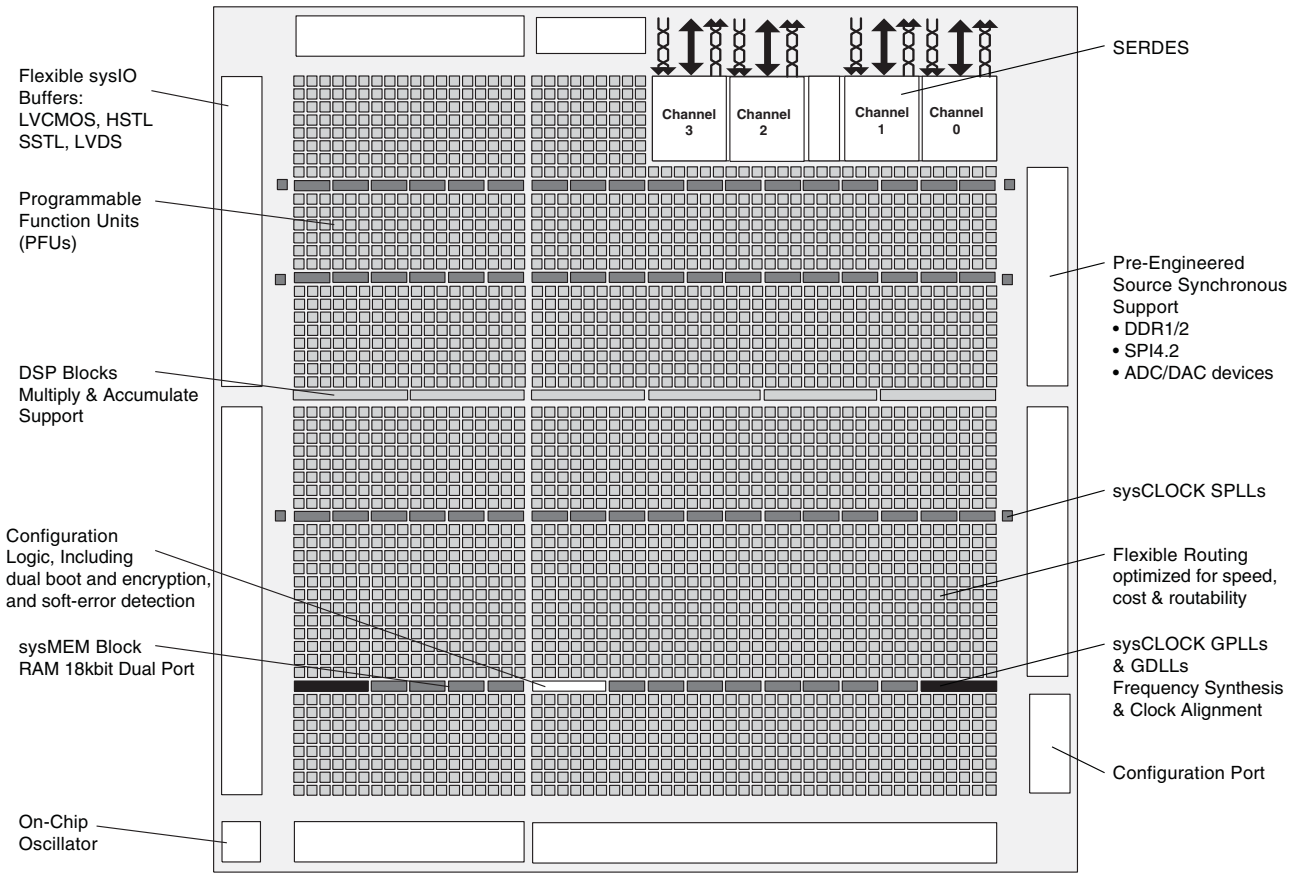
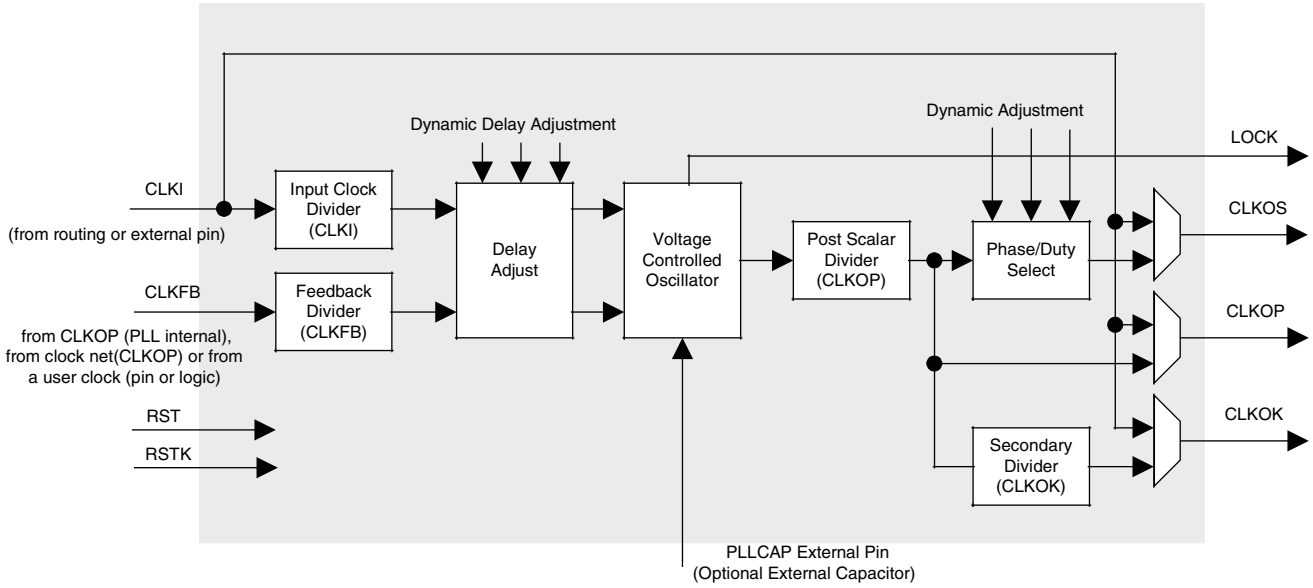


*Figure 2-5. General Purpose PLL (GPLL) Diagram*




## Standard PLL (SPLL)

Some of the larger devices have two to six Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see the list of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

*Table 2-4. GPLL and SPLL Blocks Signal Descriptions*

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | "1" to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | "1" to reset K-divider |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | "1" indicates PLL LOCK to CLKI |
| DDAMODE[1] | I | Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static) |
| DDAIZR[1] | I | Dynamic Delay Zero. "1": delay = 0, "0": delay = on |
| DDAILAG[1] | I | Dynamic Delay Lag/Lead. "1": Lead, "0": Lag |
| DDAIDEL[2:0][1] | I | Dynamic Delay Input |
| DPA MODES | I | DPA (Dynamic Phase Adjust/Duty Cycle Select) mode |
| DPHASE [3:0] | I | DPA Phase Adjust inputs |
| DDDUTY [3:0] | — | DPA Duty Cycle Select inputs |

1. These signals are not available in SPLL.

## MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in the LatticeECP2/M family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-24 shows the MAC sysDSP element.

***Figure 2-24. MAC sysDSP***

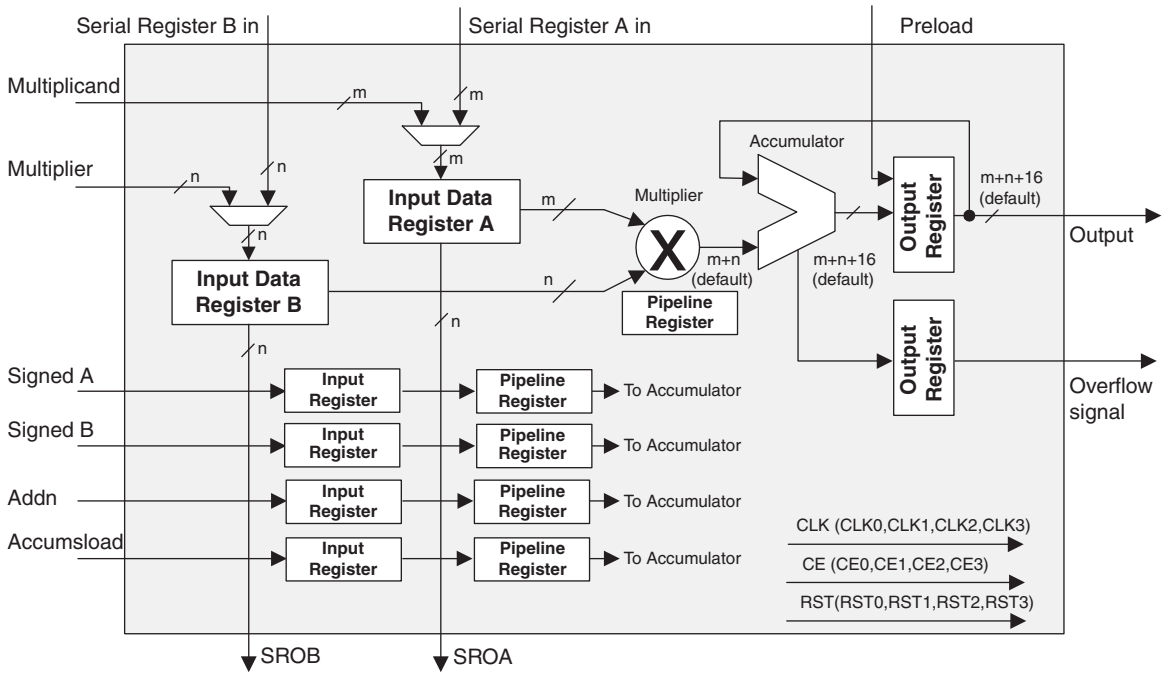
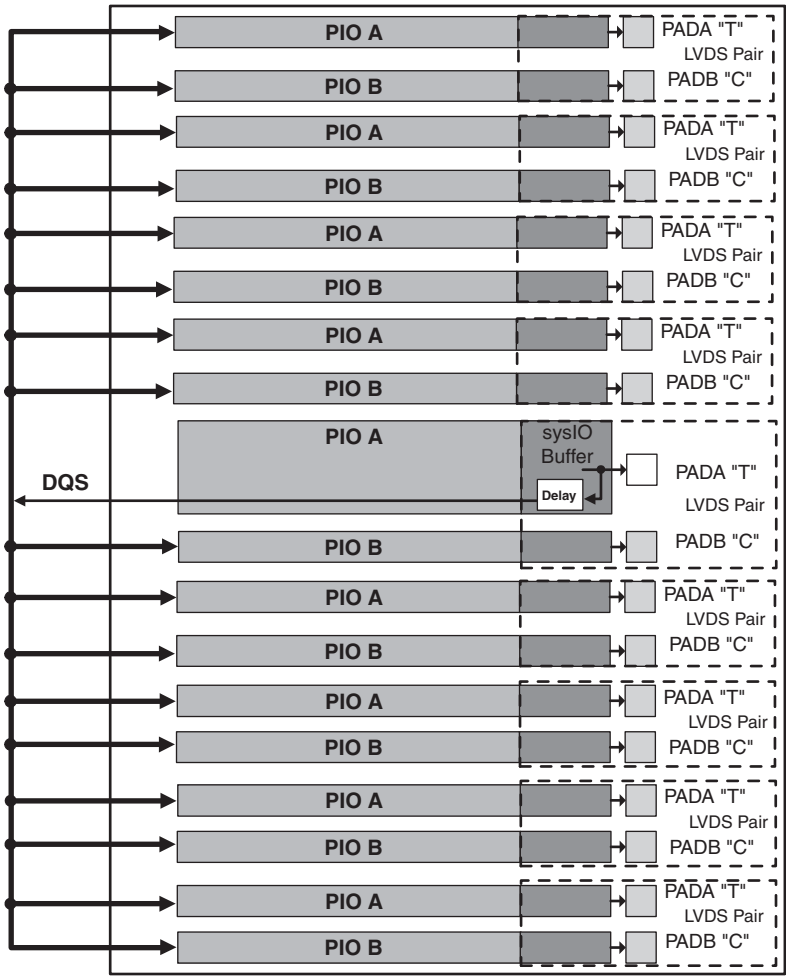


*Figure 2-34. DQS Input Routing for the Bottom Edge of the Device*




## DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-35 and Figure 2-36 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-35. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

## LatticeECP2M Supply Current (Standby)[1, 2, 3, 4]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typ.[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP2M20 | 25 | mA |
| | | ECP2M35 | 50 | mA |
| | | ECP2M50 | 85 | mA |
| | | ECP2M70 | 100 | mA |
| | | ECP2M100 | 100 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP2M20 | 24 | mA |
| | | ECP2M35 | 24 | mA |
| | | ECP2M50 | 24 | mA |
| | | ECP2M70 | 24 | mA |
| | | ECP2M100 | 24 | mA |
| $I_{CCGPLL}$ | GPLL Power Supply Current (per GPLL) | All Devices | 0.5 | mA |
| $I_{CCSPLL}$ | GPLL Power Supply Current (per SPLL) | All Devices | 0.5 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP2M20 | 2 | mA |
| | | ECP2M35 | 2 | mA |
| | | ECP2M50 | 2 | mA |
| | | ECP2M70 | 2 | mA |
| | | ECP2M100 | 2 | mA |
| $I_{CCJ}$ | $V_{CCJ}$ Power Supply Current | All Devices | 3 | mA |

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 25°C, power supplies at normal voltage.

# LatticeECP2/M External Switching Characteristics[9] (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DIBSPI}$ | Data Invalid Before Clock (Transmit) | ECP2-20 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-35 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-50 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2-70 | — | 280 | — | 280 | — | 280 | ps |
| | | ECP2M20 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M35 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M50 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M70 | — | 230 | — | 230 | — | 230 | ps |
| | | ECP2M100 | — | 230 | — | 230 | — | 230 | ps |
| **XGMII I/O Pin Parameters (312 Mbps)[5]** | | | | | | | | | |
| $t_{SUXGMII}$ | Data Setup Before Read Clock | ECP2/M | 480 | — | 480 | — | 480 | — | ps |
| $t_{HXGMII}$ | Data Hold After Read Clock | ECP2/M | 480 | — | 480 | — | 480 | — | ps |
| $t_{DVBCKXGMII}$ | Data Valid Before Clock | ECP2/M | 960 | — | 960 | — | 960 | — | ps |
| $t_{DVACKXGMII}$ | Data Valid After Clock | ECP2/M | 960 | — | 960 | — | 960 | — | ps |
| **Primary** | | | | | | | | | |
| $f_{MAX\_PRI}$[7] | Frequency for Primary Clock Tree | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W\_PRI}$ | Clock Pulse Width for Primary Clock | ECP2/M | 0.95 | — | 1.19 | — | 2.00 | — | ns |
| $t_{SKEW\_PRI}$ | Primary Clock Skew Within a Bank | ECP2/M | — | 300 | — | 360 | — | 420 | ps |
| **Edge Clock** | | | | | | | | | |
| $f_{MAX\_EDGE}$[7] | Frequency for Edge Clock | ECP2/M | — | 420 | — | 357 | — | 311 | MHz |
| $t_{W\_EDGE}$ | Clock Pulse Width for Edge Clock | ECP2/M | 0.95 | — | 1.19 | — | 2.00 | — | ns |
| $t_{SKEW\_EDGE}$ | Edge Clock Skew Within an Edge of the Device | ECP2/M | — | 300 | — | 360 | — | 420 | ps |

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to TN1159, LatticeECP2/M Pin Assignment Recommendations for best performance.

# LatticeECP2/M Internal Switching Characteristics[1]

**Over Recommended Operating Conditions**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **PFU/PFF Logic Mode Timing** | | | | | | | | |
| $t_{LUT4\_PFU}$ | LUT4 delay (A to D inputs to F output) | — | 0.180 | — | 0.198 | — | 0.216 | ns |
| $t_{LUT6\_PFU}$ | LUT6 delay (A to D inputs to OFX output) | — | 0.304 | — | 0.331 | — | 0.358 | ns |
| $t_{LSR\_PFU}$ | Set/Reset to output of PFU (Asynchronous) | — | 0.600 | — | 0.655 | — | 0.711 | ns |
| $t_{SUM\_PFU}$ | Clock to Mux (M0,M1) Input Setup Time | 0.128 | — | 0.129 | — | 0.129 | — | ns |
| $t_{HM\_PFU}$ | Clock to Mux (M0,M1) Input Hold Time | -0.051 | — | -0.049 | — | -0.046 | — | ns |
| $t_{SUD\_PFU}$ | Clock to D input setup time | 0.061 | — | 0.071 | — | 0.081 | — | ns |
| $t_{HD\_PFU}$ | Clock to D input hold time | 0.002 | — | 0.003 | — | 0.003 | — | ns |
| $t_{CK2Q\_PFU}$ | Clock to Q delay, (D-type Register Configuration) | — | 0.285 | — | 0.309 | — | 0.333 | ns |
| **PFU Dual Port Memory Mode Timing** | | | | | | | | |
| $t_{CORAM\_PFU}$ | Clock to Output (F Port) | — | 0.902 | — | 1.083 | — | 1.263 | ns |
| $t_{SUDATA\_PFU}$ | Data Setup Time | -0.172 | — | -0.205 | — | -0.238 | — | ns |
| $t_{HDATA\_PFU}$ | Data Hold Time | 0.199 | — | 0.235 | — | 0.271 | — | ns |
| $t_{SUADDR\_PFU}$ | Address Setup Time | -0.245 | — | -0.284 | — | -0.323 | — | ns |
| $t_{HADDR\_PFU}$ | Address Hold Time | 0.246 | — | 0.285 | — | 0.324 | — | ns |
| $t_{SUWREN\_PFU}$ | Write/Read Enable Setup Time | -0.122 | — | -0.145 | — | -0.168 | — | ns |
| $t_{HWREN\_PFU}$ | Write/Read Enable Hold Time | 0.132 | — | 0.156 | — | 0.180 | — | ns |
| **PIC Timing** | | | | | | | | |
| **PIO Input/Output Buffer Timing** | | | | | | | | |
| $t_{IN\_PIO}$ | Input Buffer Delay (LVCMOS25) | — | 0.613 | — | 0.681 | — | 0.749 | ns |
| $t_{OUT\_PIO}$ | Output Buffer Delay (LVCMOS25) | — | 1.115 | — | 1.115 | — | 1.343 | ns |
| **IOLOGIC Input/Output Timing** | | | | | | | | |
| $t_{SUI\_PIO}$ | Input Register Setup Time (Data Before Clock) | 0.596 | — | 0.645 | — | 0.694 | — | ns |
| $t_{HI\_PIO}$ | Input Register Hold Time (Data after Clock) | -0.570 | — | -0.614 | — | -0.658 | — | ns |
| $t_{COO\_PIO}$ | Output Register Clock to Output Delay | — | 0.61 | — | 0.66 | — | 0.72 | ns |
| $t_{SUCE\_PIO}$ | Input Register Clock Enable Setup Time | 0.032 | — | 0.037 | — | 0.041 | — | ns |
| $t_{HCE\_PIO}$ | Input Register Clock Enable Hold Time | -0.022 | — | -0.025 | — | -0.028 | — | ns |
| $t_{SULSR\_PIO}$ | Set/Reset Setup Time | 0.184 | — | 0.201 | — | 0.217 | — | ns |
| $t_{HLSR\_PIO}$ | Set/Reset Hold Time | -0.080 | — | -0.086 | — | -0.093 | — | ns |
| **EBR Timing** | | | | | | | | |
| $t_{CO\_EBR}$ | Clock (Read) to output from Address or Data | — | 2.51 | — | 2.75 | — | 2.99 | ns |
| $t_{COO\_EBR}$ | Clock (Write) to output from EBR output Register | — | 0.33 | — | 0.36 | — | 0.39 | ns |
| $t_{SUDATA\_EBR}$ | Setup Data to EBR Memory | -0.157 | — | -0.181 | — | -0.205 | — | ns |
| $t_{HDATA\_EBR}$ | Hold Data to EBR Memory | 0.173 | — | 0.195 | — | 0.217 | — | ns |
| $t_{SUADDR\_EBR}$ | Setup Address to EBR Memory | -0.115 | — | -0.130 | — | -0.145 | — | ns |
| $t_{HADDR\_EBR}$ | Hold Address to EBR Memory | 0.138 | — | 0.155 | — | 0.172 | — | ns |
| $t_{SUWREN\_EBR}$ | Setup Write/Read Enable to PFU Memory | -0.128 | — | -0.149 | — | -0.170 | — | ns |

*Table 3-18. Reference Clock*

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{REFCLK}$ | Reference clock frequency | | — | 100 | — | MHz |
| $V_{CM}$ | Input common mode voltage | | — | 0.65 | — | V |
| $T_R/T_F$ | Clock input rise/fall time | | — | — | 1.0 | ns |
| $V_{SW}$ | Differential input voltage swing | | 0.6 | — | 1.6 | V |
| $DC_{REFCLK}$ | Input clock duty cycle | | 40 | 50 | 60 | % |
| PPM | Reference clock tolerance | | -300 | — | +300 | ppm |

## LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

| Pin Type | | LFE2-20 | | | | LFE2-35 | |
|---|---|---|---|---|---|---|---|
| | | 208 PQFP | 256 fpBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank3 | 0 | 0 | 0 | 2 | 0 | 2 |
| | Bank4 | 0 | 2 | 3 | 3 | 3 | 3 |
| | Bank5 | 0 | 1 | 3 | 4 | 3 | 4 |
| | Bank6 | 0 | 1 | 2 | 3 | 1 | 3 |
| | Bank7 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 19 | 32 | 46 | 50 | 46 | 54 |
| | Bank5 | 18 | 17 | 46 | 68 | 46 | 68 |
| | Bank6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E4 | PL2A | 7 | VREF2_7/LDQ6 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| E5 | PL2B | 7 | VREF1_7/LDQ6 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| VCCIO | VCCIO7 | - | | | GNDIO7 | - | | |
| GNDIO | GNDIO7 | - | | | VCCIO | 7 | | |
| E3 | PL10A | 7 | LDQ14 | T (LVDS)* | PL12A | 7 | LDQ16 | T (LVDS)* |
| F3 | PL10B | 7 | LDQ14 | C (LVDS)* | PL12B | 7 | LDQ16 | C (LVDS)* |
| F4 | PL11A | 7 | LDQ14 | T | PL13A | 7 | LDQ16 | T |
| F5 | PL11B | 7 | LDQ14 | C | PL13B | 7 | LDQ16 | C |
| E2 | PL12A | 7 | LDQ14 | T (LVDS)* | PL14A | 7 | LDQ16 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| E1 | PL12B | 7 | LDQ14 | C (LVDS)* | PL14B | 7 | LDQ16 | C (LVDS)* |
| G6 | PL13A | 7 | LDQ14 | T | PL15A | 7 | LDQ16 | T |
| G7 | PL13B | 7 | LDQ14 | C | PL15B | 7 | LDQ16 | C |
| H4 | PL14A | 7 | LDQS14 | T (LVDS)* | PL16A | 7 | LDQS16 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| H5 | PL14B | 7 | LDQ14 | C (LVDS)* | PL16B | 7 | LDQ16 | C (LVDS)* |
| F1 | PL15A | 7 | LDQ14 | T | PL17A | 7 | LDQ16 | T |
| F2 | PL15B | 7 | LDQ14 | C | PL17B | 7 | LDQ16 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| G3 | PL16A | 7 | LDQ14 | T (LVDS)* | PL18A | 7 | LDQ16 | T (LVDS)* |
| G4 | PL16B | 7 | LDQ14 | C (LVDS)* | PL18B | 7 | LDQ16 | C (LVDS)* |
| G1 | PL17A | 7 | LDQ14 | T | PL19A | 7 | LDQ16 | T |
| G2 | PL17B | 7 | LDQ14 | C | PL19B | 7 | LDQ16 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| - | - | - | | | VCCIO | 7 | | |
| H6 | NC | - | | | PL25A | 7 | LUM0_SPLLT_IN_A/LDQ24 | T |
| - | - | - | | | VCCIO | 7 | | |
| J6 | NC | - | | | PL25B | 7 | LUM0_SPLLC_IN_A/LDQ24 | C |
| H3 | NC | - | | | PL26A | 7 | LUM0_SPLLT_FB_A/LDQ24 | T |
| H2 | NC | - | | | PL26B | 7 | LUM0_SPLLC_FB_A/LDQ24 | C |
| - | - | - | | | GNDIO7 | - | | |
| - | - | - | | | VCCIO | 7 | | |
| H1 | PL18A | 7 | LDQ22 | | PL37A | 7 | LDQ41 | |
| J4 | PL19A | 7 | LDQ22 | T | PL38A | 7 | LDQ41 | T |
| J5 | PL19B | 7 | LDQ22 | C | PL38B | 7 | LDQ41 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |
| J2 | PL20A | 7 | LDQ22 | T (LVDS)* | PL39A | 7 | LDQ41 | T (LVDS)* |
| J1 | PL20B | 7 | LDQ22 | C (LVDS)* | PL39B | 7 | LDQ41 | C (LVDS)* |
| L6 | PL21A | 7 | LDQ22 | T | PL40A | 7 | LDQ41 | T |
| L5 | PL21B | 7 | LDQ22 | C | PL40B | 7 | LDQ41 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| K3 | PL22A | 7 | LDQS22 | T (LVDS)* | PL41A | 7 | LDQS41 | T (LVDS)* |
| K4 | PL22B | 7 | LDQ22 | C (LVDS)* | PL41B | 7 | LDQ41 | C (LVDS)* |
| K2 | PL23A | 7 | LDQ22 | T | PL42A | 7 | LDQ41 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO | 7 | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| L23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| AA23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T23 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| V20 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AC16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| Y18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC6 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y9 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T4 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| F4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L4 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AE25 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| V18 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J10 | VCCAUX | - | | | VCCAUX | - | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| J17 | VCCAUX | - | | | VCCAUX | - | | |
| K18 | VCCAUX | - | | | VCCAUX | - | | |
| K9 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| T18 | VCCAUX | - | | | VCCAUX | - | | |
| T9 | VCCAUX | - | | | VCCAUX | - | | |
| U18 | VCCAUX | - | | | VCCAUX | - | | |
| U9 | VCCAUX | - | | | VCCAUX | - | | |
| V10 | VCCAUX | - | | | VCCAUX | - | | |
| V11 | VCCAUX | - | | | VCCAUX | - | | |
| V16 | VCCAUX | - | | | VCCAUX | - | | |
| V17 | VCCAUX | - | | | VCCAUX | - | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AH24 | PB89A | 4 | BDQ87 | T |
| AH25 | PB89B | 4 | BDQ87 | C |
| VCCIO | VCCIO4 | 4 | | |
| AJ26 | PB90A | 4 | BDQ87 | T |
| AK26 | PB90B | 4 | BDQ87 | C |
| AF25 | PB91A | 4 | BDQ87 | T |
| AG25 | PB91B | 4 | BDQ87 | C |
| GND | GNDIO4 | - | | |
| AK22 | PB92A | 4 | BDQ96 | T |
| AJ22 | PB92B | 4 | BDQ96 | C |
| AE22 | PB93A | 4 | BDQ96 | T |
| AF22 | PB93B | 4 | BDQ96 | C |
| AG22 | PB94A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AH22 | PB94B | 4 | BDQ96 | C |
| AG24 | PB95A | 4 | BDQ96 | T |
| AG23 | PB95B | 4 | BDQ96 | C |
| AE23 | PB96A | 4 | BDQS96 | |
| GND | GNDIO4 | - | | |
| AC22 | PB97A | 4 | BDQ96 | |
| AJ23 | PB98A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK23 | PB98B | 4 | BDQ96 | C |
| AD24 | PB99A | 4 | BDQ96 | T |
| AF24 | PB99B | 4 | BDQ96 | C |
| AC23 | PB100A | 4 | VREF2_4/BDQ96 | T |
| GND | GNDIO4 | - | | |
| AE24 | PB100B | 4 | VREF1_4/BDQ96 | C |
| AE25 | CFG2 | 8 | | |
| AB22 | CFG1 | 8 | | |
| AE26 | CFG0 | 8 | | |
| AA22 | PROGRAMN | 8 | | |
| AD25 | CCLK | 8 | | |
| AD26 | INITN | 8 | | |
| AC24 | DONE | 8 | | |
| GND | GNDIO4 | - | | |
| AC25 | PR90B | 8 | WRITEN | C |
| AE27 | PR90A | 8 | CS1N | T |
| AC26 | PR89B | 8 | CSN | C |
| AE28 | PR89A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | |
| AD27 | PR88B | 8 | D1 | C |
| AD28 | PR88A | 8 | D2 | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| V23 | PR70A | 3 | RDQ71 | T |
| W27 | PR69B | 3 | RDQ71 | C (LVDS)* |
| W28 | PR69A | 3 | RDQ71 | T (LVDS)* |
| V26 | PR68B | 3 | RDQ71 | C |
| VCCIO | VCCIO3 | 3 | | |
| V24 | PR68A | 3 | RDQ71 | T |
| W29 | PR67B | 3 | RDQ71 | C (LVDS)* |
| W30 | PR67A | 3 | RDQ71 | T (LVDS)* |
| U25 | PR66B | 3 | RDQ63 | C |
| GND | GNDIO3 | - | | |
| U23 | PR66A | 3 | RDQ63 | T |
| V29 | PR65B | 3 | RDQ63 | C (LVDS)* |
| V30 | PR65A | 3 | RDQ63 | T (LVDS)* |
| U26 | PR64B | 3 | RDQ63 | C |
| VCCIO | VCCIO3 | 3 | | |
| U24 | PR64A | 3 | RDQ63 | T |
| U27 | PR63B | 3 | RDQ63 | C (LVDS)* |
| U28 | PR63A | 3 | RDQS63 | T (LVDS)* |
| GND | GNDIO3 | - | | |
| T23 | PR62B | 3 | RDQ63 | C |
| T25 | PR62A | 3 | RDQ63 | T |
| U29 | PR61B | 3 | RDQ63 | C (LVDS)* |
| U30 | PR61A | 3 | RDQ63 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| T24 | PR60B | 3 | VREF2_3/RDQ63 | C |
| T26 | PR60A | 3 | VREF1_3/RDQ63 | T |
| T27 | PR59B | 3 | PCLKC3_0/RDQ63 | C (LVDS)* |
| T28 | PR59A | 3 | PCLKT3_0/RDQ63 | T (LVDS)* |
| R24 | PR57B | 2 | PCLKC2_0/RDQ54 | C |
| R26 | PR57A | 2 | PCLKT2_0/RDQ54 | T |
| GND | GNDIO2 | - | | |
| T29 | PR56B | 2 | RDQ54 | C (LVDS)* |
| T30 | PR56A | 2 | RDQ54 | T (LVDS)* |
| R23 | PR55B | 2 | RDQ54 | C |
| R25 | PR55A | 2 | RDQ54 | T |
| VCCIO | VCCIO2 | 2 | | |
| R27 | PR54B | 2 | RDQ54 | C (LVDS)* |
| R28 | PR54A | 2 | RDQS54 | T (LVDS)* |
| P26 | PR53B | 2 | RDQ54 | C |
| GND | GNDIO2 | - | | |
| P24 | PR53A | 2 | RDQ54 | T |
| R29 | PR52B | 2 | RDQ54 | C (LVDS)* |
| R30 | PR52A | 2 | RDQ54 | T (LVDS)* |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U9 | PL67B | 6 | LDQ66 | C | PL72B | 6 | LDQ71 | C |
| AA5 | PL68A | 6 | LDQ66 | T (LVDS)* | PL73A | 6 | LDQ71 | T* |
| AA6 | PL68B | 6 | LDQ66 | C (LVDS)* | PL73B | 6 | LDQ71 | C* |
| Y7 | PL69A | 6 | LDQ66 | T | PL74A | 6 | LDQ71 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| V9 | PL69B | 6 | LDQ66 | C | PL74B | 6 | LDQ71 | C |
| AC3 | TCK | - | | | TCK | - | | |
| W8 | TDI | - | | | TDI | - | | |
| AC4 | TMS | - | | | TMS | - | | |
| V8 | TDO | - | | | TDO | - | | |
| AA7 | VCCJ | - | | | VCCJ | - | | |
| AB6 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| Y8 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| AD1 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| AD2 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AC5 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| AA8 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC6 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| W9 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| AB7 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y9 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| AD3 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| AD4 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| AA9 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| W10 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC7 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| Y10 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AE2 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| AD5 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AE4 | PB11A | 5 | BDQ15 | T | PB11A | 5 | BDQ15 | T |
| AE3 | PB11B | 5 | BDQ15 | C | PB11B | 5 | BDQ15 | C |
| W11 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| AB8 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| AE5 | PB13A | 5 | BDQ15 | T | PB13A | 5 | BDQ15 | T |
| AD6 | PB13B | 5 | BDQ15 | C | PB13B | 5 | BDQ15 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA10 | PB14A | 5 | BDQ15 | T | PB14A | 5 | BDQ15 | T |
| AC8 | PB14B | 5 | BDQ15 | C | PB14B | 5 | BDQ15 | C |
| W12 | PB15A | 5 | BDQS15 | T | PB15A | 5 | BDQS15 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AC9 | PB15B | 5 | BDQ15 | C | PB15B | 5 | BDQ15 | C |
| W13 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| AB10 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| AF3 | PB17A | 5 | BDQ15 | T | PB17A | 5 | BDQ15 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AH12 | VCC | - | | | LLC_SQ_VCCRX1 | 14 | | |
| AK8 | PB16A | 5 | BDQ15 | T | LLC_SQ_HDOUTP1 | 14 | | T |
| AH8 | NC | - | | | LLC_SQ_VCCOB1 | 14 | | |
| AJ8 | PB16B | 5 | BDQ15 | C | LLC_SQ_HDOUTN1 | 14 | | C |
| AH9 | VCC | - | | | LLC_SQ_VCCTX1 | 14 | | |
| AJ9 | PB17B | 5 | BDQ15 | C | LLC_SQ_HDOUTN0 | 14 | | C |
| AK10 | NC | - | | | LLC_SQ_VCCOB0 | 14 | | |
| AK9 | PB17A | 5 | BDQ15 | T | LLC_SQ_HDOUTP0 | 14 | | T |
| AH10 | VCC | - | | | LLC_SQ_VCCTX0 | 14 | | |
| AJ12 | PB19B | 5 | BDQ15 | C | LLC_SQ_HDINN0 | 14 | | C |
| AJ13 | NC | - | | | LLC_SQ_VCCIB0 | 14 | | |
| AK12 | PB19A | 5 | BDQ15 | T | LLC_SQ_HDINP0 | 14 | | T |
| AH13 | VCC | - | | | LLC_SQ_VCCRX0 | 14 | | |
| AF10 | PB3A | 5 | BDQ6 | T | PB30A | 5 | BDQ33 | T |
| AE8 | PB3B | 5 | BDQ6 | C | PB30B | 5 | BDQ33 | C |
| AE11 | PB4A | 5 | BDQ6 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AD9 | PB4B | 5 | BDQ6 | C | PB31B | 5 | BDQ33 | C |
| AE10 | PB5A | 5 | BDQ6 | T | PB32A | 5 | BDQ33 | T |
| AD10 | PB5B | 5 | BDQ6 | C | PB32B | 5 | BDQ33 | C |
| AE13 | PB6A | 5 | BDQS6 | T | PB33A | 5 | BDQS33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AC12 | PB6B | 5 | BDQ6 | C | PB33B | 5 | BDQ33 | C |
| AG2 | PB7A | 5 | BDQ6 | T | PB34A | 5 | BDQ33 | T |
| AG3 | PB7B | 5 | BDQ6 | C | PB34B | 5 | BDQ33 | C |
| AD13 | PB8A | 5 | BDQ6 | T | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC13 | PB8B | 5 | BDQ6 | C | PB35B | 5 | BDQ33 | C |
| AE14 | PB9A | 5 | BDQ6 | T | PB36A | 5 | BDQ33 | T |
| AC14 | PB9B | 5 | BDQ6 | C | PB36B | 5 | BDQ33 | C |
| AF3 | PB10A | 5 | BDQ6 | T | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AF4 | PB10B | 5 | BDQ6 | C | PB37B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | - | - | | |
| AG4 | PB20A | 5 | BDQ24 | T | PB38A | 5 | BDQ42 | T |
| AG5 | PB20B | 5 | BDQ24 | C | PB38B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | | - | - | | |
| VCCIO | VCCIO5 | 5 | | | - | - | | |
| AD11 | PB24A | 5 | BDQS24**** | T | PB39A | 5 | BDQ42 | T |
| AF13 | PB24B | 5 | BDQ24 | C | PB39B | 5 | BDQ42 | C |
| AF12 | PB25A | 5 | BDQ24 | T | PB40A | 5 | BDQ42 | T |
| - | - | - | | | VCCIO5 | 5 | | |
| AD14 | PB25B | 5 | BDQ24 | C | PB40B | 5 | BDQ42 | C |
| AG8 | PB26A | 5 | BDQ24 | T | PB41A | 5 | BDQ42 | T |
| AF8 | PB26B | 5 | BDQ24 | C | PB41B | 5 | BDQ42 | C |
| AE15 | PB27A | 5 | BDQ24 | T | PB42A | 5 | BDQS42**** | T |
| - | - | - | | | GNDIO5 | - | | |
| VCCIO | VCCIO5 | 5 | | | - | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AF11 | PB62B | 5 | PCLKC5_0/BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AJ14 | PB67A | 4 | PCLKT4_0/BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK14 | PB67B | 4 | PCLKC4_0/BDQ69 | C |
| AK15 | PB68A | 4 | VREF2_4/BDQ69 | T |
| AK16 | PB68B | 4 | VREF1_4/BDQ69 | C |
| AF18 | PB69A | 4 | BDQS69 | T |
| GNDIO | GNDIO4 | - | | |
| AD16 | PB69B | 4 | BDQ69 | C |
| AJ15 | PB70A | 4 | BDQ69 | T |
| AG16 | PB70B | 4 | BDQ69 | C |
| AE17 | PB71A | 4 | BDQ69 | T |
| VCCIO | VCCIO4 | 4 | | |
| AC17 | PB71B | 4 | BDQ69 | C |
| AH16 | PB72A | 4 | BDQ69 | T |
| AK17 | PB72B | 4 | BDQ69 | C |
| AG20 | PB73A | 4 | BDQ69 | T |
| GNDIO | GNDIO4 | - | | |
| AG21 | PB73B | 4 | BDQ69 | C |
| AG18 | PB74A | 4 | BDQ78 | T |
| AJ16 | PB74B | 4 | BDQ78 | C |
| AF21 | PB75A | 4 | BDQ78 | T |
| AG22 | PB75B | 4 | BDQ78 | C |
| AD17 | PB76A | 4 | BDQ78 | T |
| AF19 | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | |
| AH17 | PB80A | 4 | BDQ78 | T |
| AJ17 | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | |
| AF26 | PB82A | 4 | BDQ78 | T |
| AE25 | PB82B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | |
| AD24 | PB92A | 4 | BDQ96 | T |
| AE24 | PB92B | 4 | BDQ96 | C |
| AD18 | PB93A | 4 | BDQ96 | T |
| AC18 | PB93B | 4 | BDQ96 | C |
| AE18 | PB94A | 4 | BDQ96 | T |
| AG19 | PB94B | 4 | BDQ96 | C |
| VCCIO | VCCIO4 | 4 | | |
| GNDIO | GNDIO4 | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| D19 | PT93B | 1 | | C |
| E18 | PT93A | 1 | | T |
| D18 | PT92B | 1 | | C |
| C17 | PT92A | 1 | | T |
| A17 | PT91B | 1 | | C |
| B17 | PT91A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| J18 | PT75B | 1 | | C |
| J19 | PT75A | 1 | | T |
| H17 | PT74B | 1 | | C |
| J17 | PT74A | 1 | | T |
| F18 | PT73B | 1 | | C |
| F17 | PT73A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| A16 | PT72B | 1 | | C |
| B16 | PT72A | 1 | | T |
| G17 | PT71B | 1 | | C |
| G16 | PT71A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| H16 | PT70B | 1 | | C |
| F16 | PT70A | 1 | | T |
| J16 | PT69B | 1 | | C |
| G15 | PT69A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| C16 | PT68B | 1 | | C |
| D16 | PT68A | 1 | | T |
| J15 | PT67B | 1 | | C |
| H15 | PT67A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| A15 | PT66B | 1 | VREF2_1 | C |
| B15 | PT66A | 1 | VREF1_1 | T |
| F15 | PT65B | 1 | PCLKC1_0 | C |
| E16 | PT65A | 1 | PCLKT1_0 | T |
| C15 | PT64B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | |
| D15 | PT64A | 0 | PCLKT0_0 | T |
| C14 | PT63B | 0 | VREF2_0 | C |
| E15 | PT63A | 0 | VREF1_0 | T |
| G14 | PT62B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| J14 | PT62A | 0 | | T |
| F14 | PT61B | 0 | | C |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AF27 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| AF28 | PR85B | 3 | RLM0_GDLLC_FB_A | C | PR102B | 3 | RLM0_GDLLC_FB_A/RDQ99 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AD26 | PR85A | 3 | RLM0_GDLLT_FB_A | T | PR102A | 3 | RLM0_GDLLT_FB_A/RDQ99 | T |
| AJ32 | PR84B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR101B | 3 | RLM0_GDLLC_IN_A**/ RDQ99 | C (LVDS)* |
| AJ33 | PR84A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR101A | 3 | RLM0_GDLLT_IN_A**/ RDQ99 | T (LVDS)* |
| AJ34 | PR83B | 3 | RLM0_GPLLC_IN_A** | C | PR100B | 3 | RLM0_GPLLC_IN_A**/ RDQ99 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AK34 | PR83A | 3 | RLM0_GPLLT_IN_A** | T | PR100A | 3 | RLM0_GPLLT_IN_A**/ RDQ99 | T |
| AH33 | PR82B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR99B | 3 | RLM0_GPLLC_FB_A/RDQ99 | C (LVDS)* |
| AH34 | PR82A | 3 | RLM0_GPLLT_FB_A/RDQS82**** | T (LVDS)* | PR99A | 3 | RLM0_GPLLT_FB_A/ RDQS99 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AF29 | PR81B | 3 | RDQ82 | C | PR98B | 3 | RDQ99 | C |
| AF31 | PR81A | 3 | RDQ82 | T | PR98A | 3 | RDQ99 | T |
| AG33 | PR80B | 3 | RDQ82 | C (LVDS)* | PR97B | 3 | RDQ99 | C (LVDS)* |
| AG34 | PR80A | 3 | RDQ82 | T (LVDS)* | PR97A | 3 | RDQ99 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AF30 | PR79B | 3 | RDQ82 | C | PR96B | 3 | RDQ99 | C |
| AF32 | PR79A | 3 | RDQ82 | T | PR96A | 3 | RDQ99 | T |
| AE29 | PR78B | 3 | RDQ82 | C (LVDS)* | PR95B | 3 | RDQ99 | C (LVDS)* |
| AE30 | PR78A | 3 | RDQ82 | T (LVDS)* | PR95A | 3 | RDQ99 | T (LVDS)* |
| AF33 | NC | - | | | PR93B | 3 | RDQ90 | C |
| AF34 | NC | - | | | PR93A | 3 | RDQ90 | T |
| - | - | - | | | GNDIO3 | - | | |
| AC27 | NC | - | | | PR92B | 3 | RDQ90 | C (LVDS)* |
| AC28 | NC | - | | | PR92A | 3 | RDQ90 | T (LVDS)* |
| AD29 | NC | - | | | PR91B | 3 | RDQ90 | C |
| AD30 | NC | - | | | PR91A | 3 | RDQ90 | T |
| - | - | - | | | VCCIO3 | 3 | | |
| AE33 | NC | - | | | PR90B | 3 | RDQ90 | C (LVDS)* |
| AE34 | NC | - | | | PR90A | 3 | RDQS90 | T (LVDS)* |
| AD32 | NC | - | | | PR89B | 3 | RDQ90 | C |
| - | - | - | | | GNDIO3 | - | | |
| AD31 | NC | - | | | PR89A | 3 | RDQ90 | T |
| AB25 | NC | - | | | PR88B | 3 | RDQ90 | C (LVDS)* |
| AC25 | NC | - | | | PR88A | 3 | RDQ90 | T (LVDS)* |
| AB28 | NC | - | | | PR87B | 3 | RDQ90 | C |
| - | - | - | | | VCCIO3 | 3 | | |
| AA26 | NC | - | | | PR87A | 3 | RDQ90 | T |
| AD33 | NC | - | | | PR86B | 3 | RDQ90 | C (LVDS)* |
| AD34 | NC | - | | | PR86A | 3 | RDQ90 | T (LVDS)* |
| AC29 | PR76B | 3 | RDQ73 | C | PR84B | 3 | RDQ81 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AA27 | PR76A | 3 | RDQ73 | T | PR84A | 3 | RDQ81 | T |
| AC32 | PR75B | 3 | RDQ73 | C (LVDS)* | PR83B | 3 | RDQ81 | C (LVDS)* |
| AC31 | PR75A | 3 | RDQ73 | T (LVDS)* | PR83A | 3 | RDQ81 | T (LVDS)* |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | IND | 20 |
| LFE2-20E-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | IND | 20 |
| LFE2-20E-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | IND | 20 |
| LFE2-20E-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | IND | 20 |
| LFE2-20E-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | IND | 20 |
| LFE2-20E-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | IND | 20 |
| LFE2-20E-5F672I | 402 | 1.2V | -5 | fpBGA | 672 | IND | 20 |
| LFE2-20E-6F672I | 402 | 1.2V | -6 | fpBGA | 672 | IND | 20 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5F484I | 331 | 1.2V | -5 | fpBGA | 484 | IND | 35 |
| LFE2-35E-6F484I | 331 | 1.2V | -6 | fpBGA | 484 | IND | 35 |
| LFE2-35E-5F672I | 450 | 1.2V | -5 | fpBGA | 672 | IND | 35 |
| LFE2-35E-6F672I | 450 | 1.2V | -6 | fpBGA | 672 | IND | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5F484I | 339 | 1.2V | -5 | fpBGA | 484 | IND | 50 |
| LFE2-50E-6F484I | 339 | 1.2V | -6 | fpBGA | 484 | IND | 50 |
| LFE2-50E-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | IND | 50 |
| LFE2-50E-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | IND | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5F672I | 500 | 1.2V | -5 | fpBGA | 672 | IND | 70 |
| LFE2-70E-6F672I | 500 | 1.2V | -6 | fpBGA | 672 | IND | 70 |
| LFE2-70E-5F900I | 583 | 1.2V | -5 | fpBGA | 900 | IND | 70 |
| LFE2-70E-6F900I | 583 | 1.2V | -6 | fpBGA | 900 | IND | 70 |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| June 2013 (cont.) | 04.0 (cont.) | DC and Switching Characteristics | sysCLOCK SPLL Timing table – Corrected signal names for $t_{RST}$ parameter. |
| | | | LatticeECP2/M sysCONFIG Port Timing Specifications table – added $t_{SUMCDI}$ and $t_{HMCDI}$ parameters. |
| September 2013 | 04.1 | Architecture | Updated Selectable Master Clock (CCLK) Frequencies during Configuration table. |
| | | DC and Switching Characteristics | Added information on $f_{MAXSPI}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |