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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	4000
Number of Logic Elements/Cells	32000
Total RAM Bits	339968
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-35se-7f672c

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP} V_{INM}$	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	μ A
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM})$, $R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, $R_T = 100$ Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.40	—	1.70	—	1.90	—	ns
		LFE2M70	1.40	—	1.70	—	1.90	—	ns
		LFE2M100	1.40	—	1.70	—	1.90	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IO}	Clock Frequency of I/O Register and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)¹									
t _{COE}	Clock to Output - PIO Output Register	LFE2-6	—	2.60	—	2.90	—	3.20	ns
		LFE2-12	—	2.60	—	2.90	—	3.20	ns
		LFE2-20	—	2.60	—	2.90	—	3.20	ns
		LFE2-35	—	2.60	—	2.90	—	3.20	ns
		LFE2-50	—	2.60	—	2.90	—	3.20	ns
		LFE2-70	—	2.60	—	2.90	—	3.20	ns
		LFE2M20	—	2.60	—	2.90	—	3.20	ns
		LFE2M35	—	2.60	—	2.90	—	3.20	ns
		LFE2M50	—	3.10	—	3.40	—	3.70	ns
		LFE2M70	—	3.10	—	3.40	—	3.70	ns
		LFE2M100	—	3.10	—	3.40	—	3.70	ns

LatticeECP2/M Internal Switching Characteristics¹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t _{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t _{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t _{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t _{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t _{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t _{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t _{RSTREC_SPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing^{2,3}								
t _{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t _{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t _{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t _{HP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t _{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t _{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t _{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t _{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t _{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
t _{SUADDSUB}	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
t _{HADDSUB}	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

SERDES High Speed Data Receiver (LatticeECP2M Family Only)

Table 3-11. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units
RX-CID _S	Stream of nontransitions ¹ (CID = Consecutive Identical Digits) @ 10 ⁻¹² BER		7 @ 3.125 Gbps 20 @ 1.25 Gbps		Bits
V _{RX-DIFF-S}	Differential input sensitivity	100	—	—	mV, p-p
V _{RX-IN}	Input levels	0	—	V _{CCR_X} + 0.8	V
V _{RX-CM-DC}	Input common mode range (DC coupled)	0.5	—	1.2	V
V _{RX-CM-AC}	Input common mode range (AC coupled) ³	0	—	1.5	V
T _{RX-RELOCK}	CDR re-lock time ²	—	—	3000	Bits
Z _{RX-TERM}	Input termination 50/75 Ohm/High Z	—	50		Ohms
RL _{RX-RL}	Return loss (without package)	—	9	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.

2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.

3. AC coupling is used to interface to LVPECL and LVDS.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-12. Receiver Total Jitter Tolerance Specification¹

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.54	UI, p-p
Random		600 mV differential eye	—	—	0.26	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.61	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.81	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.53	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	250 Mbps ²	600 mV differential eye	—	—	0.42	UI, p-p
Random		600 mV differential eye	—	—	0.10	UI, p-p
Total		600 mV differential eye	—	—	0.60	UI, p-p

1. Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

2. Jitter specification is limited by measurement equipment capability.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
-	-	-			-	-			
D3	PL5A	7		T	PL5A	7		T	
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
D2	PL5B	7		C	PL5B	7		C	
GND	GNDIO7	-			GNDIO7	-			
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T	
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C	
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C	
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*	
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T	
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
GND	GNDIO6	-			GNDIO6	-			
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	
G10	VCC	-			VCC	-			
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T	
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
R8	VCCIO6	6			VCCIO6	6			
J8	VCCIO7	7			VCCIO7	7			
K7	VCCIO7	7			VCCIO7	7			
L7	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
P15	VCCIO8	8			VCCIO8	8			
R15	VCCIO8	8			VCCIO8	8			
C5	VCCAUX	-			VCCAUX	-			
D11	VCCAUX	-			VCCAUX	-			
E17	VCCAUX	-			VCCAUX	-			
E6	VCCAUX	-			VCCAUX	-			
F13	VCCAUX	-			VCCAUX	-			
G18	VCCAUX	-			VCCAUX	-			
G5	VCCAUX	-			VCCAUX	-			
K5	VCCAUX	-			VCCAUX	-			
M17	VCCAUX	-			VCCAUX	-			
P17	VCCAUX	-			VCCAUX	-			
R5	VCCAUX	-			VCCAUX	-			
V11	VCCAUX	-			VCCAUX	-			
V13	VCCAUX	-			VCCAUX	-			
V15	VCCAUX	-			VCCAUX	-			
V7	VCCAUX	-			VCCAUX	-			
V8	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A22	GND	-			GND	-			
AA19	GND	-			GND	-			
AA4	GND	-			GND	-			
AB1	GND	-			GND	-			
AB22	GND	-			GND	-			
B19	GND	-			GND	-			
B4	GND	-			GND	-			
C14	GND	-			GND	-			
C9	GND	-			GND	-			
D2	GND	-			GND	-			
D21	GND	-			GND	-			
F17	GND	-			GND	-			
F6	GND	-			GND	-			
H10	GND	-			GND	-			
H11	GND	-			GND	-			
H12	GND	-			GND	-			
H13	GND	-			GND	-			
J14	GND	-			GND	-			
J20	GND	-			GND	-			
J3	GND	-			GND	-			

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D4	PT7B	0		C	PT7B	0		C
D3	PT7A	0		T	PT7A	0		T
C2	PT6B	0		C	PT6B	0		C
C1	PT6A	0		T	PT6A	0		T
G8	PT5B	0		C	PT5B	0		C
GND	GNDIO0	-			GNDIO0	-		
G7	PT5A	0		T	PT5A	0		T
E7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT4A	0		T	PT4A	0		T
E6	PT3B	0		C	PT3B	0		C
E5	PT3A	0		T	PT3A	0		T
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
D11	VCCIO0	0			VCCIO0	0		
D6	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		
J12	VCCIO0	0			VCCIO0	0		
D16	VCCIO1	1			VCCIO1	1		
D21	VCCIO1	1			VCCIO1	1		
G18	VCCIO1	1			VCCIO1	1		
J15	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
F23	VCCIO2	2			VCCIO2	2		
J20	VCCIO2	2			VCCIO2	2		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
F6	PL5A	7	LDQ8	T	PL18A	7	LDQ21	T	
F5	PL5B	7	LDQ8	C	PL18B	7	LDQ21	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E4	PL6A	7	LDQ8	T (LVDS)*	PL19A	7	LDQ21	T (LVDS)*	
E3	PL6B	7	LDQ8	C (LVDS)*	PL19B	7	LDQ21	C (LVDS)*	
E2	PL7A	7	LDQ8	T	PL20A	7	LDQ21	T	
E1	PL7B	7	LDQ8	C	PL20B	7	LDQ21	C	
GND	GNDIO7	-			GNDIO7	-			
H6	PL8A	7	LDQS8	T (LVDS)*	PL21A	7	LDQS21	T (LVDS)*	
H5	PL8B	7	LDQ8	C (LVDS)*	PL21B	7	LDQ21	C (LVDS)*	
F2	PL9A	7	LDQ8	T	PL22A	7	LDQ21	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F1	PL9B	7	LDQ8	C	PL22B	7	LDQ21	C	
H8	PL10A	7	LDQ8	T (LVDS)*	PL23A	7	LDQ21	T (LVDS)*	
J9	PL10B	7	LDQ8	C (LVDS)*	PL23B	7	LDQ21	C (LVDS)*	
G4	PL11A	7	LDQ8	T	PL24A	7	LDQ21	T	
GND	GNDIO7	-			GNDIO7	-			
G3	PL11B	7	LDQ8	C	PL24B	7	LDQ21	C	
H7	PL12A	7	LDQ16	T (LVDS)*	PL25A	7	LDQ29	T (LVDS)*	
J8	PL12B	7	LDQ16	C (LVDS)*	PL25B	7	LDQ29	C (LVDS)*	
G2	PL13A	7	LDQ16	T	PL26A	7	LDQ29	T	
G1	PL13B	7	LDQ16	C	PL26B	7	LDQ29	C	
H3	PL14A	7	LDQ16	T (LVDS)*	PL27A	7	LDQ29	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
H4	PL14B	7	LDQ16	C (LVDS)*	PL27B	7	LDQ29	C (LVDS)*	
J5	PL15A	7	LDQ16	T	PL28A	7	LDQ29	T	
J4	PL15B	7	LDQ16	C	PL28B	7	LDQ29	C	
J3	PL16A	7	LDQS16	T (LVDS)*	PL29A	7	LDQS29	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
K4	PL16B	7	LDQ16	C (LVDS)*	PL29B	7	LDQ29	C (LVDS)*	
H1	PL17A	7	LDQ16	T	PL30A	7	LDQ29	T	
H2	PL17B	7	LDQ16	C	PL30B	7	LDQ29	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K6	PL18A	7	LDQ16	T (LVDS)*	PL31A	7	LDQ29	T (LVDS)*	
K7	PL18B	7	LDQ16	C (LVDS)*	PL31B	7	LDQ29	C (LVDS)*	
J1	PL19A	7	LDQ16	T	PL32A	7	LDQ29	T	
J2	PL19B	7	LDQ16	C	PL32B	7	LDQ29	C	
GND	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K3	PL23A	7	LDQ24	T	PL36A	7	LDQ37	T	
K2	PL23B	7	LDQ24	C	PL36B	7	LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
K1	PL24A	7	LDQS24***	T (LVDS)*	PL37A	7	LDQS37***	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT35B	0		C	PT44B	0		C
B7	PT35A	0		T	PT44A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT34B	0		C	PT43B	0		C
D10	PT34A	0		T	PT43A	0		T
H11	PT33B	0		C	PT42B	0		C
G11	PT33A	0		T	PT42A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT32B	0		C	PT41B	0		C
B6	PT32A	0		T	PT41A	0		T
D8	PT31B	0		C	PT40B	0		C
C8	PT31A	0		T	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT30B	0		C	PT39B	0		C
E10	PT30A	0		T	PT39A	0		T
E9	PT29B	0		C	PT38B	0		C
D9	PT29A	0		T	PT38A	0		T
G10	PT28B	0		C	PT37B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT28A	0		T	PT37A	0		T
A5	PT27B	0		C	PT36B	0		C
B5	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT26A	0		T	PT35A	0		T
E8	PT25B	0		C	PT34B	0		C
F10	PT25A	0		T	PT34A	0		T
F8	PT24B	0		C	PT33B	0		C
H9	PT24A	0		T	PT33A	0		T
C5	PT23B	0		C	PT32B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT23A	0		T	PT32A	0		T
B4	PT22B	0			PT31B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T17	PR51A	8	D2***	T	PR66A	8	D2***	T	
T22	PR50B	8	D3***	C	PR65B	8	D3***	C	
GNDIO	GNDIO8	-			GNDIO8	-			
R22	PR50A	8	D4***	T	PR65A	8	D4***	T	
T15	PR49B	8	D5***	C	PR64B	8	D5***	C	
R17	PR49A	8	D6***	T	PR64A	8	D6***	T	
T20	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C	
VCCIO	VCCIO8	8			VCCIO8	8			
T21	PR48A	8	DI/CSSPI0N***	T	PR63A	8	DI/CSSPI0N***	T	
R21	PR47B	8	DOU/CSON/CSSPI1N***	C	PR62B	8	DOU/CSON/CSSPI1N***	C	
R20	PR47A	8	BUSY/SISPI***	T	PR62A	8	BUSY/SISPI***	T	
R16	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
R18	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C	
GNDIO	GNDIO3	-			GNDIO3	-			
R19	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T	
P22	PR44B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*	
P21	PR44A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*	
P16	PR43B	3	RLM0_GPLL_C_IN_A**	C	PR58B	3	RLM0_GPLL_C_IN_A**/RDQ57	C	
VCCIO	VCCIO3	3			VCCIO3	3			
P17	PR43A	3	RLM0_GPLLT_IN_A**	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T	
P20	PR42B	3	RLM0_GPLL_C_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLL_C_FB_A/RDQ57	C (LVDS)*	
P19	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57****	T (LVDS)*	
GNDIO	GNDIO3	-			GNDIO3	-			
-	-	-			VCCIO3	3			
P18	PR41B	3	RDQ38	C	PR51B	3	RDQ48	C	
N16	PR41A	3	RDQ38	T	PR51A	3	RDQ48	T	
GNDIO	GNDIO3	-			GNDIO3	-			
N22	PR40B	3	RDQ38	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*	
N21	PR40A	3	RDQ38	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*	
N17	PR39B	3	RDQ38	C	PR49B	3	RDQ48	C	
N18	PR39A	3	RDQ38	T	PR49A	3	RDQ48	T	
VCCIO	VCCIO3	3			VCCIO3	3			
M22	PR38B	3	RDQ38	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*	
M21	PR38A	3	RDQS38	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*	
M16	PR37B	3	RDQ38	C	PR47B	3	RDQ48	C	
GNDIO	GNDIO3	-			GNDIO3	-			
M17	PR37A	3	RDQ38	T	PR47A	3	RDQ48	T	
M20	PR36B	3	RDQ38	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*	
M19	PR36A	3	RDQ38	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*	
M18	PR35B	3	RDQ38	C	PR45B	3	RDQ48	C	
VCCIO	VCCIO3	3			VCCIO3	3			
L16	PR35A	3	RDQ38	T	PR45A	3	RDQ48	T	
L22	PR34B	3	RDQ38	C (LVDS)*	PR44B	3	RDQ48	C (LVDS)*	
L21	PR34A	3	RDQ38	T (LVDS)*	PR44A	3	RDQ48	T (LVDS)*	
K22	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C	
VCCIO	VCCIO3	3			VCCIO3	3			
K21	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T	
L17	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U9	PL67B	6	LDQ66	C	PL72B	6	LDQ71	C	
AA5	PL68A	6	LDQ66	T (LVDS)*	PL73A	6	LDQ71	T*	
AA6	PL68B	6	LDQ66	C (LVDS)*	PL73B	6	LDQ71	C*	
Y7	PL69A	6	LDQ66	T	PL74A	6	LDQ71	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V9	PL69B	6	LDQ66	C	PL74B	6	LDQ71	C	
AC3	TCK	-			TCK	-			
W8	TDI	-			TDI	-			
AC4	TMS	-			TMS	-			
V8	TDO	-			TDO	-			
AA7	VCCJ	-			VCCJ	-			
AB6	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T	
Y8	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C	
AD1	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD2	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AC5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AA8	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC6	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
AB7	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
Y9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AD3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA9	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
W10	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC7	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
Y10	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AE2	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO5	-			
AE4	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
AE3	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AB8	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AE5	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD6	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AA10	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AC8	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
W12	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC9	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
W13	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AB10	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AF3	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T2	PL45B	6	LLM3_SPLLC_IN_A	C (LVDS)*	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*	
U9	PL46A	6	LLM3_SPLLT_FB_A	T	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T	
U8	PL46B	6	LLM3_SPLLC_FB_A	C	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C	
VCCIO	VCCIO6	6			GNDIO6	-			
U5	PL48A	6	LDQ52	T (LVDS)*	PL60A	6	LDQ64	T (LVDS)*	
U4	PL48B	6	LDQ52	C (LVDS)*	PL60B	6	LDQ64	C (LVDS)*	
V9	PL49A	6	LDQ52	T	PL61A	6	LDQ64	T	
V7	PL49B	6	LDQ52	C	PL61B	6	LDQ64	C	
VCCIO	VCCIO6	6			VCCIO6	6			
U3	PL50A	6	LDQ52	T (LVDS)*	PL62A	6	LDQ64	T (LVDS)*	
U2	PL50B	6	LDQ52	C (LVDS)*	PL62B	6	LDQ64	C (LVDS)*	
V8	PL51A	6	LDQ52	T	PL63A	6	LDQ64	T	
U6	PL51B	6	LDQ52	C	PL63B	6	LDQ64	C	
GNDIO	GNDIO6	-			GNDIO6	-			
U1	PL52A	6	LDQS52	T (LVDS)*	PL64A	6	LDQS64	T (LVDS)*	
V2	PL52B	6	LDQ52	C (LVDS)*	PL64B	6	LDQ64	C (LVDS)*	
V5	PL53A	6	LDQ52	T	PL65A	6	LDQ64	T	
VCCIO	VCCIO6	6			VCCIO6	6			
V6	PL53B	6	LDQ52	C	PL65B	6	LDQ64	C	
V1	PL54A	6	LDQ52	T (LVDS)*	PL66A	6	LDQ64	T (LVDS)*	
W1	PL54B	6	LDQ52	C (LVDS)*	PL66B	6	LDQ64	C (LVDS)*	
W5	PL55A	6	LDQ52	T	PL67A	6	LDQ64	T	
GNDIO	GNDIO6	-			GNDIO6	-			
W6	PL55B	6	LDQ52	C	PL67B	6	LDQ64	C	
W3	PL57A	6		T (LVDS)*	PL69A	6	LDQ73	T (LVDS)*	
W4	PL57B	6		C (LVDS)*	PL69B	6	LDQ73	C (LVDS)*	
W2	PL58A	6		T	PL70A	6	LDQ73	T	
Y4	PL58B	6		C	PL70B	6	LDQ73	C	
Y1	PL59A	6		T (LVDS)*	PL71A	6	LDQ73	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
Y2	PL59B	6		C (LVDS)*	PL71B	6	LDQ73	C (LVDS)*	
Y5	PL60A	6		T	PL72A	6	LDQ73	T	
Y6	PL60B	6		C	PL72B	6	LDQ73	C	
AA1	NC	-			PL73A	6	LDQS73	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
AA2	NC	-			PL73B	6	LDQ73	C (LVDS)*	
Y3	NC	-			PL74A	6	LDQ73	T	
AB1	NC	-			PL74B	6	LDQ73	C	
-	-	-			VCCIO6	6			
Y9	NC	-			PL75A	6	LDQ73	T (LVDS)*	
Y8	NC	-			PL75B	6	LDQ73	C (LVDS)*	
Y7	NC	-			PL76A	6	LDQ73	T	
AA7	NC	-			PL76B	6	LDQ73	C	
-	-	-			GNDIO6	-			
-	-	-			-	-			
AB2	NC	-			PL78A	6	LDQ82	T (LVDS)*	
AB3	NC	-			PL78B	6	LDQ82	C (LVDS)*	
AA5	NC	-			PL79A	6	LDQ82	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y15	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
AA26	NC	-			NC	-		
AB10	PL73B	6	LDQ71	C (LVDS)*	NC	-		
AB11	NC	-			NC	-		
AB12	NC	-			NC	-		
AB13	NC	-			NC	-		
AB14	NC	-			NC	-		
AB15	NC	-			NC	-		
AB16	NC	-			NC	-		
AB17	NC	-			NC	-		
AB19	NC	-			NC	-		
AB20	NC	-			NC	-		
AB21	NC	-			NC	-		
AB9	PL73A	6	LDQ71	T (LVDS)*	NC	-		
AC10	PL74B	6	LDQ71	C	NC	-		
AC11	NC	-			NC	-		
AC21	NC	-			NC	-		
AC22	NC	-			NC	-		
AC8	PL70B	6	LDQ71	C	NC	-		
AC9	PL74A	6	LDQ71	T	NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD4	PL68A	6	LDQ71	T	NC	-		
AD5	PL68B	6	LDQ71	C	NC	-		
AD6	PL71A	6	LDQS71	T (LVDS)*	NC	-		
AD7	PL72A	6	LDQ71	T	NC	-		
AD8	PL72B	6	LDQ71	C	NC	-		
AE23	NC	-			NC	-		
AE5	PL69A	6	LDQ71	T (LVDS)*	NC	-		
AE6	PL70A	6	LDQ71	T	NC	-		
AE7	PL71B	6	LDQ71	C (LVDS)*	NC	-		
AF20	NC	-			NC	-		
AF23	NC	-			NC	-		
AF5	PL69B	6	LDQ71	C (LVDS)*	NC	-		
AG23	NC	-			NC	-		
AG26	NC	-			NC	-		
D10	PT10A	0		T	NC	-		
E10	PT9B	0		C	NC	-		
E11	PT10B	0		C	NC	-		
F10	PT9A	0		T	NC	-		
F20	NC	-			NC	-		
F23	NC	-			NC	-		
F8	PL6B	7	LDQ6	C (LVDS)*	NC	-		
G10	NC	-			NC	-		
G20	NC	-			NC	-		
G21	NC	-			NC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M10	VCCIO7	7		
M7	VCCIO7	7		
N10	VCCIO7	7		
N3	VCCIO7	7		
P10	VCCIO7	7		
R6	VCCIO7	7		
AA25	VCCIO8	8		
AD28	VCCIO8	8		
AA10	VCCAUX	-		
AA11	VCCAUX	-		
AA20	VCCAUX	-		
AA21	VCCAUX	-		
K10	VCCAUX	-		
K11	VCCAUX	-		
K20	VCCAUX	-		
K21	VCCAUX	-		
L10	VCCAUX	-		
L11	VCCAUX	-		
L20	VCCAUX	-		
L21	VCCAUX	-		
Y10	VCCAUX	-		
Y11	VCCAUX	-		
Y20	VCCAUX	-		
Y21	VCCAUX	-		
A1	GND	-		
A13	GND	-		
A18	GND	-		
A24	GND	-		
A30	GND	-		
A7	GND	-		
AA14	GND	-		
AA15	GND	-		
AA16	GND	-		
AA17	GND	-		
AA24	GND	-		
AA27	GND	-		
AA4	GND	-		
AB24	GND	-		
AB7	GND	-		
AD12	GND	-		
AD19	GND	-		
AD27	GND	-		
AE22	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F21	GND	-			GND	-		
G31	GND	-			GND	-		
G4	GND	-			GND	-		
J12	GND	-			GND	-		
J16	GND	-			GND	-		
J19	GND	-			GND	-		
J23	GND	-			GND	-		
K27	GND	-			GND	-		
K31	GND	-			GND	-		
K4	GND	-			GND	-		
K8	GND	-			GND	-		
M16	GND	-			GND	-		
M17	GND	-			GND	-		
M18	GND	-			GND	-		
M19	GND	-			GND	-		
N16	GND	-			GND	-		
N17	GND	-			GND	-		
N18	GND	-			GND	-		
N19	GND	-			GND	-		
N26	GND	-			GND	-		
N31	GND	-			GND	-		
N4	GND	-			GND	-		
N9	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R19	GND	-			GND	-		
T12	GND	-			GND	-		
T13	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T19	GND	-			GND	-		
T20	GND	-			GND	-		
T22	GND	-			GND	-		
T23	GND	-			GND	-		
T26	GND	-			GND	-		
T31	GND	-			GND	-		
T4	GND	-			GND	-		
T9	GND	-			GND	-		
U12	GND	-			GND	-		
U13	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U19	GND	-			GND	-		
U20	GND	-			GND	-		

LatticeECP2 Standard Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	COM	6
LFE2-6E-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	COM	6
LFE2-6E-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	COM	6
LFE2-6E-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	COM	6
LFE2-6E-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	COM	6
LFE2-6E-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	COM	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	COM	12
LFE2-12E-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	COM	12
LFE2-12E-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	COM	12
LFE2-12E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	12
LFE2-12E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	12
LFE2-12E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	12
LFE2-12E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	12
LFE2-12E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	12
LFE2-12E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	12
LFE2-12E-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	COM	12
LFE2-12E-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	COM	12
LFE2-12E-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	COM	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	20
LFE2-20E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	20
LFE2-20E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	20
LFE2-20E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2-20E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2-20E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	20
LFE2-20E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2-20E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2-20E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2-20E-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	COM	20
LFE2-20E-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	COM	20
LFE2-20E-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	20
LFE2-20E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	20
LFE2-20E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2-20E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	20
LFE2-20E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2-20E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2-20E-5FN672I	402	1.2V	-5	Lead-Free fpBGA	672	IND	20
LFE2-20E-6FN672I	402	1.2V	-6	Lead-Free fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2-35E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2-35E-5FN672I	450	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2-35E-6FN672I	450	1.2V	-6	Lead-Free fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484I	339	1.2V	-5	Lead-Free fpBGA	484	IND	50
LFE2-50E-6FN484I	339	1.2V	-6	Lead-Free fpBGA	484	IND	50
LFE2-50E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	50
LFE2-50E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	70
LFE2-70E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	70
LFE2-70E-5FN900I	583	1.2V	-5	Lead-Free fpBGA	900	IND	70
LFE2-70E-6FN900I	583	1.2V	-6	Lead-Free fpBGA	900	IND	70

LatticeECP2M Standard Series Devices, Conventional Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484C	304	1.2V	-5	fpBGA	484	COM	20
LFE2M20E-6F484C	304	1.2V	-6	fpBGA	484	COM	20
LFE2M20E-7F484C	304	1.2V	-7	fpBGA	484	COM	20
LFE2M20E-5F256C	140	1.2V	-5	fpBGA	256	COM	20
LFE2M20E-6F256C	140	1.2V	-6	fpBGA	256	COM	20
LFE2M20E-7F256C	140	1.2V	-7	fpBGA	256	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672C	410	1.2V	-5	fpBGA	672	COM	35
LFE2M35E-6F672C	410	1.2V	-6	fpBGA	672	COM	35
LFE2M35E-7F672C	410	1.2V	-7	fpBGA	672	COM	35
LFE2M35E-5F484C	303	1.2V	-5	fpBGA	484	COM	35
LFE2M35E-6F484C	303	1.2V	-6	fpBGA	484	COM	35
LFE2M35E-7F484C	303	1.2V	-7	fpBGA	484	COM	35
LFE2M35E-5F256C	140	1.2V	-5	fpBGA	256	COM	35
LFE2M35E-6F256C	140	1.2V	-6	fpBGA	256	COM	35
LFE2M35E-7F256C	140	1.2V	-7	fpBGA	256	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900C	410	1.2V	-5	fpBGA	900	COM	50
LFE2M50E-6F900C	410	1.2V	-6	fpBGA	900	COM	50
LFE2M50E-7F900C	410	1.2V	-7	fpBGA	900	COM	50
LFE2M50E-5F672C	372	1.2V	-5	fpBGA	672	COM	50
LFE2M50E-6F672C	372	1.2V	-6	fpBGA	672	COM	50
LFE2M50E-7F672C	372	1.2V	-7	fpBGA	672	COM	50
LFE2M50E-5F484C	270	1.2V	-5	fpBGA	484	COM	50
LFE2M50E-6F484C	270	1.2V	-6	fpBGA	484	COM	50
LFE2M50E-7F484C	270	1.2V	-7	fpBGA	484	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152C	436	1.2V	-5	fpBGA	1152	COM	70
LFE2M70E-6F1152C	436	1.2V	-6	fpBGA	1152	COM	70
LFE2M70E-7F1152C	436	1.2V	-7	fpBGA	1152	COM	70
LFE2M70E-5F900C	416	1.2V	-5	fpBGA	900	COM	70
LFE2M70E-6F900C	416	1.2V	-6	fpBGA	900	COM	70
LFE2M70E-7F900C	416	1.2V	-7	fpBGA	900	COM	70