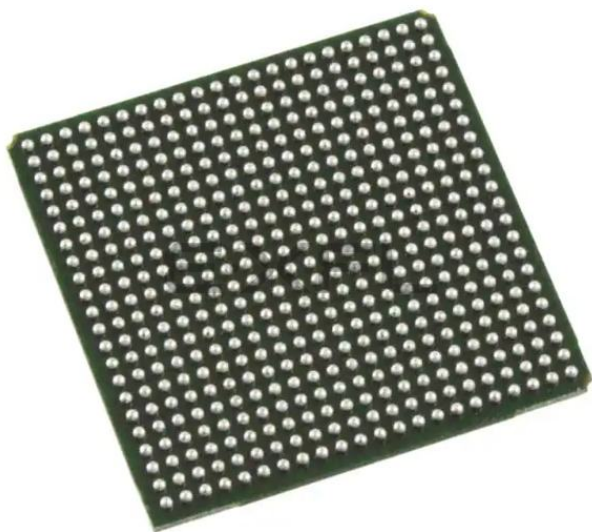




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

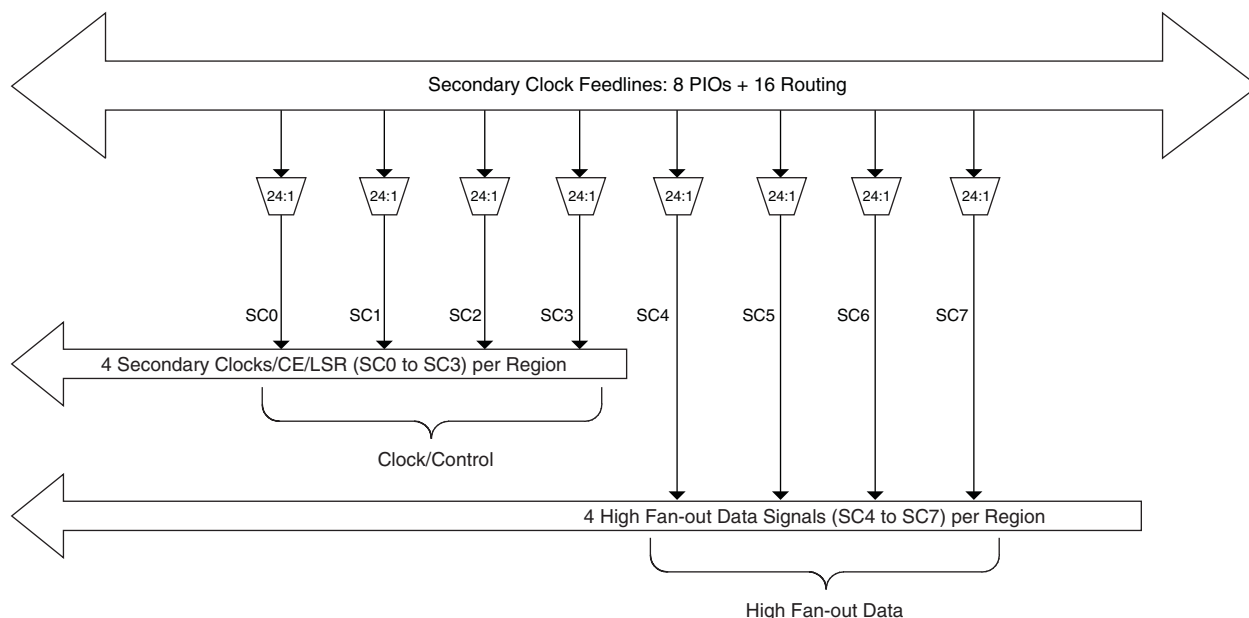
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	396288
Number of I/O	339
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-50e-6f484c

Figure 2-16. Secondary Clock Selection

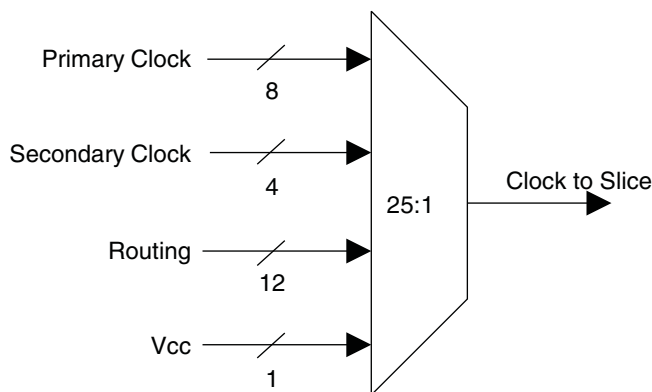


Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

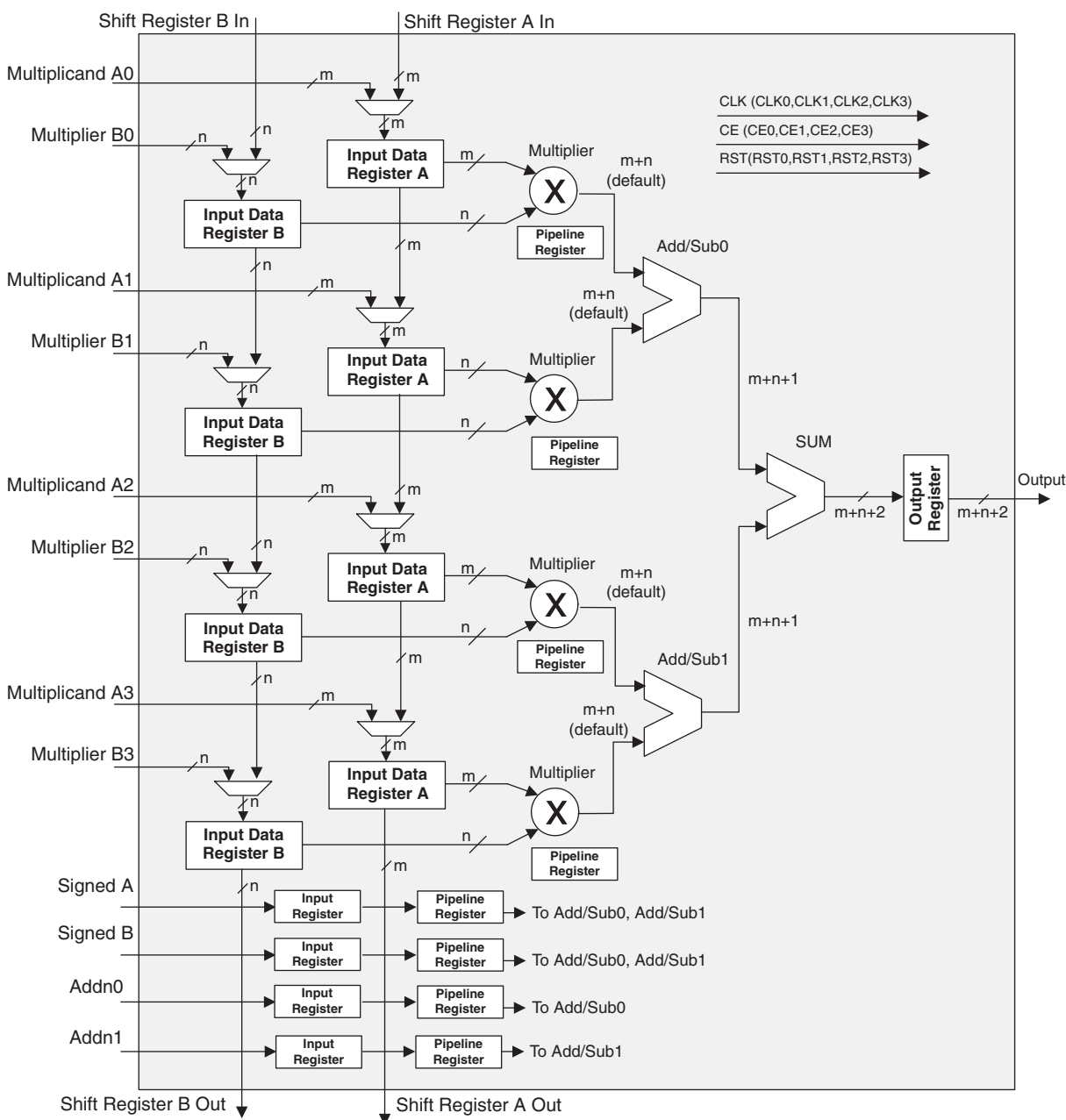
Figure 2-17. Slice0 through Slice2 Clock Selection



MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

Figure 2-26. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

3. Left and Right (Banks 2, 3, 6 and 7) sys/I/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sys/I/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

4. Bank 8 sys/I/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sys/I/O buffers in Bank 8 consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

In LatticeECP2 devices, only the I/Os on the bottom banks have programmable PCI clamps. In LatticeECP2M devices, the I/Os on the left and bottom banks have programmable PCI clamps.

Typical sys/I/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP2/M devices, see the list of additional technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Prior to and throughout programming of the FPGA, the I/O of the device have a weak-pullup resistor to V_{CCIO} on the input buffer and the output buffer is tri-stated. A pullup to V_{CCIO} is present on the input until the user programs the input differently in the FPGA design. See the [DC Electrical Characteristics](#) table of this data sheet. The pullup value will be between 20-30K ohms based on the V_{CCIO} voltage supplied on the board. This pullup will also remain active if the design does not use a particular I/O.

Supported sys/I/O Standards

The LatticeECP2/M sys/I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTTL and other standards. The buffers support the LVTTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSQS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/

LatticeECP2 Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply Current	ECP2-6	10	mA
		ECP2-12	20	mA
		ECP2-20	30	mA
		ECP2-35	50	mA
		ECP2-50	70	mA
		ECP2-70	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	24	mA
		ECP2-12	24	mA
		ECP2-20	24	mA
		ECP2-35	24	mA
		ECP2-50	24	mA
		ECP2-70	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2-6	2	mA
		ECP2-12	2	mA
		ECP2-20	2	mA
		ECP2-35	2	mA
		ECP2-50	2	mA
		ECP2-70	2	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a "blank" configuration data file.
5. $T_J = 25^{\circ}\text{C}$, power supplies at normal voltage.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

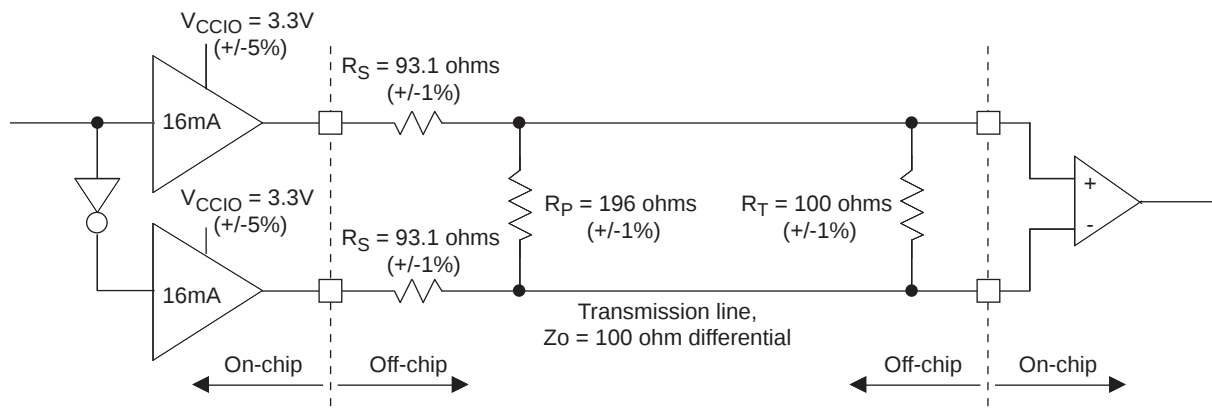


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply ($\pm 5\%$)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor ($\pm 1\%$)	93	Ω
R_P	Driver Parallel Resistor ($\pm 1\%$)	196	Ω
R_T	Receiver Termination ($\pm 1\%$)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	3.8	ns
32-bit Decoder	4.5	ns
64-bit Decoder	5.0	ns
4:1 MUX	3.2	ns
8:1 MUX	3.4	ns
16:1 MUX	3.5	ns
32:1 MUX	4.0	ns

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	599	MHz
32-bit Decoder	542	MHz
64-bit Decoder	417	MHz
4:1 MUX	847	MHz
8:1 MUX	803	MHz
16:1 MUX	660	MHz
32:1 MUX	577	MHz
8-bit Adder	591	MHz
16-bit Adder	500	MHz
64-bit Adder	306	MHz
16-bit Counter	488	MHz
32-bit Counter	378	MHz
64-bit Counter	260	MHz
64-bit Accumulator	253	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	280	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	819	MHz
32x4 Pseudo-Dual Port RAM	521	MHz
64x8 Pseudo-Dual Port RAM	435	MHz
DSP Functions		
18x18 Multiplier (All Registers)	420	MHz
9x9 Multiplier (All Registers)	420	MHz

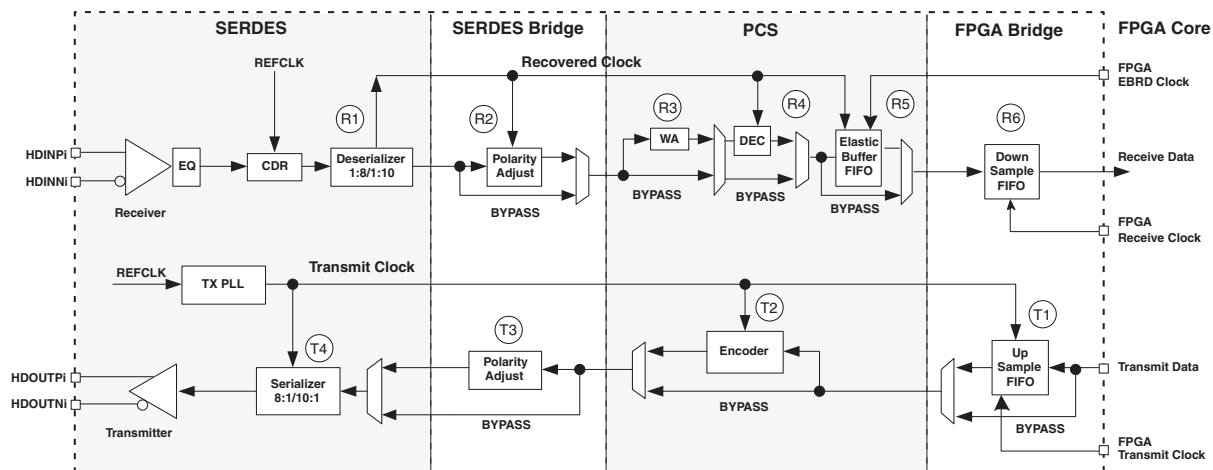
LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps) ⁵									
t _{SUXGMII}	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{DVBCKXGMII}	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
t _{DVACKXGMII}	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

- General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
- DDR timing numbers based on SSTL25 for BGA packages only.
- DDR2 timing numbers based on SSTL18 for BGA packages only.
- SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
- XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
- IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
- Using the LVDS I/O standard.
- ECP2-6 and ECP2-12 do not support SPI4.2
- The AC numbers do not apply to PCLK6 and PCLK7.
- Applies to CLKOP only.
- Please refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#) for best performance.

Figure 3-12. Transmitter and Receiver Block Diagram



Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See “Typical sysI/O I/O Behavior During Power-up” for more information about I/O behavior during power-up.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V _{CCPLL}	—	PLL supply pins. Should be tied to V _{CC} even when the corresponding PLL is unused.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES ⁴	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP ⁴	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V _{CCPLL}	—	Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A ⁵	I	Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A ⁵	I	Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.

LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M19	NC	-			PR26A	3	RDQ25	T
J22	NC	-			PR23B	3	RDQ25	C (LVDS)*
-	-	-			GNDIO	-		
L22	NC	-			PR24B	3	RDQ25	C
H22	NC	-			PR23A	3	RDQ25	T (LVDS)*
K22	NC	-			PR24A	3	RDQ25	T
M20	PR16B	3	VREF2_3	C	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO3	3			VCCIO3	3		
L21	PR16A	3	VREF1_3	T	PR22A	3	VREF1_3/RDQ25	T
K21	PR15B	3	PCLKC3_0	C (LVDS)*	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J21	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
M18	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
L17	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T
L19	PR12B	2	RDQ10	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
K18	PR10B	2	RDQ10	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
L20	PR12A	2	RDQ10	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR10A	2	RDQS10	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
L18	PR11B	2	RDQ10	C	PR17B	2	RDQ16	C
K17	PR11A	2	RDQ10	T	PR17A	2	RDQ16	T
GNDIO	GNDIO2	-			GNDIO2	-		
J17	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*
G22	PR9B	2	RDQ10	C	PR15B	2	RDQ16	C
J18	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*
F22	PR9A	2	RDQ10	T	PR15A	2	RDQ16	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*
K20	PR7B	2	RDQ10	C	PR13B	2	RDQ16	C
G21	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*
J19	PR7A	2	RDQ10	T	PR13A	2	RDQ16	T
D22	NC	-			PR10B	2	RDQ8	C (LVDS)*
F21	NC	-			PR11B	2	RDQ8	C
-	-	-			GNDIO	-		
E21	NC	-			PR10A	2	RDQ8	T (LVDS)*
E22	NC	-			PR11A	2	RDQ8	T
H19	NC	-			PR8B	2	RDQ8	C (LVDS)*
G20	NC	-			PR9B	2	RDQ8	C
-	-	-			VCCIO2	2		
G19	NC	-			PR8A	2	RDQS8	T (LVDS)*
F20	NC	-			PR9A	2	RDQ8	T
G17	PR5B	2		C	PR7B	2	RDQ8	C
GNDIO	GNDIO2	-			GNDIO2	-		
E20	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K8	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L12	GND	-			GND	-		
L13	GND	-			GND	-		
L15	GND	-			GND	-		
L8	GND	-			GND	-		
M10	GND	-			GND	-		
M11	GND	-			GND	-		
M12	GND	-			GND	-		
M13	GND	-			GND	-		
M15	GND	-			GND	-		
M8	GND	-			GND	-		
N10	GND	-			GND	-		
N11	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N15	GND	-			GND	-		
N8	GND	-			GND	-		
P14	GND	-			GND	-		
P20	GND	-			GND	-		
P3	GND	-			GND	-		
P9	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R12	GND	-			GND	-		
R13	GND	-			GND	-		
U17	GND	-			GND	-		
U6	GND	-			GND	-		
W2	GND	-			GND	-		
W21	GND	-			GND	-		
Y14	GND	-			GND	-		
Y9	GND	-			GND	-		
A1	GND	-			GND	-		
N18	VCCPLL	-			VCCPLL	-		
K6	NC	-			VCCPLL	-		
N6	VCCPLL	-			VCCPLL	-		
J16	NC	-			VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
F6	PL5A	7	LDQ8	T	PL18A	7	LDQ21	T	
F5	PL5B	7	LDQ8	C	PL18B	7	LDQ21	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E4	PL6A	7	LDQ8	T (LVDS)*	PL19A	7	LDQ21	T (LVDS)*	
E3	PL6B	7	LDQ8	C (LVDS)*	PL19B	7	LDQ21	C (LVDS)*	
E2	PL7A	7	LDQ8	T	PL20A	7	LDQ21	T	
E1	PL7B	7	LDQ8	C	PL20B	7	LDQ21	C	
GND	GNDIO7	-			GNDIO7	-			
H6	PL8A	7	LDQS8	T (LVDS)*	PL21A	7	LDQS21	T (LVDS)*	
H5	PL8B	7	LDQ8	C (LVDS)*	PL21B	7	LDQ21	C (LVDS)*	
F2	PL9A	7	LDQ8	T	PL22A	7	LDQ21	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F1	PL9B	7	LDQ8	C	PL22B	7	LDQ21	C	
H8	PL10A	7	LDQ8	T (LVDS)*	PL23A	7	LDQ21	T (LVDS)*	
J9	PL10B	7	LDQ8	C (LVDS)*	PL23B	7	LDQ21	C (LVDS)*	
G4	PL11A	7	LDQ8	T	PL24A	7	LDQ21	T	
GND	GNDIO7	-			GNDIO7	-			
G3	PL11B	7	LDQ8	C	PL24B	7	LDQ21	C	
H7	PL12A	7	LDQ16	T (LVDS)*	PL25A	7	LDQ29	T (LVDS)*	
J8	PL12B	7	LDQ16	C (LVDS)*	PL25B	7	LDQ29	C (LVDS)*	
G2	PL13A	7	LDQ16	T	PL26A	7	LDQ29	T	
G1	PL13B	7	LDQ16	C	PL26B	7	LDQ29	C	
H3	PL14A	7	LDQ16	T (LVDS)*	PL27A	7	LDQ29	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
H4	PL14B	7	LDQ16	C (LVDS)*	PL27B	7	LDQ29	C (LVDS)*	
J5	PL15A	7	LDQ16	T	PL28A	7	LDQ29	T	
J4	PL15B	7	LDQ16	C	PL28B	7	LDQ29	C	
J3	PL16A	7	LDQS16	T (LVDS)*	PL29A	7	LDQS29	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
K4	PL16B	7	LDQ16	C (LVDS)*	PL29B	7	LDQ29	C (LVDS)*	
H1	PL17A	7	LDQ16	T	PL30A	7	LDQ29	T	
H2	PL17B	7	LDQ16	C	PL30B	7	LDQ29	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K6	PL18A	7	LDQ16	T (LVDS)*	PL31A	7	LDQ29	T (LVDS)*	
K7	PL18B	7	LDQ16	C (LVDS)*	PL31B	7	LDQ29	C (LVDS)*	
J1	PL19A	7	LDQ16	T	PL32A	7	LDQ29	T	
J2	PL19B	7	LDQ16	C	PL32B	7	LDQ29	C	
GND	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K3	PL23A	7	LDQ24	T	PL36A	7	LDQ37	T	
K2	PL23B	7	LDQ24	C	PL36B	7	LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
K1	PL24A	7	LDQS24***	T (LVDS)*	PL37A	7	LDQS37***	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C	
AE10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T	
AF10	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C	
W14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T	
AB13	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T	
AB14	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T	
AF11	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C	
AD14	PB43A	5	BDQ42	T	PB52A	5	BDQ51	T	
AA15	PB43B	5	BDQ42	C	PB52B	5	BDQ51	C	
AE12	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T	
AF12	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C	
AE13	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T	
AF13	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C	
AB17	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C	
AE14	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AF14	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
AA16	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C	
AC17	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
AB16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
AE15	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C	
AE16	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AF16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
Y16	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AB18	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AD18	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AD19	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR43B	2	RDQ41	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
K22	PR43A	2	RDQ41	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
M24	PR42B	2	RDQ41	C	PR55B	2	RDQ54	C
N23	PR42A	2	RDQ41	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR41B	2	RDQ41	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
K25	PR41A	2	RDQS41	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
M20	PR40B	2	RDQ41	C	PR53B	2	RDQ54	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR40A	2	RDQ41	T	PR53A	2	RDQ54	T
L22	PR39B	2	RDQ41	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
M22	PR39A	2	RDQ41	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
K21	PR38B	2	RDQ41	C	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR38A	2	RDQ41	T	PR51A	2	RDQ54	T
K24	PR37B	2	RDQ41	C (LVDS)*	PR50B	2	RDQ54	C (LVDS)*
J24	PR37A	2	RDQ41	T (LVDS)*	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCCPLL	2			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
J25	PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
J23	PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
K23	PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
H26	PR24B	2	RDQ24	C (LVDS)*	PR37B	2	RDQ37	C (LVDS)*
H25	PR24A	2	RDQS24***	T (LVDS)*	PR37A	2	RDQS37***	T (LVDS)*
H24	PR23B	2	RDQ24	C	PR36B	2	RDQ37	C
GND	GNDIO2	-			GNDIO2	-		
H23	PR23A	2	RDQ24	T	PR36A	2	RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR19B	2	RDQ16	C	PR32B	2	RDQ29	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR19A	2	RDQ16	T	PR32A	2	RDQ29	T
F26	PR18B	2	RDQ16	C (LVDS)*	PR31B	2	RDQ29	C (LVDS)*
F25	PR18A	2	RDQ16	T (LVDS)*	PR31A	2	RDQ29	T (LVDS)*
K20	PR17B	2	RDQ16	C	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR17A	2	RDQ16	T	PR30A	2	RDQ29	T
E26	PR16B	2	RDQ16	C (LVDS)*	PR29B	2	RDQ29	C (LVDS)*
E25	PR16A	2	RDQS16	T (LVDS)*	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR15B	2	RDQ16	C	PR28B	2	RDQ29	C
H22	PR15A	2	RDQ16	T	PR28A	2	RDQ29	T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AH12	VCC	-			LLC_SQ_VCCR1	14			
AK8	PB16A	5	BDQ15	T	LLC_SQ_HDOUTP1	14		T	
AH8	NC	-			LLC_SQ_VCCOB1	14			
AJ8	PB16B	5	BDQ15	C	LLC_SQ_HDOUTN1	14		C	
AH9	VCC	-			LLC_SQ_VCCTX1	14			
AJ9	PB17B	5	BDQ15	C	LLC_SQ_HDOUTN0	14		C	
AK10	NC	-			LLC_SQ_VCCOB0	14			
AK9	PB17A	5	BDQ15	T	LLC_SQ_HDOUTP0	14		T	
AH10	VCC	-			LLC_SQ_VCCTX0	14			
AJ12	PB19B	5	BDQ15	C	LLC_SQ_HDINN0	14		C	
AJ13	NC	-			LLC_SQ_VCCIB0	14			
AK12	PB19A	5	BDQ15	T	LLC_SQ_HDINP0	14		T	
AH13	VCC	-			LLC_SQ_VCCR0	14			
AF10	PB3A	5	BDQ6	T	PB30A	5	BDQ33	T	
AE8	PB3B	5	BDQ6	C	PB30B	5	BDQ33	C	
AE11	PB4A	5	BDQ6	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AD9	PB4B	5	BDQ6	C	PB31B	5	BDQ33	C	
AE10	PB5A	5	BDQ6	T	PB32A	5	BDQ33	T	
AD10	PB5B	5	BDQ6	C	PB32B	5	BDQ33	C	
AE13	PB6A	5	BDQS6	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC12	PB6B	5	BDQ6	C	PB33B	5	BDQ33	C	
AG2	PB7A	5	BDQ6	T	PB34A	5	BDQ33	T	
AG3	PB7B	5	BDQ6	C	PB34B	5	BDQ33	C	
AD13	PB8A	5	BDQ6	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AC13	PB8B	5	BDQ6	C	PB35B	5	BDQ33	C	
AE14	PB9A	5	BDQ6	T	PB36A	5	BDQ33	T	
AC14	PB9B	5	BDQ6	C	PB36B	5	BDQ33	C	
AF3	PB10A	5	BDQ6	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF4	PB10B	5	BDQ6	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			-	-			
AG4	PB20A	5	BDQ24	T	PB38A	5	BDQ42	T	
AG5	PB20B	5	BDQ24	C	PB38B	5	BDQ42	C	
GNDIO	GNDIO5	-			-	-			
VCCIO	VCCIO5	5			-	-			
AD11	PB24A	5	BDQS24****	T	PB39A	5	BDQ42	T	
AF13	PB24B	5	BDQ24	C	PB39B	5	BDQ42	C	
AF12	PB25A	5	BDQ24	T	PB40A	5	BDQ42	T	
-	-	-			VCCIO5	5			
AD14	PB25B	5	BDQ24	C	PB40B	5	BDQ42	C	
AG8	PB26A	5	BDQ24	T	PB41A	5	BDQ42	T	
AF8	PB26B	5	BDQ24	C	PB41B	5	BDQ42	C	
AE15	PB27A	5	BDQ24	T	PB42A	5	BDQS42****	T	
-	-	-			GNDIO5	-			
VCCIO	VCCIO5	5			-	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
M26	PR27A	2	RDQS27	T (LVDS)*	PR37A	2	RDQS37	T (LVDS)*	
L30	PR26B	2	RDQ27	C	PR36B	2	RDQ37	C	
GNDIO	GNDIO2	-			GNDIO2	-			
L29	PR26A	2	RDQ27	T	PR36A	2	RDQ37	T	
L28	PR25B	2	RDQ27	C (LVDS)*	PR35B	2	RDQ37	C (LVDS)*	
L27	PR25A	2	RDQ27	T (LVDS)*	PR35A	2	RDQ37	T (LVDS)*	
H29	PR24B	2	RDQ27	C	PR34B	2	RDQ37	C	
VCCIO	VCCIO2	2			VCCIO2	2			
G29	PR24A	2	RDQ27	T	PR34A	2	RDQ37	T	
L22	PR23B	2	RDQ27	C (LVDS)*	PR33B	2	RDQ37	C (LVDS)*	
M22	PR23A	2	RDQ27	T (LVDS)*	PR33A	2	RDQ37	T (LVDS)*	
F30	PR21B	2		C	PR31B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
F29	PR21A	2		T	PR31A	2	RDQ28	T	
-	-	-			-	-			
-	-	-			-	-			
E30	PR20B	2		C (LVDS)*	PR30B	2	RDQ28	C (LVDS)*	
E29	PR20A	2		T (LVDS)*	PR30A	2	RDQ28	T (LVDS)*	
VCCIO	VCCIO2	2			-	-			
L25	PR19B	2		C	PR29B	2	RDQ28	C	
L26	PR19A	2		T	PR29A	2	RDQ28	T	
-	-	-			VCCIO2	2			
H28	PR18B	2		C (LVDS)*	PR28B	2	RDQ28	C (LVDS)*	
J28	PR18A	2		T (LVDS)*	PR28A	2	RDQS28	T (LVDS)*	
G28	PR16B	2		C	PR27B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
G27	PR16A	2		T	PR27A	2	RDQ28	T	
L24	NC	-			PR26B	2	RDQ28	C (LVDS)*	
L23	NC	-			PR26A	2	RDQ28	T (LVDS)*	
D30	NC	-			PR25B	2	RDQ28	C	
-	-	-			VCCIO2	2			
D29	NC	-			PR25A	2	RDQ28	T	
K24	NC	-			PR24B	2	RDQ28	C (LVDS)*	
K25	NC	-			PR24A	2	RDQ28	T (LVDS)*	
J27	NC	-			PR22B	2		C	
-	-	-			GNDIO2	-			
K26	NC	-			PR22A	2		T	
K23	PR15B	2		C (LVDS)*	PR21B	2		C (LVDS)*	
K22	PR15A	2		T (LVDS)*	PR21A	2		T (LVDS)*	
J22	PR14B	2		C	PR20B	2		C	
VCCIO	VCCIO2	-			VCCIO2	2			
J23	PR14A	2		T	PR20A	2		T	
-	-	-			GNDIO2	-			
-	-	-			-	-			
J26	NC	-			PR17B	2	RDQ15	C (LVDS)*	
H26	NC	-			PR17A	2	RDQ15	T (LVDS)*	
H27	NC	-			PR16B	2	RDQ15	C	
G26	NC	-			PR16A	2	RDQ15	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
J16	PT51B	1		C	PT60B	1		C	
G15	PT51A	1		T	PT60A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT50B	1		C	PT59B	1		C	
D16	PT50A	1		T	PT59A	1		T	
J15	PT49B	1		C	PT58B	1		C	
H15	PT49A	1		T	PT58A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A15	PT48B	1	VREF2_1	C	PT57B	1	VREF2_1	C	
B15	PT48A	1	VREF1_1	T	PT57A	1	VREF1_1	T	
F15	PT47B	1	PCLKC1_0	C	PT56B	1	PCLKC1_0	C	
E16	PT47A	1	PCLKT1_0	T	PT56A	1	PCLKT1_0	T	
C15	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
D15	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T	
C14	PT45B	0	VREF2_0	C	PT54B	0	VREF2_0	C	
E15	PT45A	0	VREF1_0	T	PT54A	0	VREF1_0	T	
G14	PT44B	0		C	PT53B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J14	PT44A	0		T	PT53A	0		T	
F14	PT43B	0		C	PT52B	0		C	
H14	PT43A	0		T	PT52A	0		T	
A14	PT42B	0		C	PT51B	0		C	
B14	PT42A	0		T	PT51A	0		T	
D13	PT41B	0		C	PT50B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F13	PT41A	0		T	PT50A	0		T	
G13	PT40B	0		C	PT49B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J11	PT40A	0		T	PT49A	0		T	
D4	PT38B	0		C	PT47B	0		C	
D5	PT38A	0		T	PT47A	0		T	
E5	PT37B	0		C	PT46B	0		C	
F6	PT37A	0		T	PT46A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT34B	0		C	PT43B	0		C	
D8	PT34A	0		T	PT43A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
J13	PT32B	0		C	PT41B	0		C	
G11	PT32A	0		T	PT41A	0		T	
H13	PT31B	0		C	PT40B	0		C	
H12	PT31A	0		T	PT40A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
E8	PT30B	0		C	PT39B	0		C	
D9	PT30A	0		T	PT39A	0		T	
D12	PT28B	0		C	PT37B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R21	VCC	-			VCC	-		
R22	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T21	VCC	-			VCC	-		
U14	VCC	-			VCC	-		
U21	VCC	-			VCC	-		
V14	VCC	-			VCC	-		
V21	VCC	-			VCC	-		
W14	VCC	-			VCC	-		
W21	VCC	-			VCC	-		
Y13	VCC	-			VCC	-		
Y14	VCC	-			VCC	-		
Y21	VCC	-			VCC	-		
Y22	VCC	-			VCC	-		
C12	VCCIO0	0			VCCIO0	0		
C16	VCCIO0	0			VCCIO0	0		
E14	VCCIO0	0			VCCIO0	0		
H12	VCCIO0	0			VCCIO0	0		
H16	VCCIO0	0			VCCIO0	0		
M14	VCCIO0	0			VCCIO0	0		
M15	VCCIO0	0			VCCIO0	0		
C19	VCCIO1	1			VCCIO1	1		
C23	VCCIO1	1			VCCIO1	1		
E21	VCCIO1	1			VCCIO1	1		
H19	VCCIO1	1			VCCIO1	1		
H23	VCCIO1	1			VCCIO1	1		
M20	VCCIO1	1			VCCIO1	1		
M21	VCCIO1	1			VCCIO1	1		
G32	VCCIO2	2			VCCIO2	2		
K28	VCCIO2	2			VCCIO2	2		
K32	VCCIO2	2			VCCIO2	2		
N27	VCCIO2	2			VCCIO2	2		
N32	VCCIO2	2			VCCIO2	2		
P23	VCCIO2	2			VCCIO2	2		
R23	VCCIO2	2			VCCIO2	2		
T27	VCCIO2	2			VCCIO2	2		
T32	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
AB27	VCCIO3	3			VCCIO3	3		
AB32	VCCIO3	3			VCCIO3	3		
AE28	VCCIO3	3			VCCIO3	3		
AE32	VCCIO3	3			VCCIO3	3		
AH32	VCCIO3	3			VCCIO3	3		
W27	VCCIO3	3			VCCIO3	3		
W32	VCCIO3	3			VCCIO3	3		
Y23	VCCIO3	3			VCCIO3	3		
AC20	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
AG19	VCCIO4	4			VCCIO4	4		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100