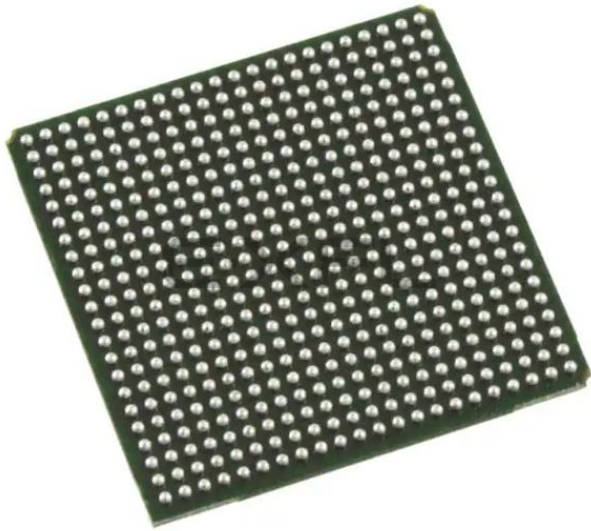




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	396288
Number of I/O	339
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-50se-5f484i

IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The Math-Works® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

Table 2-14. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS	N/A	2.5
MLVDS ¹	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3
RSDS ¹	N/A	2.5
LVC MOS33D ¹	4mA, 8mA, 12mA, 16mA, 20mA	3.3

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

Hot Socketing

LatticeECP2/M devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2/M ideal for many multiple power supply and hot-swap applications.

SERDES Power Supply Requirements (LatticeECP2M Family Only)¹

Over Recommended Operating Conditions

Symbol	Description	Typ. ²	Units
Standby (Power Down)			
I _{CCTX-SB}	V _{CCTX} current (per channel)	10	μA
I _{CCR_X-SB}	V _{CCR_X} current (per channel)	75	μA
I _{CCIB-SB}	Input buffer current (per channel)	0	μA
I _{CCOB-SB}	Output buffer current (per channel)	0	μA
I _{CCP-SB}	SERDES PLL current (per quad)	30	μA
I _{CCAX33-SB}	SERDES termination current (per quad)	10	μA
Operating (Data Rate = 3.125 Gbps)			
I _{CCTX-OP}	V _{CCTX} current (per channel)	19	mA
I _{CCR_X-OP}	V _{CCR_X} current (per channel)	34	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	mA
I _{CCOB-OP}	Output buffer current (per channel)	13	mA
I _{CCP-OP}	SERDES PLL current (per quad)	26	mA
I _{CCAX33-OP}	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.

2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power¹

Symbol	Description	Typ. ²	Units
P _{S-1CH-31}	SERDES power (one channel @ 3.125 Gbps)	90	mW
P _{S-1CH-25}	SERDES power (one channel @ 2.5 Gbps)	87	mW
P _{S-1CH-12}	SERDES power (one channel @ 1.25 Gbps)	86	mW
P _{S-1CH-02}	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

2. Typical values measured at 25°C and 1.2V.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

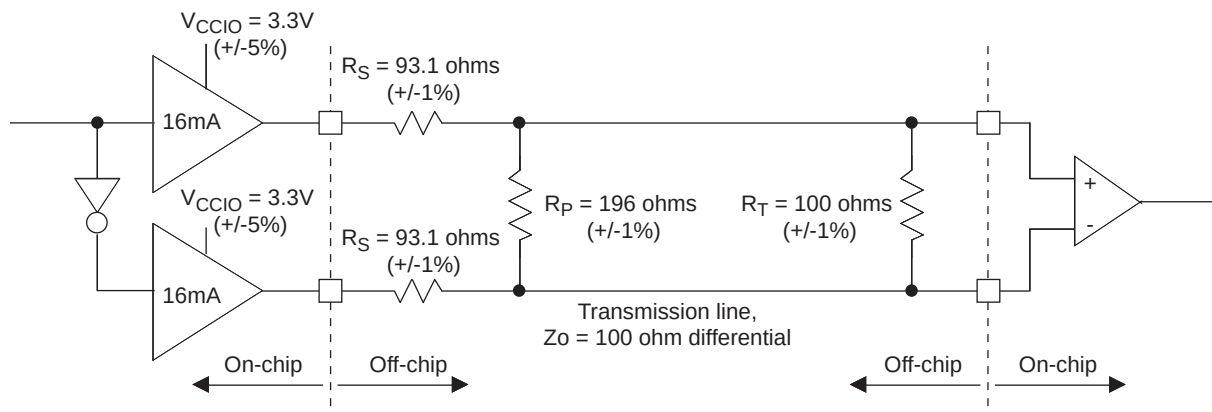


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{HPLL}	Clock to Data Hold - PIO Input Register	LFE2-6	1.00	—	1.20	—	1.40	—	ns
		LFE2-12	1.00	—	1.20	—	1.40	—	ns
		LFE2-20	1.00	—	1.20	—	1.40	—	ns
		LFE2-35	1.00	—	1.20	—	1.40	—	ns
		LFE2-50	1.00	—	1.20	—	1.40	—	ns
		LFE2-70	1.00	—	1.20	—	1.40	—	ns
		LFE2M20	1.00	—	1.20	—	1.40	—	ns
		LFE2M35	1.00	—	1.20	—	1.40	—	ns
		LFE2M50	1.00	—	1.20	—	1.40	—	ns
		LFE2M70	1.00	—	1.20	—	1.40	—	ns
		LFE2M100	1.00	—	1.20	—	1.40	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.80	—	2.00	—	2.20	—	ns
		LFE2-12	1.80	—	2.00	—	2.20	—	ns
		LFE2-20	1.80	—	2.00	—	2.20	—	ns
		LFE2-35	1.80	—	2.00	—	2.20	—	ns
		LFE2-50	1.80	—	2.00	—	2.20	—	ns
		LFE2-70	1.80	—	2.00	—	2.20	—	ns
		LFE2M20	1.80	—	2.00	—	2.20	—	ns
		LFE2M35	1.80	—	2.00	—	2.20	—	ns
		LFE2M50	1.90	—	2.10	—	2.30	—	ns
		LFE2M70	1.90	—	2.10	—	2.30	—	ns
		LFE2M100	2.00	—	2.20	—	2.40	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
DDR I/O Pin Parameters ²									
t _{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t _{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t _{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f _{MAX_DDR}	DDR Clock Frequency ⁶	ECP2/M	95	200	95	166	95	133	MHz
DDR2 I/O Pin Parameters ³									
t _{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND ¹	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	LFE2M50: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 LFE2M70/LFE2M100: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC ²	LFE2M35: AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 LFE2M50: AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	LFE2M50: G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 LFE2M70/LFE2M100: AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
-	-	-			-	-			
D3	PL5A	7		T	PL5A	7		T	
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
D2	PL5B	7		C	PL5B	7		C	
GND	GNDIO7	-			GNDIO7	-			
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T	
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C	
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C	
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*	
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T	
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
GND	GNDIO6	-			GNDIO6	-			
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	
G10	VCC	-			VCC	-			
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T	
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C	

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C	
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T	
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C	
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T	
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T	
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T	
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C	
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T	
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T	
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
VCCIO	VCCIO4	4			VCCIO	4			
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T	
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO	4			
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T	
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C	
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T	
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W19	CFG2	8			CFG2	8			
V19	CFG1	8			CFG1	8			

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB29B	5	BDQ33	C	PB29B	5	BDQ33	C	
AE10	PB30A	5	BDQ33	T	PB30A	5	BDQ33	T	
AF10	PB30B	5	BDQ33	C	PB30B	5	BDQ33	C	
W14	PB31A	5	BDQ33	T	PB31A	5	BDQ33	T	
AB13	PB31B	5	BDQ33	C	PB31B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB32A	5	BDQ33	T	PB32A	5	BDQ33	T	
AB14	PB32B	5	BDQ33	C	PB32B	5	BDQ33	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB33A	5	BDQS33	T	PB33A	5	BDQS33	T	
AF11	PB33B	5	BDQ33	C	PB33B	5	BDQ33	C	
AD14	PB34A	5	BDQ33	T	PB34A	5	BDQ33	T	
AA15	PB34B	5	BDQ33	C	PB34B	5	BDQ33	C	
AE12	PB35A	5	PCLKT5_0/BDQ33	T	PB35A	5	PCLKT5_0/BDQ33	T	
AF12	PB35B	5	PCLKC5_0/BDQ33	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB40A	4	PCLKT4_0/BDQ42	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB40B	4	PCLKC4_0/BDQ42	C	PB40B	4	PCLKC4_0/BDQ42	C	
AE13	PB41A	4	BDQ42	T	PB41A	4	BDQ42	T	
AF13	PB41B	4	BDQ42	C	PB41B	4	BDQ42	C	
AB17	PB42A	4	BDQS42	T	PB42A	4	BDQS42	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB42B	4	BDQ42	C	PB42B	4	BDQ42	C	
AE14	PB43A	4	BDQ42	T	PB43A	4	BDQ42	T	
AF14	PB43B	4	BDQ42	C	PB43B	4	BDQ42	C	
AA16	PB44A	4	BDQ42	T	PB44A	4	BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB44B	4	BDQ42	C	PB44B	4	BDQ42	C	
AC17	PB45A	4	BDQ42	T	PB45A	4	BDQ42	T	
AB16	PB45B	4	BDQ42	C	PB45B	4	BDQ42	C	
AE15	PB46A	4	BDQ42	T	PB46A	4	BDQ42	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB46B	4	BDQ42	C	PB46B	4	BDQ42	C	
AE16	PB47A	4	BDQ51	T	PB47A	4	BDQ51	T	
AF16	PB47B	4	BDQ51	C	PB47B	4	BDQ51	C	
Y16	PB48A	4	BDQ51	T	PB48A	4	BDQ51	T	
AB18	PB48B	4	BDQ51	C	PB48B	4	BDQ51	C	
AD17	PB49A	4	BDQ51	T	PB49A	4	BDQ51	T	
AD18	PB49B	4	BDQ51	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB50A	4	BDQ51	T	PB50A	4	BDQ51	T	
AD19	PB50B	4	BDQ51	C	PB50B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB51A	4	BDQS51	T	PB51A	4	BDQS51	T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G24	PR6B	2	RDQ8	C (LVDS)*	PR12B	2	RDQ14	C (LVDS)*
G23	PR6A	2	RDQ8	T (LVDS)*	PR12A	2	RDQ14	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR5B	2	RDQ8	C	PR11B	2	RDQ14	C
J19	PR5A	2	RDQ8	T	PR11A	2	RDQ14	T
D26	PR4B	2	RDQ8	C (LVDS)*	PR10B	2	RDQ14	C (LVDS)*
C26	PR4A	2	RDQ8	T (LVDS)*	PR10A	2	RDQ14	T (LVDS)*
F22	NC	-			PR9B	2	RDQ6	C
E24	NC	-			PR9A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
D25	NC	-			PR8B	2	RDQ6	C (LVDS)*
C25	NC	-			PR8A	2	RDQ6	T (LVDS)*
D24	NC	-			PR7B	2	RDQ6	C
B25	NC	-			PR7A	2	RDQ6	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	NC	-			PR6B	2	RDQ6	C (LVDS)*
G22	NC	-			PR6A	2	RDQS6	T (LVDS)*
B24	NC	-			PR5B	2	RDQ6	C
GND	GNDIO2	-			GNDIO2	-		
C24	NC	-			PR5A	2	RDQ6	T
D23	NC	-			PR4B	2	RDQ6	C (LVDS)*
C23	NC	-			PR4A	2	RDQ6	T (LVDS)*
G21	PR3B	2		C	PR3B	2	RDQ6	C
VCCIO	VCCIO2	2			VCCIO2	2		
H20	PR3A	2		T	PR3A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2/RDQ6	C (LVDS)*
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2/RDQ6	T (LVDS)*
E23	PT64B	1	VREF2_1	C	PT73B	1	VREF2_1	C
GND	GNDIO1	-			GNDIO1	-		
D22	PT64A	1	VREF1_1	T	PT73A	1	VREF1_1	T
G20	PT63B	1		C	PT72B	1		C
J18	PT63A	1		T	PT72A	1		T
F20	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H19	PT62A	1		T	PT71A	1		T
A24	PT61B	1		C	PT70B	1		C
A23	PT61A	1		T	PT70A	1		T
E21	PT60B	1		C	PT69B	1		C
F19	PT60A	1		T	PT69A	1		T
C22	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
E20	PT59A	1		T	PT68A	1		T
B22	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B23	PT58A	1		T	PT67A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR43B	2	RDQ41	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
K22	PR43A	2	RDQ41	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
M24	PR42B	2	RDQ41	C	PR55B	2	RDQ54	C
N23	PR42A	2	RDQ41	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR41B	2	RDQ41	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
K25	PR41A	2	RDQS41	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
M20	PR40B	2	RDQ41	C	PR53B	2	RDQ54	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR40A	2	RDQ41	T	PR53A	2	RDQ54	T
L22	PR39B	2	RDQ41	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
M22	PR39A	2	RDQ41	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
K21	PR38B	2	RDQ41	C	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR38A	2	RDQ41	T	PR51A	2	RDQ54	T
K24	PR37B	2	RDQ41	C (LVDS)*	PR50B	2	RDQ54	C (LVDS)*
J24	PR37A	2	RDQ41	T (LVDS)*	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCCPLL	2			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
J25	PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
J23	PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
K23	PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
H26	PR24B	2	RDQ24	C (LVDS)*	PR37B	2	RDQ37	C (LVDS)*
H25	PR24A	2	RDQS24***	T (LVDS)*	PR37A	2	RDQS37***	T (LVDS)*
H24	PR23B	2	RDQ24	C	PR36B	2	RDQ37	C
GND	GNDIO2	-			GNDIO2	-		
H23	PR23A	2	RDQ24	T	PR36A	2	RDQ37	T
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR19B	2	RDQ16	C	PR32B	2	RDQ29	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR19A	2	RDQ16	T	PR32A	2	RDQ29	T
F26	PR18B	2	RDQ16	C (LVDS)*	PR31B	2	RDQ29	C (LVDS)*
F25	PR18A	2	RDQ16	T (LVDS)*	PR31A	2	RDQ29	T (LVDS)*
K20	PR17B	2	RDQ16	C	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR17A	2	RDQ16	T	PR30A	2	RDQ29	T
E26	PR16B	2	RDQ16	C (LVDS)*	PR29B	2	RDQ29	C (LVDS)*
E25	PR16A	2	RDQS16	T (LVDS)*	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR15B	2	RDQ16	C	PR28B	2	RDQ29	C
H22	PR15A	2	RDQ16	T	PR28A	2	RDQ29	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
E21	PT76A	1		T
VCCIO	VCCIO1	1		
B22	PT75B	1		C
A22	PT75A	1		T
H20	PT74B	1		C
F21	PT74A	1		T
F20	PT73B	1		C
GND	GNDIO1	-		
H19	PT73A	1		T
D21	PT72B	1		C
C21	PT72A	1		T
E20	PT71B	1		C
VCCIO	VCCIO1	1		
G21	PT71A	1		T
B21	PT70B	1		C
A21	PT70A	1		T
F19	PT69B	1		C
G20	PT69A	1		T
E19	PT68B	1		C
GND	GNDIO1	-		
G19	PT68A	1		T
D20	PT67B	1		C
VCCIO	VCCIO1	1		
C20	PT67A	1		T
B20	PT66B	1		C
A20	PT66A	1		T
F18	PT65B	1		C
H18	PT65A	1		T
D19	PT64B	1		C
C19	PT64A	1		T
GND	GNDIO1	-		
G18	PT63B	1		C
E18	PT63A	1		T
H17	PT62B	1		C
F17	PT62A	1		T
VCCIO	VCCIO1	1		
G17	PT61B	1		C
E17	PT61A	1		T
B19	PT60B	1		C
A19	PT60A	1		T
GND	GNDIO1	-		
D17	PT59B	1		C
B18	PT59A	1		T

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
F20	PR30A	2	RDQ27	T
GNDIO	GNDIO2	-		
G17	PR29B	2	RDQ27	C (LVDS)*
F17	PR29A	2	RDQ27	T (LVDS)*
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E22	PR14B	2		C
D22	PR14A	2		T
VCCIO	VCCIO2	-		
E20	PR13B	2		C (LVDS)*
D20	PR13A	2		T (LVDS)*
D19	PR12B	2	RUM0_SPLLC_FB_A	C
GNDIO	GNDIO2	-		
E19	PR12A	2	RUM0_SPLLT_FB_A	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*
VCCIO	VCCIO2	-		
E18	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-		
D18	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
F16	XRES	-		
C22	URC_SQ_VCCR0	12		
A21	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCR1	12		
B20	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
P8	PL45A	6	LDQ48	T	PL49A	6	LDQ52	T	
R6	PL45B	6	LDQ48	C	PL49B	6	LDQ52	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T1	PL46A	6	LDQ48	T (LVDS)*	PL50A	6	LDQ52	T*	
U1	PL46B	6	LDQ48	C (LVDS)*	PL50B	6	LDQ52	C*	
R7	PL47A	6	LDQ48	T	PL51A	6	LDQ52	T	
T5	PL47B	6	LDQ48	C	PL51B	6	LDQ52	C	
GNDIO	GNDIO6	-			GNDIO6	-			
U3	PL48A	6	LDQS48	T (LVDS)*	PL52A	6	LDQS52	T*	
U4	PL48B	6	LDQ48	C (LVDS)*	PL52B	6	LDQ52	C*	
U5	PL49A	6	LDQ48	T	PL53A	6	LDQ52	T	
VCCIO	VCCIO6	6			VCCIO6	6			
U6	PL49B	6	LDQ48	C	PL53B	6	LDQ52	C	
U2	PL50A	6	LDQ48	T (LVDS)*	PL54A	6	LDQ52	T*	
V1	PL50B	6	LDQ48	C (LVDS)*	PL54B	6	LDQ52	C*	
W2	PL51A	6	LDQ48	T	PL55A	6	LDQ52	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V2	PL51B	6	LDQ48	C	PL55B	6	LDQ52	C	
V4	PL55A	6	LDQ57	T (LVDS)*	PL59A	6		T*	
VCCIO	VCCIO6	6			VCCIO6	6			
V3	PL55B	6	LDQ57	C (LVDS)*	PL59B	6		C*	
-	-	-			GNDIO6	-			
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	PL62A	6	LLM0_GPLLT_IN_A	T*	
GNDIO	GNDIO6	-			GNDIO6	-			
W3	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	PL62B	6	LLM0_GPLLC_IN_A	C*	
W1	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	PL63A	6	LLM0_GPLLT_FB_A	T	
Y1	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	PL63B	6	LLM0_GPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AA1	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*	PL64A	6	LLM0_GDLLT_IN_A	T*	
AB1	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	PL64B	6	LLM0_GDLLC_IN_A	C*	
U7	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T	PL65A	6	LLM0_GDLLT_FB_A	T	
V6	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	PL65B	6	LLM0_GDLLC_FB_A	C	
GNDIO	GNDIO6	-			GNDIO6	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
W5	PL62A	6	LDQ66	T (LVDS)*	PL67A	6	LDQ71	T*	
Y4	PL62B	6	LDQ66	C (LVDS)*	PL67B	6	LDQ71	C*	
U8	PL63A	6	LDQ66	T	PL68A	6	LDQ71	T	
W6	PL63B	6	LDQ66	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y3	PL64A	6	LDQ66	T (LVDS)*	PL69A	6	LDQ71	T*	
AA3	PL64B	6	LDQ66	C (LVDS)*	PL69B	6	LDQ71	C*	
V7	NC	-			PL70A	6	LDQ71	T	
Y5	PL65B	6	LDQ66	C	PL70B	6	LDQ71	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB2	PL66A	6	LDQS66	T (LVDS)*	PL71A	6	LDQS71	T*	
AA4	PL66B	6	LDQ66	C (LVDS)*	PL71B	6	LDQ71	C*	
Y6	PL67A	6	LDQ66	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M2	PL26A	7	LDQ28	T (LVDS)*	PL30A	7	LDQ32	T (LVDS)*
M1	PL26B	7	LDQ28	C (LVDS)*	PL30B	7	LDQ32	C (LVDS)*
L6	PL27A	7	LDQ28	T	PL31A	7	LDQ32	T
L5	PL27B	7	LDQ28	C	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-			GNDIO7	-		
L3	PL28A	7	LDQS28	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*
L4	PL28B	7	LDQ28	C (LVDS)*	PL32B	7	LDQ32	C (LVDS)*
M3	PL29A	7	LDQ28	T	PL33A	7	LDQ32	T
VCCIO	VCCIO7	7			VCCIO7	7		
M4	PL29B	7	LDQ28	C	PL33B	7	LDQ32	C
N1	PL30A	7	LDQ28	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*
N2	PL30B	7	LDQ28	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*
M5	PL31A	7	LDQ28	T	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
N6	PL31B	7	LDQ28	C	PL35B	7	LDQ32	C
P3	NC	-			PL37A	7		T (LVDS)*
-	-	-			GNDIO7	-		
P4	NC	-			PL37B	7		C (LVDS)*
P9	NC	-			PL38A	7		T
M7	NC	-			PL38B	7		C
-	-	-			VCCIO7	7		
P1	NC	-			PL39A	7		T (LVDS)*
P2	NC	-			PL39B	7		C (LVDS)*
N7	NC	-			PL40A	7		T
P7	NC	-			PL40B	7		C
-	-	-			GNDIO7	-		
P5	PL33A	7	LDQ37	T (LVDS)*	PL41A	7	LDQ45	T (LVDS)*
N5	PL33B	7	LDQ37	C (LVDS)*	PL41B	7	LDQ45	C (LVDS)*
P8	PL34A	7	LDQ37	T	PL42A	7	LDQ45	T
P6	PL34B	7	LDQ37	C	PL42B	7	LDQ45	C
VCCIO	VCCIO7	7			VCCIO7	7		
R3	PL35A	7	LDQ37	T (LVDS)*	PL43A	7	LDQ45	T (LVDS)*
R4	PL35B	7	LDQ37	C (LVDS)*	PL43B	7	LDQ45	C (LVDS)*
R10	PL36A	7	LDQ37	T	PL44A	7	LDQ45	T
P11	PL36B	7	LDQ37	C	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-			GNDIO7	-		
R7	PL37A	7	LDQS37	T (LVDS)*	PL45A	7	LDQS45	T (LVDS)*
R8	PL37B	7	LDQ37	C (LVDS)*	PL45B	7	LDQ45	C (LVDS)*
R5	PL38A	7	LDQ37	T	PL46A	7	LDQ45	T
VCCIO	VCCIO7	7			VCCIO7	7		
T5	PL38B	7	LDQ37	C	PL46B	7	LDQ45	C
R1	PL39A	7	LDQ37	T (LVDS)*	PL47A	7	LDQ45	T (LVDS)*
R2	PL39B	7	LDQ37	C (LVDS)*	PL47B	7	LDQ45	C (LVDS)*
R11	PL40A	7	LDQ37	T	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-			GNDIO7	-		
T10	PL40B	7	LDQ37	C	PL48B	7	LDQ45	C
T1	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
T2	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
U10	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AL8	LLC_SQ_VCCIB1	14			LLC_SQ_VCCIB1	14		
AM7	LLC_SQ_HDINN1	14		C	LLC_SQ_HDINN1	14		C
AN6	LLC_SQ_VCCRX1	14			LLC_SQ_VCCRX1	14		
AP6	LLC_SQ_HDOUTP1	14		T	LLC_SQ_HDOUTP1	14		T
AK7	LLC_SQ_VCCOB1	14			LLC_SQ_VCCOB1	14		
AP7	LLC_SQ_HDOUTN1	14		C	LLC_SQ_HDOUTN1	14		C
AN7	LLC_SQ_VCCTX1	14			LLC_SQ_VCCTX1	14		
AP8	LLC_SQ_HDOUTN0	14		C	LLC_SQ_HDOUTN0	14		C
AL9	LLC_SQ_VCCOB0	14			LLC_SQ_VCCOB0	14		
AP9	LLC_SQ_HDOUTP0	14		T	LLC_SQ_HDOUTP0	14		T
AN8	LLC_SQ_VCCTX0	14			LLC_SQ_VCCTX0	14		
AM8	LLC_SQ_HDINN0	14		C	LLC_SQ_HDINN0	14		C
AN9	LLC_SQ_VCCIB0	14			LLC_SQ_VCCIB0	14		
AM9	LLC_SQ_HDINP0	14		T	LLC_SQ_HDINP0	14		T
AL7	LLC_SQ_VCCRX0	14			LLC_SQ_VCCRX0	14		
-	-	-			VCCIO5	5		
AJ12	NC	-			PB32A	5	BDQ33	T
AH12	NC	-			PB32B	5	BDQ33	C
-	-	-			GNDIO5	-		
-	-	-			VCCIO5	5		
AL13	NC	-			PB36A	5	BDQ33	T
AK13	NC	-			PB36B	5	BDQ33	C
-	-	-			GNDIO5	-		
AE14	NC	-			PB38A	5	BDQ42	T
AG13	NC	-			PB38B	5	BDQ42	C
AN14	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AP14	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
AH14	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
AJ15	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AL14	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
AM14	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AF14	PB35A	5	BDQ33	T	PB44A	5	BDQ42	T
AF13	PB35B	5	BDQ33	C	PB44B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
AE15	PB36A	5	BDQ33	T	PB45A	5	BDQ42	T
AG14	PB36B	5	BDQ33	C	PB45B	5	BDQ42	C
AH15	PB37A	5	BDQ33	T	PB46A	5	BDQ42	T
AK15	PB37B	5	BDQ33	C	PB46B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
AL15	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T
AM15	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C
AK16	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T
AJ16	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C
AN15	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T
VCCIO	VCCIO5	5			VCCIO5	5		
AP15	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C
AG15	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T