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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	396288
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-50se-5fn672c

Table 2-14. Supported Output Standards

Output Standard	Drive	V _{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVC MOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVC MOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVC MOS18	4mA, 8mA, 12mA, 16mA	1.8
LVC MOS15	4mA, 8mA	1.5
LVC MOS12	2mA, 6mA	1.2
LVC MOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVC MOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVC MOS15, Open Drain	4mA, 8mA	—
LVC MOS12, Open Drain	2mA, 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS	N/A	2.5
MLVDS ¹	N/A	2.5
BLVDS ¹	N/A	2.5
LVPECL ¹	N/A	3.3
RSDS ¹	N/A	2.5
LVC MOS33D ¹	4mA, 8mA, 12mA, 16mA, 20mA	3.3

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

Hot Socketing

LatticeECP2/M devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2/M ideal for many multiple power supply and hot-swap applications.

RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

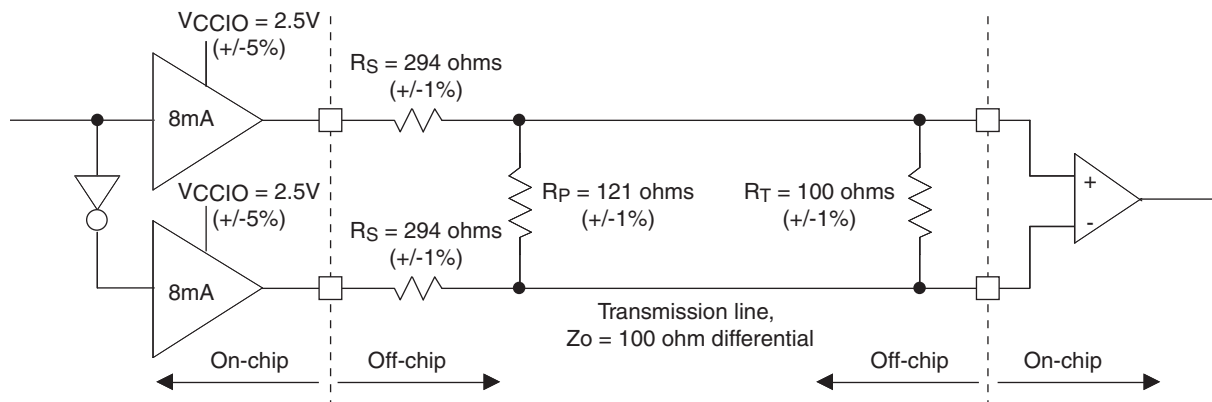


Table 3-5. RSDS DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.35	V
V _{OL}	Output Low Voltage	1.15	V
V _{OD}	Output Differential Voltage	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SUE}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _{HE}	Clock to Data Hold - PIO Input Register	LFE2-6	0.90	—	1.10	—	1.30	—	ns
		LFE2-12	0.90	—	1.10	—	1.30	—	ns
		LFE2-20	0.90	—	1.10	—	1.30	—	ns
		LFE2-35	0.90	—	1.10	—	1.30	—	ns
		LFE2-50	0.90	—	1.10	—	1.30	—	ns
		LFE2-70	0.90	—	1.10	—	1.30	—	ns
		LFE2M20	0.90	—	1.10	—	1.30	—	ns
		LFE2M35	0.90	—	1.10	—	1.30	—	ns
		LFE2M50	1.20	—	1.40	—	1.60	—	ns
		LFE2M70	1.20	—	1.40	—	1.60	—	ns
		LFE2M100	1.20	—	1.40	—	1.60	—	ns
t _{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.00	—	1.30	—	1.60	—	ns
		LFE2-12	1.00	—	1.30	—	1.60	—	ns
		LFE2-20	1.00	—	1.30	—	1.60	—	ns
		LFE2-35	1.00	—	1.30	—	1.60	—	ns
		LFE2-50	1.00	—	1.30	—	1.60	—	ns
		LFE2-70	1.00	—	1.30	—	1.60	—	ns
		LFE2M20	1.20	—	1.60	—	1.90	—	ns
		LFE2M35	1.20	—	1.60	—	1.90	—	ns
		LFE2M50	1.20	—	1.60	—	1.90	—	ns
		LFE2M70	1.20	—	1.60	—	1.90	—	ns
		LFE2M100	1.20	—	1.60	—	1.90	—	ns

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, slow slew rate	2.18	2.26	2.33	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, slow slew rate	2.19	2.35	2.51	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, slow slew rate	1.50	1.66	1.82	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, slow slew rate	1.60	1.59	1.58	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, slow slew rate	1.43	1.39	1.34	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, slow slew rate	2.22	2.27	2.32	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, slow slew rate	1.93	2.08	2.23	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, slow slew rate	1.43	1.51	1.58	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, slow slew rate	1.47	1.46	1.45	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, slow slew rate	2.32	2.38	2.43	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, slow slew rate	1.84	1.98	2.12	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, slow slew rate	2.52	2.63	2.74	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, slow slew rate	1.69	1.83	1.96	ns
PCI33	PCI33	0.04	0.04	0.04	ns

1. Timing Adders are characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. These timing adders are measured with the recommended resistor values.

Timing v.A 0.11

SERDES External Reference Clock (LatticeECP2M Family Only)

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

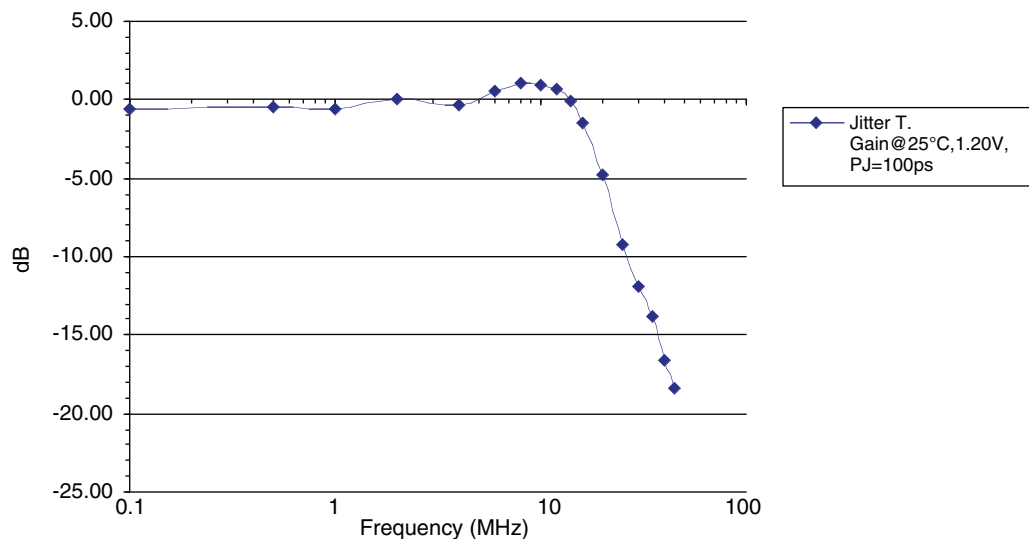
Table 3-14. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F _{REF}	Frequency range	25	—	320	MHz
F _{REF-PPM}	Frequency tolerance	-300	—	300	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ¹	100	—	1200	mV, p-p
V _{REF-IN}	Input levels	0	—	V _{CCP} + 0.8	V
V _{REF-CM-DC}	Input common mode range (DC coupled)	0.5	—	1.2	V
V _{REF-CM-AC}	Input common mode range (AC coupled) ²	0	—	1.5	V
D _{REF}	Duty cycle ³	40	—	60	%
T _{REF-R}	Rise time (20% to 80%)		500	1000	ps
T _{REF-F}	Fall time (80% to 20%)		500	1000	ps
Z _{REF-IN-TERM}	Input termination		50/2K		Ohms
C _{REF-IN-CAP}	Input capacitance ⁴	—	—	1.5	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:

$$(\text{Min input level}) + (\text{Peak-to-peak input swing})/2 \leq (\text{Input common mode voltage}) \leq (\text{Max input level}) - (\text{Peak-to-peak input swing})/2$$
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

Figure 3-13. Jitter Transfer



Note: This graph is for a nominal device.

SERDES Power-Down/Power-Up Specification

Table 3-15. Power-Down and Power-Up Specification

Symbol	Description	Max.	Units
t _{PWRDN}	Power-down time after all power down register bits set to '0'	10	μs
t _{PWRUP}	Power-up time after all power down register bits set to '1'	100	μs

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J1	J1	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
K3	K3	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
J2	J2	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
GND	GND	GNDIO6	-		
L2	L2	PL38A	6	LDQ42	T (LVDS)*
K2	K2	PL39A	6	LDQ42	T
L3	L3	PL38B	6	LDQ42	C (LVDS)*
K1	K1	PL39B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
L4	L4	PL40A	6	LDQ42	T (LVDS)*
L1	L1	PL41A	6	LDQ42	T
L5	L5	PL40B	6	LDQ42	C (LVDS)*
M1	M1	PL41B	6	LDQ42	C
GND	GND	GNDIO6	-		
N1	N1	PL43A	6	LDQ42	T
N2	N2	PL42A	6	LDQS42	T (LVDS)*
P1	P1	PL43B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
P2	P2	PL42B	6	LDQ42	C (LVDS)*
R1	R1	PL44A	6	LDQ42	T (LVDS)*
GND	GND	GNDIO6	-		
R2	R2	PL44B	6	LDQ42	C (LVDS)*
N4	N4	TDI	-		
M4	M4	TCK	-		
P3	P3	TDO	-		
N3	N3	TMS	-		
K7	K7	VCCJ	-		
M5	M5	PB2A	5	VREF2_5/BDQ6	T
K6	K6	PB3A	5	BDQ6	
M6	M6	PB2B	5	VREF1_5/BDQ6	C
R3	R3	PB5A	5	BDQ6	T
P4	P4	PB5B	5	BDQ6	C
-	VCC	VCCIO	5		
-	GND	GNDIO5	5		
N5	N5	PB30A	5	BDQ33	T
N6	N6	PB30B	5	BDQ33	C
T2	T2	PB31A	5	BDQ33	T
P6	P6	PB32A	5	BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
T3	T3	PB31B	5	BDQ33	C
R6	R6	PB32B	5	BDQ33	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T7	PL29B	6	LDQ28	C	PL43B	6	LDQ42	C	
T6	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
AA2	PL31A	6	LDQ28	T	PL45A	6	LDQ42	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y1	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	
AA1	PL31B	6	LDQ28	C	PL45B	6	LDQ42	C	
W1	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
V3	PL30B	6	LDQ28	C (LVDS)*	PL44B	6	LDQ42	C (LVDS)*	
GNDIO	GNDIO6	-			GNDIO	-			
V4	PL30A	6	LDQ28	T (LVDS)*	PL44A	6	LDQ42	T (LVDS)*	
U5	TDI	-			TDI	-			
U7	TCK	-			TCK	-			
V6	TDO	-			TDO	-			
V5	TMS	-			TMS	-			
T8	VCCJ	-			VCCJ	-			
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
GNDIO	GNDIO5	-			GNDIO	-			
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO	-			
-	-	-			VCCIO5	5			
Y6	PB12A	5	BDQ15	T	PB21A	5	BDQ24	T	
W7	PB11A	5	BDQ15	T	PB20A	5	BDQ24	T	
Y7	PB12B	5	BDQ15	C	PB21B	5	BDQ24	C	
W8	PB11B	5	BDQ15	C	PB20B	5	BDQ24	C	
U8	PB14A	5	BDQ15	T	PB23A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA7	PB13A	5	BDQ15	T	PB22A	5	BDQ24	T	
U9	PB14B	5	BDQ15	C	PB23B	5	BDQ24	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A6	PT21A	0		T	PT30A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
C7	PT17B	0		C	PT26B	0		C	
D10	PT18B	0		C	PT27B	0		C	
C6	PT17A	0		T	PT26A	0		T	
E10	PT18A	0		T	PT27A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F10	PT15B	0		C	PT24B	0		C	
B6	PT16B	0		C	PT25B	0		C	
D9	PT15A	0		T	PT24A	0		T	
B5	PT16A	0		T	PT25A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
A5	PT13B	0		C	PT22B	0		C	
F9	PT14B	0		C	PT23B	0		C	
A4	PT13A	0		T	PT22A	0		T	
E9	PT14A	0		T	PT23A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
G8	PT11B	0		C	PT20B	0		C	
A3	PT12B	0		C	PT21B	0		C	
E8	PT11A	0		T	PT20A	0		T	
A2	PT12A	0		T	PT21A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
-	-	-			VCCIO0	0			
C3	PT10B	0		C	PT10B	0		C	
B3	PT10A	0		T	PT10A	0		T	
-	-	-			GNDIO0	-			
E7	PT8B	0		C	PT8B	0		C	
F8	PT9B	0		C	PT9B	0		C	
F7	PT8A	0		T	PT8A	0		T	
D7	PT9A	0		T	PT9A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
D4	PT6B	0		C	PT6B	0		C	
D5	PT7B	0		C	PT7B	0		C	
C4	PT6A	0		T	PT6A	0		T	
D6	PT7A	0		T	PT7A	0		T	
GNDIO	GNDIO0	-			GNDIO	-			
J7	PT4B	0		C	PT4B	0		C	
B2	PT5B	0		C	PT5B	0		C	
H7	PT4A	0		T	PT4A	0		T	
B1	PT5A	0		T	PT5A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
D3	PT3B	0		C	PT3B	0		C	
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K8	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L12	GND	-			GND	-		
L13	GND	-			GND	-		
L15	GND	-			GND	-		
L8	GND	-			GND	-		
M10	GND	-			GND	-		
M11	GND	-			GND	-		
M12	GND	-			GND	-		
M13	GND	-			GND	-		
M15	GND	-			GND	-		
M8	GND	-			GND	-		
N10	GND	-			GND	-		
N11	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N15	GND	-			GND	-		
N8	GND	-			GND	-		
P14	GND	-			GND	-		
P20	GND	-			GND	-		
P3	GND	-			GND	-		
P9	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R12	GND	-			GND	-		
R13	GND	-			GND	-		
U17	GND	-			GND	-		
U6	GND	-			GND	-		
W2	GND	-			GND	-		
W21	GND	-			GND	-		
Y14	GND	-			GND	-		
Y9	GND	-			GND	-		
A1	GND	-			GND	-		
N18	VCCPLL	-			VCCPLL	-		
K6	NC	-			VCCPLL	-		
N6	VCCPLL	-			VCCPLL	-		
J16	NC	-			VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
F6	PL5A	7	LDQ8	T	PL18A	7	LDQ21	T	
F5	PL5B	7	LDQ8	C	PL18B	7	LDQ21	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E4	PL6A	7	LDQ8	T (LVDS)*	PL19A	7	LDQ21	T (LVDS)*	
E3	PL6B	7	LDQ8	C (LVDS)*	PL19B	7	LDQ21	C (LVDS)*	
E2	PL7A	7	LDQ8	T	PL20A	7	LDQ21	T	
E1	PL7B	7	LDQ8	C	PL20B	7	LDQ21	C	
GND	GNDIO7	-			GNDIO7	-			
H6	PL8A	7	LDQS8	T (LVDS)*	PL21A	7	LDQS21	T (LVDS)*	
H5	PL8B	7	LDQ8	C (LVDS)*	PL21B	7	LDQ21	C (LVDS)*	
F2	PL9A	7	LDQ8	T	PL22A	7	LDQ21	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F1	PL9B	7	LDQ8	C	PL22B	7	LDQ21	C	
H8	PL10A	7	LDQ8	T (LVDS)*	PL23A	7	LDQ21	T (LVDS)*	
J9	PL10B	7	LDQ8	C (LVDS)*	PL23B	7	LDQ21	C (LVDS)*	
G4	PL11A	7	LDQ8	T	PL24A	7	LDQ21	T	
GND	GNDIO7	-			GNDIO7	-			
G3	PL11B	7	LDQ8	C	PL24B	7	LDQ21	C	
H7	PL12A	7	LDQ16	T (LVDS)*	PL25A	7	LDQ29	T (LVDS)*	
J8	PL12B	7	LDQ16	C (LVDS)*	PL25B	7	LDQ29	C (LVDS)*	
G2	PL13A	7	LDQ16	T	PL26A	7	LDQ29	T	
G1	PL13B	7	LDQ16	C	PL26B	7	LDQ29	C	
H3	PL14A	7	LDQ16	T (LVDS)*	PL27A	7	LDQ29	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
H4	PL14B	7	LDQ16	C (LVDS)*	PL27B	7	LDQ29	C (LVDS)*	
J5	PL15A	7	LDQ16	T	PL28A	7	LDQ29	T	
J4	PL15B	7	LDQ16	C	PL28B	7	LDQ29	C	
J3	PL16A	7	LDQS16	T (LVDS)*	PL29A	7	LDQS29	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
K4	PL16B	7	LDQ16	C (LVDS)*	PL29B	7	LDQ29	C (LVDS)*	
H1	PL17A	7	LDQ16	T	PL30A	7	LDQ29	T	
H2	PL17B	7	LDQ16	C	PL30B	7	LDQ29	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K6	PL18A	7	LDQ16	T (LVDS)*	PL31A	7	LDQ29	T (LVDS)*	
K7	PL18B	7	LDQ16	C (LVDS)*	PL31B	7	LDQ29	C (LVDS)*	
J1	PL19A	7	LDQ16	T	PL32A	7	LDQ29	T	
J2	PL19B	7	LDQ16	C	PL32B	7	LDQ29	C	
GND	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K3	PL23A	7	LDQ24	T	PL36A	7	LDQ37	T	
K2	PL23B	7	LDQ24	C	PL36B	7	LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
K1	PL24A	7	LDQS24***	T (LVDS)*	PL37A	7	LDQS37***	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
AB19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AE19	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AA17	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	
AF18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T	
AF19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T	
W17	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C	
Y19	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
Y17	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
AF20	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
AA20	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
W18	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
AD20	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
GND	GNDIO4	-			GNDIO4	-			
AE21	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
AF21	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
AF22	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T	
AD22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C	
AF23	PB75A	4	BDQ78	T	PB93A	4	BDQ96	T	
AE23	PB75B	4	BDQ78	C	PB93B	4	BDQ96	C	
AD23	PB76A	4	BDQ78	T	PB94A	4	BDQ96	T	
AC23	PB76B	4	BDQ78	C	PB94B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T	
AC20	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T	
AC22	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C	
W19	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T	
AA21	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C	
AF24	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T	
AE24	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T	
AB22	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C	

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO6	-			GNDIO6	-		
L1	PL42A	6	LLM0_GPLLT_IN_A	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57***	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
L2	PL42B	6	LLM0_GPLLC_IN_A	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*
L3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T
L4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C
VCCIO	VCCIO6	6			VCCIO6	6		
M1	PL44A	6	LLM0_GDLLT_IN_A	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*
N1	PL44B	6	LLM0_GDLLC_IN_A	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*
N2	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T
N3	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C
GNDIO	GNDIO6	-			GNDIO6	-		
M4	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	-			GNDIO6	-		
K6	TCK	-			TCK	-		
L5	TDI	-			TDI	-		
N4	TMS	-			TMS	-		
N6	TDO	-			TDO	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T
N5	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C
L6	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
M6	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
P3	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
P4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
P2	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
P1	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
R1	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	-			GNDIO5	-		
R2	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
R3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
T2	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
R4	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
T4	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
GNDIO	GNDIO5	-			GNDIO5	-		
T5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
T6	PB16A	5	VREF2_5/BDQ15	T	PB34A	5	VREF2_5/BDQ33	T
R6	PB16B	5	VREF1_5/BDQ15	C	PB34B	5	VREF1_5/BDQ33	C
P6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T
P7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N11	CCLK	8			CCLK	8		
M11	INITN	8			INITN	8		
N13	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
M12	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
M13	PR53A	8	CS1N	T	PR68A	8	CS1N	T
N14	PR52B	8	CSN	C	PR67B	8	CSN	C
N15	PR52A	8	D0/SPIFASTN	T	PR67A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
N16	PR51B	8	D1	C	PR66B	8	D1	C
M16	PR51A	8	D2	T	PR66A	8	D2	T
L12	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
L13	PR50A	8	D4	T	PR65A	8	D4	T
L16	PR49B	8	D5	C	PR64B	8	D5	C
K16	PR49A	8	D6	T	PR64A	8	D6	T
L14	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C
VCCIO	VCCIO8	8			VCCIO8	8		
L15	PR48A	8	DI/CSSPI0N	T	PR63A	8	DI/CSSPI0N	T
K13	PR47B	8	DOUT/CSON/CSSPI1N	C	PR62B	8	DOUT/CSON/CSSPI1N	C
K14	PR47A	8	BUSY/SISPI	T	PR62A	8	BUSY/SISPI	T
K11	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
K15	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C
GNDIO	GNDIO3	-			GNDIO3	-		
J16	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T
H16	PR44B	3	RLM0_GDLLC_IN_A	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*
J15	PR44A	3	RLM0_GDLLT_IN_A	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*
J14	PR43B	3	RLM0_GPLLC_IN_A	C	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C
VCCIO	VCCIO3	3			VCCIO3	3		
J13	PR43A	3	RLM0_GPLLT_IN_A	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T
H13	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C (LVDS)*
H12	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57***	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
G16	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
H15	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
E16	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*
F15	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
F16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
G15	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J11	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J12	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
G14	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
G13	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C12	URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCR2	12		
A15	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCR3	12		
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
E13	PT55B	1		C
D12	PT55A	1		T
GNDIO	GNDIO1	-		
A9	PT54B	1		C
A8	PT54A	1		T
A7	PT53B	1		C
A6	PT53A	1		T
VCCIO	VCCIO1	1		
E12	PT52B	1		C
F12	PT52A	1		T
A5	PT51B	1		C
A4	PT51A	1		T
GNDIO	GNDIO1	-		
B7	PT50B	1		C
B8	PT50A	1		T
G11	PT49B	1		C
E11	PT49A	1		T
VCCIO	VCCIO1	1		
D11	PT48B	1	VREF2_1	C
D10	PT48A	1	VREF1_1	T
G10	PT47B	1	PCLKC1_0	C
F11	PT47A	1	PCLKT1_0	T
G9	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
F9	PT46A	0	PCLKT0_0	T
C9	PT45B	0	VREF2_0	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U9	PL67B	6	LDQ66	C	PL72B	6	LDQ71	C	
AA5	PL68A	6	LDQ66	T (LVDS)*	PL73A	6	LDQ71	T*	
AA6	PL68B	6	LDQ66	C (LVDS)*	PL73B	6	LDQ71	C*	
Y7	PL69A	6	LDQ66	T	PL74A	6	LDQ71	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V9	PL69B	6	LDQ66	C	PL74B	6	LDQ71	C	
AC3	TCK	-			TCK	-			
W8	TDI	-			TDI	-			
AC4	TMS	-			TMS	-			
V8	TDO	-			TDO	-			
AA7	VCCJ	-			VCCJ	-			
AB6	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T	
Y8	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C	
AD1	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD2	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AC5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AA8	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC6	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
AB7	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
Y9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AD3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA9	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
W10	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC7	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
Y10	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AE2	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO5	-			
AE4	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
AE3	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AB8	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AE5	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD6	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AA10	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AC8	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
W12	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC9	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
W13	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AB10	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AF3	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
Y22	PR60B	3		C	PR81B	3	RDQ82	C	
Y23	PR60A	3		T	PR81A	3	RDQ82	T	
AB26	NC	-			PR80B	3	RDQ82	C (LVDS)*	
AB27	NC	-			PR80A	3	RDQ82	T (LVDS)*	
-	-	-			VCCIO3	3			
Y24	NC	-			PR79B	3	RDQ82	C	
Y25	NC	-			PR79A	3	RDQ82	T	
AA29	NC	-			PR78B	3	RDQ82	C (LVDS)*	
Y28	NC	-			PR78A	3	RDQ82	T (LVDS)*	
Y30	NC	-			PR76B	3	RDQ73	C	
Y29	NC	-			PR76A	3	RDQ73	T	
-	-	-			GNDIO3	-			
-	-	-			-	-			
W22	NC	-			PR75B	3	RDQ73	C (LVDS)*	
V22	NC	-			PR75A	3	RDQ73	T (LVDS)*	
Y27	NC	-			PR74B	3	RDQ73	C	
-	-	-			VCCIO3	3			
Y26	NC	-			PR74A	3	RDQ73	T	
W30	NC	-			PR73B	3	RDQ73	C (LVDS)*	
W29	NC	-			PR73A	3	RDQS73	T (LVDS)*	
-	-	-			GNDIO3	-			
W25	NC	-			PR72B	3	RDQ73	C	
W26	NC	-			PR72A	3	RDQ73	T	
U29	PR59B	3		C (LVDS)*	PR71B	3	RDQ73	C (LVDS)*	
V29	PR59A	3		T (LVDS)*	PR71A	3	RDQ73	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
V30	PR58B	3		C	PR70B	3	RDQ73	C	
U30	PR58A	3		T	PR70A	3	RDQ73	T	
W27	PR57B	3		C (LVDS)*	PR69B	3	RDQ73	C (LVDS)*	
W28	PR57A	3		T (LVDS)*	PR69A	3	RDQ73	T (LVDS)*	
V24	PR55B	3	RDQ52	C	PR67B	3	RDQ64	C	
V25	PR55A	3	RDQ52	T	PR67A	3	RDQ64	T	
GNDIO	GNDIO3	-			GNDIO3	-			
U28	PR54B	3	RDQ52	C (LVDS)*	PR66B	3	RDQ64	C (LVDS)*	
U27	PR54A	3	RDQ52	T (LVDS)*	PR66A	3	RDQ64	T (LVDS)*	
U23	PR53B	3	RDQ52	C	PR65B	3	RDQ64	C	
V23	PR53A	3	RDQ52	T	PR65A	3	RDQ64	T	
VCCIO	VCCIO3	3			VCCIO3	3			
V26	PR52B	3	RDQ52	C (LVDS)*	PR64B	3	RDQ64	C (LVDS)*	
U26	PR52A	3	RDQS52	T (LVDS)*	PR64A	3	RDQS64	T (LVDS)*	
U25	PR51B	3	RDQ52	C	PR63B	3	RDQ64	C	
GNDIO	GNDIO3	-			GNDIO3	-			
U24	PR51A	3	RDQ52	T	PR63A	3	RDQ64	T	
T30	PR50B	3	RDQ52	C (LVDS)*	PR62B	3	RDQ64	C (LVDS)*	
R30	PR50A	3	RDQ52	T (LVDS)*	PR62A	3	RDQ64	T (LVDS)*	
T23	PR49B	3	RDQ52	C	PR61B	3	RDQ64	C	
VCCIO	VCCIO3	3			VCCIO3	3			
T22	PR49A	3	RDQ52	T	PR61A	3	RDQ64	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L13	VCC	-			VCC	-			
L18	VCC	-			VCC	-			
L19	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M13	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
M17	VCC	-			VCC	-			
M18	VCC	-			VCC	-			
M19	VCC	-			VCC	-			
M20	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N12	VCC	-			VCC	-			
N19	VCC	-			VCC	-			
N20	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P19	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R19	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T19	VCC	-			VCC	-			
U12	VCC	-			VCC	-			
U19	VCC	-			VCC	-			
V11	VCC	-			VCC	-			
V12	VCC	-			VCC	-			
V19	VCC	-			VCC	-			
V20	VCC	-			VCC	-			
W11	VCC	-			VCC	-			
W12	VCC	-			VCC	-			
W13	VCC	-			VCC	-			
W14	VCC	-			VCC	-			
W15	VCC	-			VCC	-			
W16	VCC	-			VCC	-			
W17	VCC	-			VCC	-			
W18	VCC	-			VCC	-			
W19	VCC	-			VCC	-			
W20	VCC	-			VCC	-			
Y12	VCC	-			VCC	-			
Y13	VCC	-			VCC	-			
Y18	VCC	-			VCC	-			
Y19	VCC	-			VCC	-			
D14	VCCIO0	0			VCCIO0	0			
E6	VCCIO0	0			VCCIO0	0			
E9	VCCIO0	0			VCCIO0	0			
F12	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C29	URC_SQ_VCCR1	12		
B28	URC_SQ_HDINN1	12		C
C28	URC_SQ_VCCIB1	12		
A28	URC_SQ_HDINP1	12		T
B24	URC_SQ_VCCAUX33	12		
E24	URC_SQ_REFCLKN	12		C
D24	URC_SQ_REFCLKP	12		T
C24	URC_SQ_VCCP	12		
A20	URC_SQ_HDINP2	12		T
C20	URC_SQ_VCCIB2	12		
B20	URC_SQ_HDINN2	12		C
C19	URC_SQ_VCCR2	12		
A23	URC_SQ_HDOUTP2	12		T
C23	URC_SQ_VCCOB2	12		
B23	URC_SQ_HDOUTN2	12		C
C22	URC_SQ_VCCTX2	12		
B22	URC_SQ_HDOUTN3	12		C
A21	URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCR3	12		
D23	PT100B	1		C
GNDIO	GNDIO1	-		
E21	PT100A	1		T
D26	PT99B	1		C
E26	PT99A	1		T
E23	PT98B	1		C
VCCIO	VCCIO1	1		
G22	PT98A	1		T
-	-	-		
D22	PT97B	1		C
F21	PT97A	1		T
G18	PT96B	1		C
H18	PT96A	1		T
D20	PT95B	1		C
GNDIO	GNDIO1	-		
D21	PT95A	1		T
E20	PT94B	1		C
VCCIO	VCCIO1	1		
E19	PT94A	1		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO5	-			GNDIO5	-		
AE16	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C
AF15	PB44A	5	BDQ42	T	PB53A	5	BDQ51	T
VCCIO	VCCIO5	5			VCCIO5	5		
AD16	PB44B	5	BDQ42	C	PB53B	5	BDQ51	C
AK17	PB45A	5	BDQ42	T	PB54A	5	BDQ51	T
AH16	PB45B	5	BDQ42	C	PB54B	5	BDQ51	C
AN16	PB46A	5	BDQ42	T	PB55A	5	BDQ51	T
GNDIO	GNDIO5	-			GNDIO5	-		
AP16	PB46B	5	BDQ42	C	PB55B	5	BDQ51	C
AL17	PB47A	5	BDQ51	T	PB56A	5	BDQ60	T
AM17	PB47B	5	BDQ51	C	PB56B	5	BDQ60	C
AN17	PB48A	5	BDQ51	T	PB57A	5	BDQ60	T
AP17	PB48B	5	BDQ51	C	PB57B	5	BDQ60	C
AD17	PB49A	5	BDQ51	T	PB58A	5	BDQ60	T
AE17	PB49B	5	BDQ51	C	PB58B	5	BDQ60	C
VCCIO	VCCIO5	5			VCCIO5	5		
AL18	PB50A	5	BDQ51	T	PB59A	5	BDQ60	T
AM18	PB50B	5	BDQ51	C	PB59B	5	BDQ60	C
GNDIO	GNDIO5	-			GNDIO5	-		
AP18	PB51A	5	BDQS51	T	PB60A	5	BDQS60	T
AN18	PB51B	5	BDQ51	C	PB60B	5	BDQ60	C
AG17	PB52A	5	VREF2_5/BDQ51	T	PB61A	5	VREF2_5/BDQ60	T
AJ17	PB52B	5	VREF1_5/BDQ51	C	PB61B	5	VREF1_5/BDQ60	C
AF17	PB53A	5	PCLKT5_0/BDQ51	T	PB62A	5	PCLKT5_0/BDQ60	T
AH17	PB53B	5	PCLKC5_0/BDQ51	C	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AF18	PB58A	4	PCLKT4_0/BDQ60	T	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4			VCCIO4	4		
AD18	PB58B	4	PCLKC4_0/BDQ60	C	PB67B	4	PCLKC4_0/BDQ69	C
AP19	PB59A	4	VREF2_4/BDQ60	T	PB68A	4	VREF2_4/BDQ69	T
AN19	PB59B	4	VREF1_4/BDQ60	C	PB68B	4	VREF1_4/BDQ69	C
AP20	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-			GNDIO4	-		
AM20	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C
AN20	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T
AM21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C
AG18	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4			VCCIO4	4		
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
AJ18	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T
AH18	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C
AK18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-			GNDIO4	-		
AK19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C
AP21	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T
AN21	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C
AL20	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T