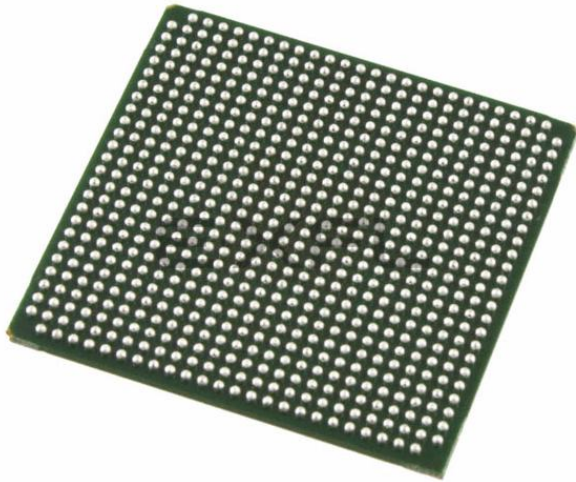




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	396288
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-50se-6f672c

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2/M family of devices has two DLLs per device.

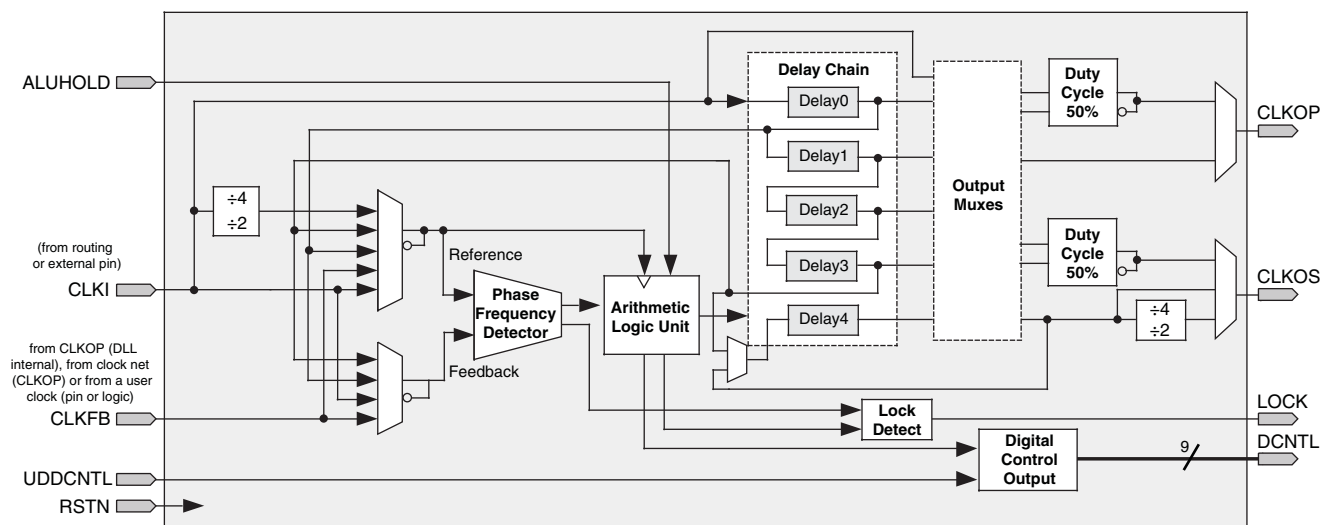
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is fed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLLDELA delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-6 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

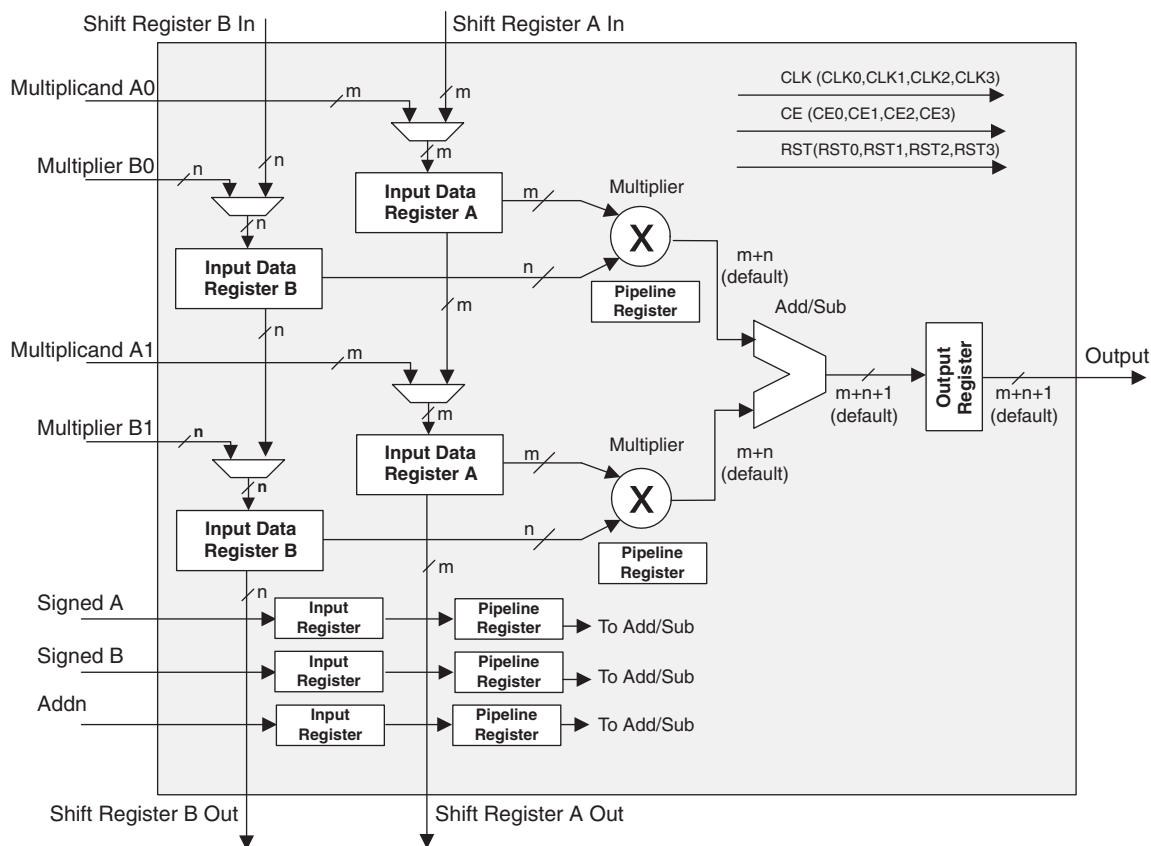
Figure 2-6. Delay Locked Loop Diagram (DLL)



MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

Figure 2-25. MULTADDSUB

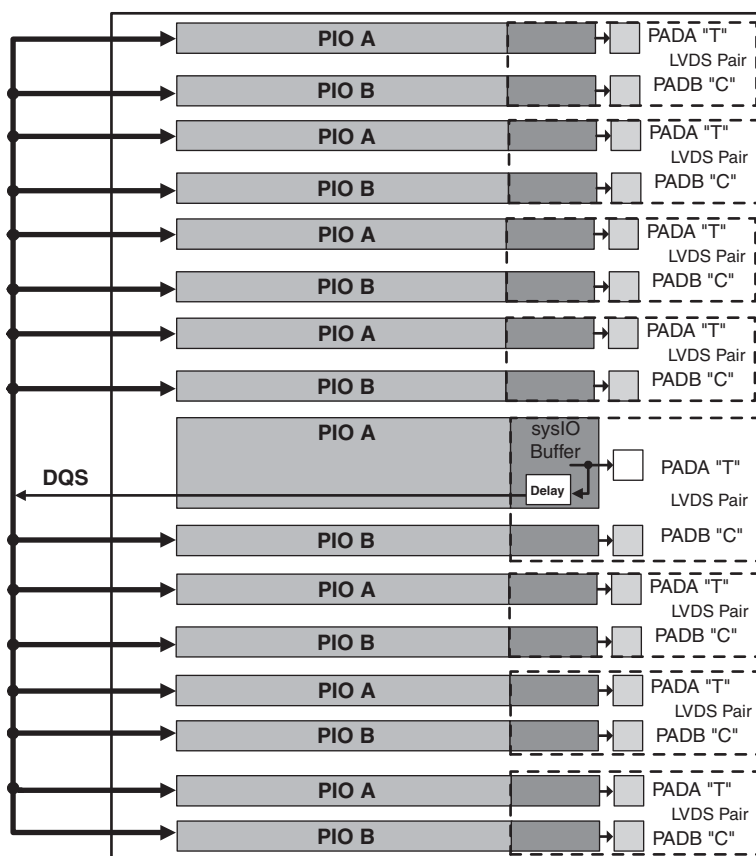


Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device



LatticeECP2 Initialization Supply Current^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ^{5, 6, 7}	Units
I_{CC}	Core Power Supply Current	ECP2-6	34	mA
		ECP2-12	54	mA
		ECP2-20	82	mA
		ECP2-35	135	mA
		ECP2-50	187	mA
		ECP2-70	267	mA
I_{CCAUx}	Auxiliary Power Supply Current	ECP2-6	30	mA
		ECP2-12	30	mA
		ECP2-20	30	mA
		ECP2-35	30	mA
		ECP2-50	30	mA
		ECP2-70	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.

6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

Table 3-9. Channel Output Jitter - x20 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.27	0.51	UI, p-p
Total	3.125 Gbps	—	0.35	0.59	UI, p-p
Deterministic	2.5 Gbps	—	0.09	0.19	UI, p-p
Random	2.5 Gbps	—	0.23	0.34	UI, p-p
Total	2.5 Gbps	—	0.29	0.45	UI, p-p
Deterministic	1.25 Gbps	—	0.05	0.11	UI, p-p
Random	1.25 Gbps	—	0.16	0.22	UI, p-p
Total	1.25 Gbps	—	0.20	0.28	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x20 mode.

Table 3-10. SERDES/PCS Latency Breakdown (Parallel Clock Cycle)

Item	Description	Min.	Average	Max.	Fixed	Bypass	Units
Transmit Data Latency							
T1	FPGA Bridge Transmit ²	1	3	5		1	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge Transmit	—	—	—	2	1	word clk
T4 ³	Serializer: 8-bit mode	—	—	—	15 + $\Delta 1$	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + $\Delta 1$	—	UI + ps
Receive Data Latency							
R1 ³	Deserializer: 8-bit mode	—	—	—	10 + $\Delta 2$	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + $\Delta 2$	—	UI + ps
R2	SERDES Bridge Receive	—	—	—	2	1	word clk
R3	Word Alignment	3.1	—	4	—	0	word clk
R4	8b10b Decoder	—	—	—	1	1	word clk
R5	Clock Tolerance Compensation	7	15	23		1	word clk
R6	FPGA Bridge Receive ²	1	3	5		1	word clk

1. PCS internal parallel clock. This clock rate is the same as rxfullclk.

2. FPGA Bridge latency varies by the upsample/downsample FIFO read/write. The numbers given are for the 8b10b interface. The depth of the downsample/upsample FIFO is 4. The earliest read can be done after the write clock cycle (one clock) in downsample FIFO. The latest read will be done after the FIFO is full (4 + 1 = 5). For the 16b20b interface, the numbers are doubled: min. = 2, max. = 10. This latency depends on the internal FIFO flag operation.

3. $\Delta 1$ = -245ps, $\Delta 2$ = 700ps

SERDES High Speed Data Receiver (LatticeECP2M Family Only)

Table 3-11. Serial Input Data Specifications

Symbol	Description	Min.	Typ.	Max.	Units
RX-CID _S	Stream of nontransitions ¹ (CID = Consecutive Identical Digits) @ 10 ⁻¹² BER		7 @ 3.125 Gbps 20 @ 1.25 Gbps		Bits
V _{RX-DIFF-S}	Differential input sensitivity	100	—	—	mV, p-p
V _{RX-IN}	Input levels	0	—	V _{CCR_X} + 0.8	V
V _{RX-CM-DC}	Input common mode range (DC coupled)	0.5	—	1.2	V
V _{RX-CM-AC}	Input common mode range (AC coupled) ³	0	—	1.5	V
T _{RX-RELOCK}	CDR re-lock time ²	—	—	3000	Bits
Z _{RX-TERM}	Input termination 50/75 Ohm/High Z	—	50		Ohms
RL _{RX-RL}	Return loss (without package)	—	9	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.
3. AC coupling is used to interface to LVPECL and LVDS.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-12. Receiver Total Jitter Tolerance Specification¹

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.54	UI, p-p
Random		600 mV differential eye	—	—	0.26	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.61	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.81	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.53	UI, p-p
Random		600 mV differential eye	—	—	0.22	UI, p-p
Total		600 mV differential eye	—	—	0.80	UI, p-p
Deterministic	250 Mbps ²	600 mV differential eye	—	—	0.42	UI, p-p
Random		600 mV differential eye	—	—	0.10	UI, p-p
Total		600 mV differential eye	—	—	0.60	UI, p-p

1. Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.
2. Jitter specification is limited by measurement equipment capability.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO6	-			GNDIO6	-		
L2	PL24A	6	LDQ28	T (LVDS)*	PL24A	6	LDQ28	T (LVDS)*
K2	PL25A	6	LDQ28	T	PL25A	6	LDQ28	T
L3	PL24B	6	LDQ28	C (LVDS)*	PL24B	6	LDQ28	C (LVDS)*
K1	PL25B	6	LDQ28	C	PL25B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
L4	PL26A	6	LDQ28	T (LVDS)*	PL26A	6	LDQ28	T (LVDS)*
L1	PL27A	6	LDQ28	T	PL27A	6	LDQ28	T
L5	PL26B	6	LDQ28	C (LVDS)*	PL26B	6	LDQ28	C (LVDS)*
M1	PL27B	6	LDQ28	C	PL27B	6	LDQ28	C
GND	GNDIO6	-			GNDIO6	-		
N1	PL29A	6	LDQ28	T	PL29A	6	LDQ28	T
N2	PL28A	6	LDQS28	T (LVDS)*	PL28A	6	LDQS28	T (LVDS)*
P1	PL29B	6	LDQ28	C	PL29B	6	LDQ28	C
VCCIO	VCCIO6	6			VCCIO6	6		
P2	PL28B	6	LDQ28	C (LVDS)*	PL28B	6	LDQ28	C (LVDS)*
R1	PL30A	6	LDQ28	T (LVDS)*	PL30A	6	LDQ28	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
R2	PL30B	6	LDQ28	C (LVDS)*	PL30B	6	LDQ28	C (LVDS)*
N4	TDI	-			TDI	-		
M4	TCK	-			TCK	-		
P3	TDO	-			TDO	-		
N3	TMS	-			TMS	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
K6	NC	-			PB3A	5	BDQ6	
M6	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
R3	NC	-			PB5A	5	BDQ6	T
P4	NC	-			PB5B	5	BDQ6	C
-	-	-			VCCIO	5		
-	-	-			GNDIO5	5		
N5	PB3A	5	BDQ6	T	PB21A	5	BDQ24	T
N6	PB3B	5	BDQ6	C	PB21B	5	BDQ24	C
T2	PB4A	5	BDQ6	T	PB22A	5	BDQ24	T
P6	PB5A	5	BDQ6	T	PB23A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB4B	5	BDQ6	C	PB22B	5	BDQ24	C
R6	PB5B	5	BDQ6	C	PB23B	5	BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
R4	PB6A	5	BDQS6	T	PB24A	5	BDQS24	T
L6	PB7A	5	BDQ6	T	PB25A	5	BDQ24	T
T4	PB6B	5	BDQ6	C	PB24B	5	BDQ24	C
L7	PB7B	5	BDQ6	C	PB25B	5	BDQ24	C
N7	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M8	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
P7	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
R8	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
VCCIO	VCCIO4	4			VCCIO4	4		
T5	PB14A	4	BDQ15	T	PB32A	4	BDQ33	T
T6	PB14B	4	BDQ15	C	PB32B	4	BDQ33	C
T8	PB15A	4	BDQS15	T	PB33A	4	BDQS33	T
GND	GNDIO4	-			GNDIO4	-		
R7	PB16A	4	BDQ15	T	PB34A	4	BDQ33	T
T9	PB15B	4	BDQ15	C	PB33B	4	BDQ33	C
T7	PB16B	4	BDQ15	C	PB34B	4	BDQ33	C
L8	PB17A	4	BDQ15	T	PB35A	4	BDQ33	T
VCCIO	VCCIO4	4			VCCIO4	4		
P8	PB18A	4	BDQ15	T	PB36A	4	BDQ33	T
L9	PB17B	4	BDQ15	C	PB35B	4	BDQ33	C
N8	PB18B	4	BDQ15	C	PB36B	4	BDQ33	C
R9	PB19A	4	BDQ15	T	PB37A	4	BDQ33	T
GND	GNDIO4	-			GNDIO4	-		
R10	PB19B	4	BDQ15	C	PB37B	4	BDQ33	C
-	-	-			VCCIO	4		
-	-	-			GNDIO4	4		
N9	PB20A	4	BDQ24	T	PB47A	4	BDQ51	T
T10	PB21A	4	BDQ24	T	PB48A	4	BDQ51	T
M9	PB20B	4	BDQ24	C	PB47B	4	BDQ51	C
R11	PB21B	4	BDQ24	C	PB48B	4	BDQ51	C
P10	PB22A	4	BDQ24	T	PB49A	4	BDQ51	T
N11	PB23A	4	BDQ24	T	PB50A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
N10	PB22B	4	BDQ24	C	PB49B	4	BDQ51	C
P11	PB23B	4	BDQ24	C	PB50B	4	BDQ51	C
T11	PB24A	4	BDQS24	T	PB51A	4	BDQS51	T
GND	GNDIO4	-			GNDIO4	-		
M11	PB25A	4	BDQ24	T	PB52A	4	BDQ51	T
T12	PB24B	4	BDQ24	C	PB51B	4	BDQ51	C
L11	PB25B	4	BDQ24	C	PB52B	4	BDQ51	C
T13	PB26A	4	BDQ24	T	PB53A	4	BDQ51	T
R13	PB27A	4	BDQ24	T	PB54A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
T14	PB26B	4	BDQ24	C	PB53B	4	BDQ51	C
P13	PB27B	4	BDQ24	C	PB54B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
N12	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
M12	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
R15	CFG2	8			CFG2	8		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
-	-	-			GNDIO7	-			
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*	
F4	PL3A	7		T	PL5A	7	LDQ8	T	
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*	
F5	PL3B	7		C	PL5B	7	LDQ8	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
G6	PL5A	7		T	PL7A	7	LDQ8	T	
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
G7	PL5B	7		C	PL7B	7	LDQ8	C	
GNDIO	GNDIO7	-			GNDIO7	-			
F1	NC	-			PL9A	7	LDQ8	T	
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*	
F2	NC	-			PL9B	7	LDQ8	C	
-	-	-			VCCIO7	7			
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*	
G1	NC	-			PL11A	7	LDQ8	T	
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*	
G2	NC	-			PL11B	7	LDQ8	C	
-	-	-			GNDIO	-			
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*	
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T	
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*	
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C	
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C	
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*	
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C	
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
VCCIO	VCCIO6	6			-	-			

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F19	PR5A	2		T	PR7A	2	RDQ8	T	
D20	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
F18	PR3B	2		C	PR5B	2	RDQ8	C	
VCCIO	VCCIO2	2			VCCIO2	2			
C21	NC	-			PR4B	2	RDQ8	C (LVDS)*	
F16	PR3A	2		T	PR5A	2	RDQ8	T	
C22	NC	-			PR4A	2	RDQ8	T (LVDS)*	
-	-	-			GNDIO	-			
D19	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
E19	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
B21	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
B22	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
GNDIO	GNDIO1	-			GNDIO1	-			
D18	PT53B	1		C	PT62B	1		C	
C20	PT54B	1		C	PT63B	1		C	
E18	PT53A	1		T	PT62A	1		T	
C19	PT54A	1		T	PT63A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D17	PT51B	1		C	PT60B	1		C	
B20	PT52B	1		C	PT61B	1		C	
C18	PT51A	1		T	PT60A	1		T	
A19	PT52A	1		T	PT61A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
A18	PT49B	1		C	PT58B	1		C	
A21	PT50B	1		C	PT59B	1		C	
B18	PT49A	1		T	PT58A	1		T	
A20	PT50A	1		T	PT59A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D16	PT47B	1		C	PT56B	1		C	
G16	PT48B	1		C	PT57B	1		C	
E16	PT47A	1		T	PT56A	1		T	
G15	PT48A	1		T	PT57A	1		T	
C17	PT46B	1		C	PT55B	1		C	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT46A	1		T	PT55A	1		T	
A17	PT44B	1		C	PT53B	1		C	
B17	PT45B	1		C	PT54B	1		C	
A16	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
B16	PT45A	1		T	PT54A	1		T	
E15	PT42B	1		C	PT51B	1		C	
C15	PT43B	1		C	PT52B	1		C	
F15	PT42A	1		T	PT51A	1		T	
D15	PT43A	1		T	PT52A	1		T	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G12	PT40B	0		C
E12	PT40A	0		T
VCCIO	VCCIO0	0		
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO0	-		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
VCCIO	VCCIO0	0		
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO0	-		
A11	PT32A	0		T
E10	PT31B	0		C
VCCIO	VCCIO0	0		
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO0	-		
VCCIO	VCCIO0	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO0	-		
D7	PT14A	0		T
D8	PT13B	0		C
VCCIO	VCCIO0	0		
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
GNDIO	GNDIO2	-			GNDIO2	-			
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			-	-			
F16	XRES	-			XRES	-			
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12			
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T	
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A18	URC_SQ_HDOUTP ₀	12		T	URC_SQ_HDOUTP ₀	12		T	
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B18	URC_SQ_HDOUTN ₀	12		C	URC_SQ_HDOUTN ₀	12		C	
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B17	URC_SQ_HDOUTN ₁	12		C	URC_SQ_HDOUTN ₁	12		C	
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A17	URC_SQ_HDOUTP ₁	12		T	URC_SQ_HDOUTP ₁	12		T	
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12			
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T	
B16	URC_SQ_VCCAUX ₃₃	12			URC_SQ_VCCAUX ₃₃	12			
E17	URC_SQ_REFCLK _N	12		C	URC_SQ_REFCLK _N	12		C	
D17	URC_SQ_REFCLK _P	12		T	URC_SQ_REFCLK _P	12		T	
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T	
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A15	URC_SQ_HDOUTP ₂	12		T	URC_SQ_HDOUTP ₂	12		T	
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B15	URC_SQ_HDOUTN ₂	12		C	URC_SQ_HDOUTN ₂	12		C	
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B14	URC_SQ_HDOUTN ₃	12		C	URC_SQ_HDOUTN ₃	12		C	
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A14	URC_SQ_HDOUTP ₃	12		T	URC_SQ_HDOUTP ₃	12		T	
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	NC	-			NC	-		
F14	NC	-			NC	-		
F13	NC	-			NC	-		
G12	NC	-			NC	-		
G13	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U21	CS1N***	8		
U17	CSN***	8		
U16	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8		
T16	D1***	8		
T17	D2***	8		
T22	D3***	8		
GNDIO	GNDIO8	-		
R22	D4***	8		
T15	D5***	8		
R17	D6***	8		
T20	D7/SPID0***	8		
VCCIO	VCCIO8	8		
T21	DI/CSSPI0N***	8		
R21	DOUT/CSON/CSSPI1N***	8		
R20	BUSY/SISPI***	8		
R16	RLM0_PLLCAP	3		
R18	PR65B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	-		
R19	PR65A	3	RLM0_GDLLT_FB_A	T
P22	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*
P21	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*
P16	PR63B	3	RLM0_GPLL_C_IN_A**	C
VCCIO	VCCIO3	3		
P17	PR63A	3	RLM0_GPLLT_IN_A**	T
P20	PR62B	3	RLM0_GPLL_C_FB_A	C (LVDS)*
P19	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*
GNDIO	GNDIO3	-		
VCCIO	VCCIO3	3		
P18	PR55B	3	RDQ52	C
N16	PR55A	3	RDQ52	T
GNDIO	GNDIO3	-		
N22	PR54B	3	RDQ52	C (LVDS)*
N21	PR54A	3	RDQ52	T (LVDS)*
N17	PR53B	3	RDQ52	C
N18	PR53A	3	RDQ52	T
VCCIO	VCCIO3	3		
M22	PR52B	3	RDQ52	C (LVDS)*
M21	PR52A	3	RDQS52	T (LVDS)*
M16	PR51B	3	RDQ52	C
GNDIO	GNDIO3	-		
M17	PR51A	3	RDQ52	T
M20	PR50B	3	RDQ52	C (LVDS)*

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
Y22	PR60B	3		C	PR81B	3	RDQ82	C	
Y23	PR60A	3		T	PR81A	3	RDQ82	T	
AB26	NC	-			PR80B	3	RDQ82	C (LVDS)*	
AB27	NC	-			PR80A	3	RDQ82	T (LVDS)*	
-	-	-			VCCIO3	3			
Y24	NC	-			PR79B	3	RDQ82	C	
Y25	NC	-			PR79A	3	RDQ82	T	
AA29	NC	-			PR78B	3	RDQ82	C (LVDS)*	
Y28	NC	-			PR78A	3	RDQ82	T (LVDS)*	
Y30	NC	-			PR76B	3	RDQ73	C	
Y29	NC	-			PR76A	3	RDQ73	T	
-	-	-			GNDIO3	-			
-	-	-			-	-			
W22	NC	-			PR75B	3	RDQ73	C (LVDS)*	
V22	NC	-			PR75A	3	RDQ73	T (LVDS)*	
Y27	NC	-			PR74B	3	RDQ73	C	
-	-	-			VCCIO3	3			
Y26	NC	-			PR74A	3	RDQ73	T	
W30	NC	-			PR73B	3	RDQ73	C (LVDS)*	
W29	NC	-			PR73A	3	RDQS73	T (LVDS)*	
-	-	-			GNDIO3	-			
W25	NC	-			PR72B	3	RDQ73	C	
W26	NC	-			PR72A	3	RDQ73	T	
U29	PR59B	3		C (LVDS)*	PR71B	3	RDQ73	C (LVDS)*	
V29	PR59A	3		T (LVDS)*	PR71A	3	RDQ73	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
V30	PR58B	3		C	PR70B	3	RDQ73	C	
U30	PR58A	3		T	PR70A	3	RDQ73	T	
W27	PR57B	3		C (LVDS)*	PR69B	3	RDQ73	C (LVDS)*	
W28	PR57A	3		T (LVDS)*	PR69A	3	RDQ73	T (LVDS)*	
V24	PR55B	3	RDQ52	C	PR67B	3	RDQ64	C	
V25	PR55A	3	RDQ52	T	PR67A	3	RDQ64	T	
GNDIO	GNDIO3	-			GNDIO3	-			
U28	PR54B	3	RDQ52	C (LVDS)*	PR66B	3	RDQ64	C (LVDS)*	
U27	PR54A	3	RDQ52	T (LVDS)*	PR66A	3	RDQ64	T (LVDS)*	
U23	PR53B	3	RDQ52	C	PR65B	3	RDQ64	C	
V23	PR53A	3	RDQ52	T	PR65A	3	RDQ64	T	
VCCIO	VCCIO3	3			VCCIO3	3			
V26	PR52B	3	RDQ52	C (LVDS)*	PR64B	3	RDQ64	C (LVDS)*	
U26	PR52A	3	RDQS52	T (LVDS)*	PR64A	3	RDQS64	T (LVDS)*	
U25	PR51B	3	RDQ52	C	PR63B	3	RDQ64	C	
GNDIO	GNDIO3	-			GNDIO3	-			
U24	PR51A	3	RDQ52	T	PR63A	3	RDQ64	T	
T30	PR50B	3	RDQ52	C (LVDS)*	PR62B	3	RDQ64	C (LVDS)*	
R30	PR50A	3	RDQ52	T (LVDS)*	PR62A	3	RDQ64	T (LVDS)*	
T23	PR49B	3	RDQ52	C	PR61B	3	RDQ64	C	
VCCIO	VCCIO3	3			VCCIO3	3			
T22	PR49A	3	RDQ52	T	PR61A	3	RDQ64	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF17	GND	-			GND	-			
AF25	GND	-			GND	-			
AF6	GND	-			GND	-			
AJ10	GND	-			GND	-			
AJ21	GND	-			GND	-			
AJ27	GND	-			GND	-			
AJ4	GND	-			GND	-			
AK1	GND	-			GND	-			
AK13	GND	-			GND	-			
AK18	GND	-			GND	-			
AK24	GND	-			GND	-			
AK30	GND	-			GND	-			
AK7	GND	-			GND	-			
B10	GND	-			GND	-			
B21	GND	-			GND	-			
B27	GND	-			GND	-			
B4	GND	-			GND	-			
D25	GND	-			GND	-			
D6	GND	-			GND	-			
E14	GND	-			GND	-			
E17	GND	-			GND	-			
F22	GND	-			GND	-			
F27	GND	-			GND	-			
F4	GND	-			GND	-			
F9	GND	-			GND	-			
G12	GND	-			GND	-			
G19	GND	-			GND	-			
J24	GND	-			GND	-			
J7	GND	-			GND	-			
K14	GND	-			GND	-			
K15	GND	-			GND	-			
K16	GND	-			GND	-			
K17	GND	-			GND	-			
K27	GND	-			GND	-			
K4	GND	-			GND	-			
L14	GND	-			GND	-			
L15	GND	-			GND	-			
L16	GND	-			GND	-			
L17	GND	-			GND	-			
M23	GND	-			GND	-			
M8	GND	-			GND	-			
N14	GND	-			GND	-			
N15	GND	-			GND	-			
N16	GND	-			GND	-			
N17	GND	-			GND	-			
N27	GND	-			GND	-			
N4	GND	-			GND	-			
P11	GND	-			GND	-			

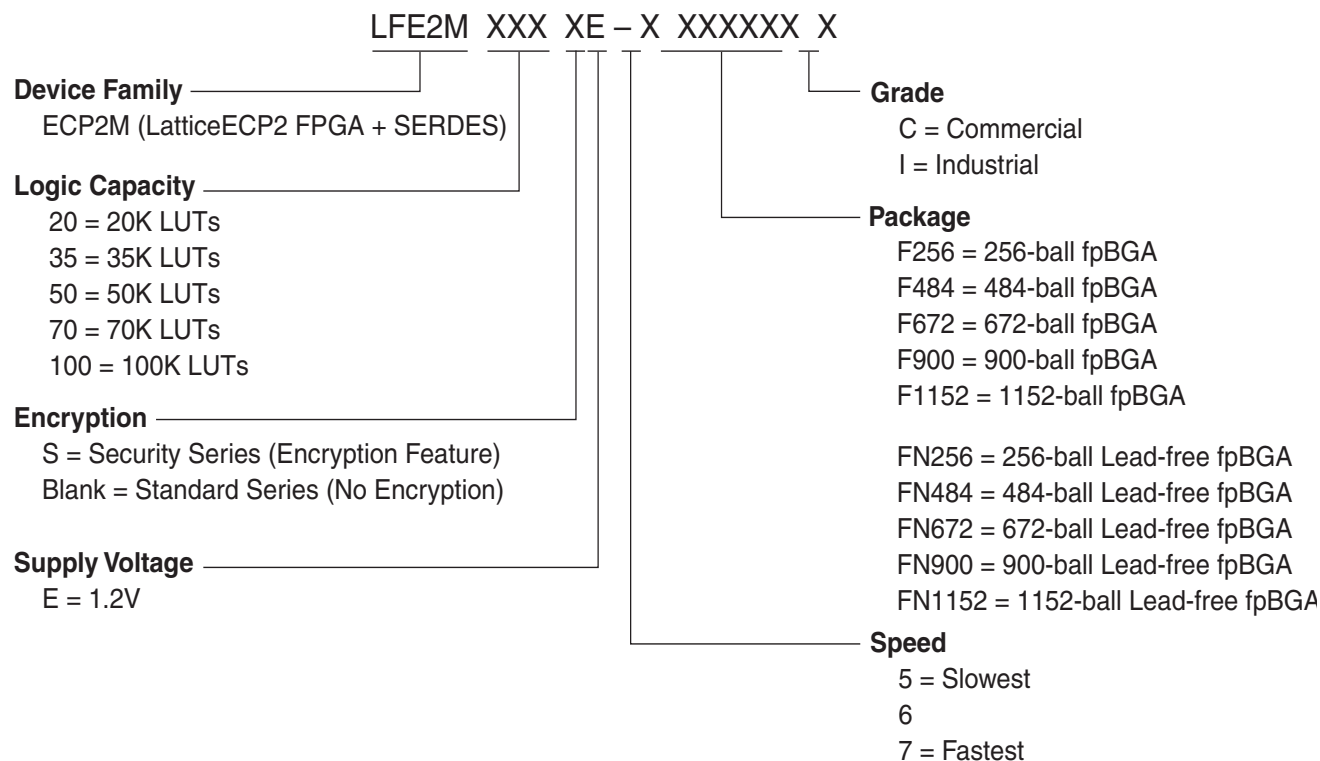
LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
VCCIO	VCCIO7	7			VCCIO7	7		
T6	PL44A	7	LDQ46	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*
R6	PL44B	7	LDQ46	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*
U9	PL45A	7	LDQ46	T	PL53A	7	LDQ54	T
T7	PL45B	7	LDQ46	C	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-			GNDIO7	-		
U5	PL46A	7	LDQS46	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*
U6	PL46B	7	LDQ46	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*
U7	PL47A	7	LDQ46	T	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7			VCCIO7	7		
V9	PL47B	7	LDQ46	C	PL55B	7	LDQ54	C
V11	PL48A	7	LDQ46	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*
V10	PL48B	7	LDQ46	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*
U4	PL49A	7	PCLKT7_0/LDQ46	T	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-			GNDIO7	-		
U3	PL49B	7	PCLKC7_0/LDQ46	C	PL57B	7	PCLKC7_0/LDQ54	C
U2	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
U1	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
V5	PL52A	6	VREF2_6/LDQ55	T	PL60A	6	VREF2_6/LDQ63	T
V6	PL52B	6	VREF1_6/LDQ55	C	PL60B	6	VREF1_6/LDQ63	C
V7	PL53A	6	LDQ55	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V8	PL53B	6	LDQ55	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*
V4	PL54A	6	LDQ55	T	PL62A	6	LDQ63	T
V3	PL54B	6	LDQ55	C	PL62B	6	LDQ63	C
V2	PL55A	6	LDQS55	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
V1	PL55B	6	LDQ55	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*
W7	PL56A	6	LDQ55	T	PL64A	6	LDQ63	T
W5	PL56B	6	LDQ55	C	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6			VCCIO6	6		
W2	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	PL65A	6	LLM4_SPLLT_IN_A/LDQ63	T (LVDS)*
W1	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*	PL65B	6	LLM4_SPLLC_IN_A/LDQ63	C (LVDS)*
Y6	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T	PL66A	6	LLM4_SPLLT_FB_A/LDQ63	T
W6	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C	PL66B	6	LLM4_SPLLC_FB_A/LDQ63	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL60A	6	LDQ64	T (LVDS)*	PL68A	6	LDQ72	T (LVDS)*
Y2	PL60B	6	LDQ64	C (LVDS)*	PL68B	6	LDQ72	C (LVDS)*
Y7	PL61A	6	LDQ64	T	PL69A	6	LDQ72	T
Y5	PL61B	6	LDQ64	C	PL69B	6	LDQ72	C
VCCIO	VCCIO6	6			VCCIO6	6		
W10	PL62A	6	LDQ64	T (LVDS)*	PL70A	6	LDQ72	T (LVDS)*
Y8	PL62B	6	LDQ64	C (LVDS)*	PL70B	6	LDQ72	C (LVDS)*
Y4	PL63A	6	LDQ64	T	PL71A	6	LDQ72	T
Y3	PL63B	6	LDQ64	C	PL71B	6	LDQ72	C
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL64A	6	LDQS64	T (LVDS)*	PL72A	6	LDQS72	T (LVDS)*
AA2	PL64B	6	LDQ64	C (LVDS)*	PL72B	6	LDQ72	C (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

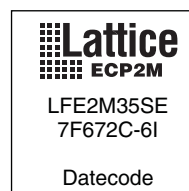
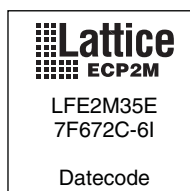
LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E23	PT82B	1		C	PT100B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
F23	PT82A	1		T	PT100A	1		T
F24	NC	-			PT99B	1		C
G23	NC	-			PT99A	1		T
D23	PT80B	1		C	PT98B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
D22	PT80A	1		T	PT98A	1		T
-	-	-			GNDIO1	-		
-	-	-			VCCIO1	1		
C21	PT79B	1		C	PT88B	1		C
D21	PT79A	1		T	PT88A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
B21	PT77B	1		C	PT86B	1		C
A21	PT77A	1		T	PT86A	1		T
F22	PT76B	1		C	PT85B	1		C
E22	PT76A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO1	-			-	-		
J22	NC	-			PT84B	1		C
G22	NC	-			PT84A	1		T
-	-	-			GNDIO1	-		
H22	PT72B	1		C	PT81B	1		C
K22	PT72A	1		T	PT81A	1		T
G21	PT71B	1		C	PT80B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
J21	PT71A	1		T	PT80A	1		T
H21	NC	-			PT79B	1		C
K21	NC	-			PT79A	1		T
D20	PT69B	1		C	PT78B	1		C
F20	PT69A	1		T	PT78A	1		T
C20	PT68B	1		C	PT77B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
E20	PT68A	1		T	PT77A	1		T
G20	PT67B	1		C	PT76B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
J20	PT67A	1		T	PT76A	1		T
A20	PT66B	1		C	PT75B	1		C
B20	PT66A	1		T	PT75A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A19	PT63B	1		C	PT72B	1		C
B19	PT63A	1		T	PT72A	1		T
K20	PT62B	1		C	PT71B	1		C
H20	PT62A	1		T	PT71A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
L19	NC	-			PT70B	1		C
L20	NC	-			PT70A	1		T
E19	PT60B	1		C	PT69B	1		C
C18	PT60A	1		T	PT69A	1		T

LatticeECP2M Part Number Description



Ordering Information

Note: LatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:



LatticeECP2M S-Series Devices, Lead-Free Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2M20SE-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2M20SE-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2M20SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2M20SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2M20SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2M35SE-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2M35SE-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	Com	35
LFE2M35SE-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2M35SE-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2M35SE-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2M35SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	35
LFE2M35SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	35
LFE2M35SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	Com	50
LFE2M50SE-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	Com	50
LFE2M50SE-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	Com	50
LFE2M50SE-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2M50SE-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2M50SE-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	Com	50
LFE2M50SE-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2M50SE-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2M50SE-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152C	436	1.2V	-5	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-6FN1152C	436	1.2V	-6	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-7FN1152C	436	1.2V	-7	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2M70SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2M70SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	70