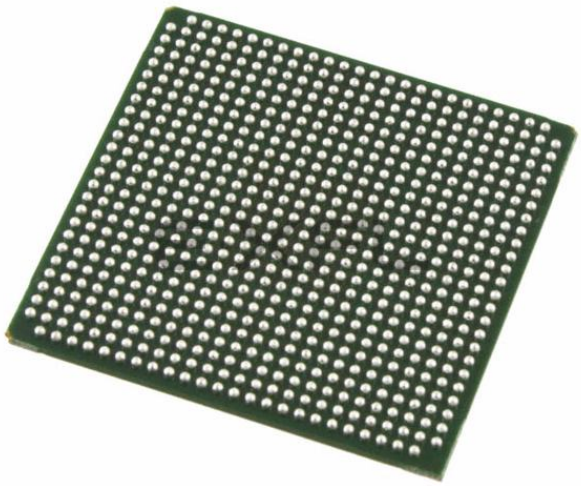
Lattice Semiconductor Corporation - LFE2-50SE-6FN672C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	396288
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-50se-6fn672c

Table 1-2. LatticeECP2M (Including "S-Series") Family Selection

Device	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL+SPLL+DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Packages and SERDES / I/O Combinations					
256-ball fpBGA (17 x 17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23 x 23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27 x 27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31 x 31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35 x 35 mm)				16 / 436	16 / 520

Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LVDS25E

The top and bottom sides of LatticeECP2/M devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

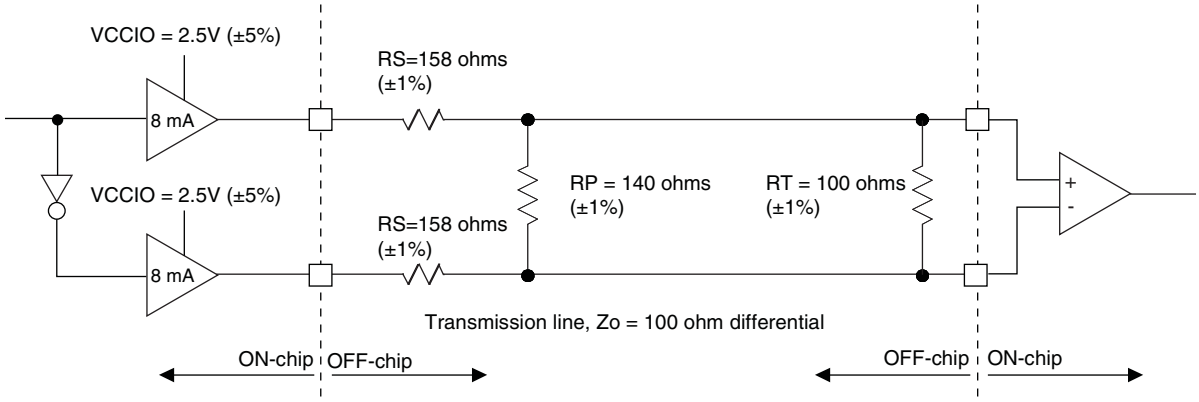

Table 3-2. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	158	Ω
R_P	Driver Parallel Resistor (+/-1%)	140	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

Available Device Resources by Package, LatticeECP2

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA
PLL/DLL	ECP2-6	4	—	—	—
	ECP2-12	4	4	—	—
	ECP2-20	4	4	4	—
	ECP2-35	—	4	4	—
	ECP2-50	—	6	6	—
	ECP2-70	—	—	8	8

Available Device Resources by Package, LatticeECP2M

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA	1152 fpBGA
PLL/DLL	ECP2M20	10	10	—	—	—
	ECP2M35	10	10	10	—	—
	ECP2M50	—	10	10	10	—
	ECP2M70	—	—	—	10	10
	ECP2M100	—	—	—	10	10

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
136	PT6B	0		C	PT16B	0		C
137	PT6A	0		T	PT16A	0		T
138	GND	-			GND	-		
139	VCCIO0	0			VCCIO0	0		
140	PT4B	0		C	PT6B	0		C
141	PT4A	0		T	PT6A	0		T
142	VCCAUX	-			VCCAUX	-		
143	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
144	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one-to-one connection with a package ball or pin.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
46	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*
47	PL30A	6	LDQ28		PL44A	6	LDQ42	
48	TCK	-			TCK	-		
49	TDI	-			TDI	-		
50	TDO	-			TDO	-		
51	VCCJ	-			VCCJ	-		
52	TMS	-			TMS	-		
53	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
54	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
55	VCCIO5	5			VCCIO5	5		
56	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
57	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
58	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
59	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
60	GND	-			GND	-		
61	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T
62	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C
63	VCCIO5	5			VCCIO5	5		
64	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T
65	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C
66	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T
67	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C
68	GND	-			GND	-		
69	PB20A	5	BDQ24	T	PB30A	5	BDQ33	T
70	VCCAUX	-			VCCAUX	-		
71	PB20B	5	BDQ24	C	PB30B	5	BDQ33	C
72	PB22A	5	BDQ24	T	PB32A	5	BDQ33	T
73	PB22B	5	BDQ24	C	PB32B	5	BDQ33	C
74	VCC	-			VCC	-		
75	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
76	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
77	GND	-			GND	-		
78	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
79	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
80	VCC	-			VCC	-		
81	GND	-			GND	-		
82	PB34A	4	BDQ33	T	PB42A	4	BDQS42	T
83	PB34B	4	BDQ33	C	PB42B	4	BDQ42	C
84	PB36A	4	BDQ33	T	PB44A	4	BDQ42	T
85	PB36B	4	BDQ33	C	PB44B	4	BDQ42	C
86	VCCAUX	-			VCCAUX	-		
87	PB40A	4	BDQ42	T	PB50A	4	BDQ51	T
88	PB40B	4	BDQ42	C	PB50B	4	BDQ51	C
89	GND	-			GND	-		
90	PB42A	4	BDQS42	T	PB52A	4	BDQ51	T
91	PB42B	4	BDQ42	C	PB52B	4	BDQ51	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
92	PB44A	4	BDQ42	T	PB54A	4	BDQ51	T
93	VCCIO4	4			VCCIO4	4		
94	PB44B	4	BDQ42	C	PB54B	4	BDQ51	C
95	PB48A	4	BDQ51	T	PB58A	4	BDQ60	T
96	PB48B	4	BDQ51	C	PB58B	4	BDQ60	C
97	VCC	-			VCC	-		
98	PB52A	4	BDQ51	T	PB60A	4	BDQS60	T
99	PB52B	4	BDQ51	C	PB60B	4	BDQ60	C
100	VCCIO4	4			VCCIO4	4		
101	PB54A	4	BDQ51		PB63A	4	BDQ60	
102	GND	-			GND	-		
103	PB55A	4	VREF2_4/BDQ51	T	PB64A	4	VREF2_4/BDQ60	T
104	PB55B	4	VREF1_4/BDQ51	C	PB64B	4	VREF1_4/BDQ60	C
105	CFG1	8			CFG1	8		
106	PROGRAMN	8			PROGRAMN	8		
107	CFG2	8			CFG2	8		
108	INITN	8			INITN	8		
109	CFG0	8			CFG0	8		
110	CCLK	8			CCLK	8		
111	DONE	8			DONE	8		
112	PR29A	8	D0/SPIFASTN		PR43A	8	D0/SPIFASTN	
113	VCCIO8	8			VCCIO8	8		
114	PR26A	8	D6		PR40A	8	D6	
115	GND	-			GND	-		
116	VCC	-			VCC	-		
117	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
118	VCCIO8	8			VCCIO8	8		
119	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
120	PR24B	8	DOUT/CSON	C	PR38B	8	DOUT/CSON	C
121	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
122	GND	-			GND	-		
123	VCCIO3	3			VCCIO3	3		
124	PR21A	3	RLM0_GPLLT_FB_A		PR31A	3	RLM0_GPLLT_FB_A/RDQ34	
125	VCCAUX	-			VCCAUX	-		
126	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
127	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
128	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
129	VCC	-			VCC	-		
130	PR18B	3	RLM0_GDLLC_FB_A	C	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
131	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
132	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
133	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
134	PR16B	3	VREF2_3	C	PR22B	3	VREF2_3/RDQ25	C
135	VCCIO3	3			VCCIO3	3		
136	PR16A	3	VREF1_3	T	PR22A	3	VREF1_3/RDQ25	T
137	PR15B	3	PCLKC3_0	C (LVDS)*	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W5	PL38B	6	LDQ42	C (LVDS)*	PL52B	6	LDQ56	C (LVDS)*
AC1	PL39A	6	LDQ42	T	PL53A	6	LDQ56	T
AD1	PL39B	6	LDQ42	C	PL53B	6	LDQ56	C
VCCIO	VCCIO6	6			VCCIO6	6		
Y6	PL40A	6	LDQ42	T (LVDS)*	PL54A	6	LDQ56	T (LVDS)*
Y5	PL40B	6	LDQ42	C (LVDS)*	PL54B	6	LDQ56	C (LVDS)*
AE2	PL41A	6	LDQ42	T	PL55A	6	LDQ56	T
AD2	PL41B	6	LDQ42	C	PL55B	6	LDQ56	C
GND	GNDIO6	-			GNDIO6	-		
AB3	PL42A	6	LDQS42	T (LVDS)*	PL56A	6	LDQS56	T (LVDS)*
AB2	PL42B	6	LDQ42	C (LVDS)*	PL56B	6	LDQ56	C (LVDS)*
W7	PL43A	6	LDQ42	T	PL57A	6	LDQ56	T
VCCIO	VCCIO6	6			VCCIO6	6		
W8	PL43B	6	LDQ42	C	PL57B	6	LDQ56	C
Y7	PL44A	6	LDQ42	T (LVDS)*	PL58A	6	LDQ56	T (LVDS)*
Y8	PL44B	6	LDQ42	C (LVDS)*	PL58B	6	LDQ56	C (LVDS)*
AC2	PL45A	6	LDQ42	T	PL59A	6	LDQ56	T
GND	GNDIO6	-			GNDIO6	-		
AD3	PL45B	6	LDQ42	C	PL59B	6	LDQ56	C
AC3	TCK	-			TCK	-		
AA8	TDI	-			TDI	-		
AB4	TMS	-			TMS	-		
AA5	TDO	-			TDO	-		
AB5	VCCJ	-			VCCJ	-		
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
GND	GNDIO5	-			GNDIO5	-		
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D4	PT7B	0		C	PT7B	0		C
D3	PT7A	0		T	PT7A	0		T
C2	PT6B	0		C	PT6B	0		C
C1	PT6A	0		T	PT6A	0		T
G8	PT5B	0		C	PT5B	0		C
GND	GNDIO0	-			GNDIO0	-		
G7	PT5A	0		T	PT5A	0		T
E7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT4A	0		T	PT4A	0		T
E6	PT3B	0		C	PT3B	0		C
E5	PT3A	0		T	PT3A	0		T
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
D11	VCCIO0	0			VCCIO0	0		
D6	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		
J12	VCCIO0	0			VCCIO0	0		
D16	VCCIO1	1			VCCIO1	1		
D21	VCCIO1	1			VCCIO1	1		
G18	VCCIO1	1			VCCIO1	1		
J15	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
F23	VCCIO2	2			VCCIO2	2		
J20	VCCIO2	2			VCCIO2	2		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
G10	VCCPLL	-			VCCPLL	-		
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
E7	VCCIO0	0			VCCIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
E10	VCCIO1	1			VCCIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
VCCIO	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
VCCIO	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
VCCIO	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
VCCIO	VCCIO8	8			VCCIO8	8		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A15	GND	-			GND	-		
A16	GND	-			GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
E18	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
D18	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			-	-		
F16	XRES	-			XRES	-		
C22	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A21	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B20	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C12	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
D1	PL2A	7	LDQ6	T (LVDS)*
E1	PL2B	7	LDQ6	C (LVDS)*
F1	PL3A	7	LDQ6	T
F2	PL3B	7	LDQ6	C
F5	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7		
G6	PL4B	7	LDQ6	C (LVDS)*
F4	PL5A	7	LDQ6	T
F3	PL5B	7	LDQ6	C
G1	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-		
G2	PL6B	7	LDQ6	C (LVDS)*
H1	PL7A	7	LDQ6	T
H2	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7		
H7	PL8A	7	LDQ6	T (LVDS)*
H6	PL8B	7	LDQ6	C (LVDS)*
G3	PL9A	7	VREF2_7/LDQ6	T
H3	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C
GNDIO	GNDIO7	-		
J3	PL13A	7		T (LVDS)*
J4	PL13B	7		C (LVDS)*
J7	PL14A	7		T
VCCIO	VCCIO7	7		
J6	PL14B	7		C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
K1	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*
K2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*
J5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T
K5	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C
VCCIO	VCCIO7	7		
K7	PL34A	7	LDQ36	T (LVDS)*
K6	PL34B	7	LDQ36	C (LVDS)*
L6	PL35A	7	LDQ36	T
L7	PL35B	7	LDQ36	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF23	PB64A	4	BDQ60	T	LRC_SQ_HDINP1	13		T
AD23	NC	-			LRC_SQ_VCCIB1	13		
AE23	PB66B	4	BDQ69	C	LRC_SQ_HDINN1	13		C
AD24	VCC	-			LRC_SQ_VCCRX1	13		
AF20	PB55A	4	BDQ51	T	LRC_SQ_HDOUTP1	13		T
AD20	NC	-			LRC_SQ_VCCOB1	13		
AE20	PB55B	4	BDQ51	C	LRC_SQ_HDOUTN1	13		C
AD21	VCC	-			LRC_SQ_VCCTX1	13		
AE21	PB63B	4	BDQ60	C	LRC_SQ_HDOUTN0	13		C
AF22	NC	-			LRC_SQ_VCCOB0	13		
AF21	PB62A	4	BDQ60	T	LRC_SQ_HDOUTP0	13		T
AD22	VCC	-			LRC_SQ_VCCTX0	13		
AE24	PB67B	4	BDQ69	C	LRC_SQ_HDINN0	13		C
AE25	NC	-			LRC_SQ_VCCIB0	13		
AF24	PB67A	4	BDQ69	T	LRC_SQ_HDINP0	13		T
AD25	VCC	-			LRC_SQ_VCCRX0	13		
AA21	CFG2	8			CFG2	8		
AA22	CFG1	8			CFG1	8		
AB23	CFG0	8			CFG0	8		
AC26	PROGRAMN	8			PROGRAMN	8		
AB24	CCLK	8			CCLK	8		
AA23	INITN	8			INITN	8		
AB25	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
Y19	PR68B	8	WRITEN***	C	WRITEN***	8		
Y21	PR68A	8	CS1N***	T	CS1N***	8		
AB26	PR67B	8	CSN***	C	CSN***	8		
Y22	PR67A	8	D0/SPIFASTN***	T	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8				8		
W19	PR66B	8	D1***	C	D1***	8		
Y20	PR66A	8	D2***	T	D2***	8		
W22	PR65B	8	D3***	C	D3***	8		
GNDIO	GNDIO8	-				-		
W18	PR65A	8	D4***	T	D4***	8		
Y23	PR64B	8	D5***	C	D5***	8		
AA24	PR64A	8	D6***	T	D6***	8		
W21	PR63B	8	D7/SPID0***	C	D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
V20	PR63A	8	DI/CSSPI0N***	T	DI/CSSPI0N***	8		
W23	PR62B	8	DOUT/CSON/CSSPI1N***	C	DOUT/CSON/ CSSPI1N***	8		
Y24	PR62A	8	BUSY/SISPI***	T	BUSY/SISPI***	8		
V19	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
V21	PR60B	3	RLM0_GDLLC_FB_A	C	PR65B	3	RLM0_GDLLC_FB_A	C
GNDIO	GNDIO3	-			GNDIO3	-		
U19	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T	PR65A	3	RLM0_GDLLT_FB_A	T
AA26	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*	PR64B	3	RLM0_GDLLC_IN_A	C*
Y26	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*	PR64A	3	RLM0_GDLLT_IN_A	T*
V23	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C	PR63B	3	RLM0_GPLLC_IN_A	C

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M26	PR27A	2	RDQS27	T (LVDS)*	PR37A	2	RDQS37	T (LVDS)*
L30	PR26B	2	RDQ27	C	PR36B	2	RDQ37	C
GNDIO	GNDIO2	-			GNDIO2	-		
L29	PR26A	2	RDQ27	T	PR36A	2	RDQ37	T
L28	PR25B	2	RDQ27	C (LVDS)*	PR35B	2	RDQ37	C (LVDS)*
L27	PR25A	2	RDQ27	T (LVDS)*	PR35A	2	RDQ37	T (LVDS)*
H29	PR24B	2	RDQ27	C	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2			VCCIO2	2		
G29	PR24A	2	RDQ27	T	PR34A	2	RDQ37	T
L22	PR23B	2	RDQ27	C (LVDS)*	PR33B	2	RDQ37	C (LVDS)*
M22	PR23A	2	RDQ27	T (LVDS)*	PR33A	2	RDQ37	T (LVDS)*
F30	PR21B	2		C	PR31B	2	RDQ28	C
GNDIO	GNDIO2	-			GNDIO2	-		
F29	PR21A	2		T	PR31A	2	RDQ28	T
-	-	-			-	-		
-	-	-			-	-		
E30	PR20B	2		C (LVDS)*	PR30B	2	RDQ28	C (LVDS)*
E29	PR20A	2		T (LVDS)*	PR30A	2	RDQ28	T (LVDS)*
VCCIO	VCCIO2	2			-	-		
L25	PR19B	2		C	PR29B	2	RDQ28	C
L26	PR19A	2		T	PR29A	2	RDQ28	T
-	-	-			VCCIO2	2		
H28	PR18B	2		C (LVDS)*	PR28B	2	RDQ28	C (LVDS)*
J28	PR18A	2		T (LVDS)*	PR28A	2	RDQS28	T (LVDS)*
G28	PR16B	2		C	PR27B	2	RDQ28	C
GNDIO	GNDIO2	-			GNDIO2	-		
G27	PR16A	2		T	PR27A	2	RDQ28	T
L24	NC	-			PR26B	2	RDQ28	C (LVDS)*
L23	NC	-			PR26A	2	RDQ28	T (LVDS)*
D30	NC	-			PR25B	2	RDQ28	C
-	-	-			VCCIO2	2		
D29	NC	-			PR25A	2	RDQ28	T
K24	NC	-			PR24B	2	RDQ28	C (LVDS)*
K25	NC	-			PR24A	2	RDQ28	T (LVDS)*
J27	NC	-			PR22B	2		C
-	-	-			GNDIO2	-		
K26	NC	-			PR22A	2		T
K23	PR15B	2		C (LVDS)*	PR21B	2		C (LVDS)*
K22	PR15A	2		T (LVDS)*	PR21A	2		T (LVDS)*
J22	PR14B	2		C	PR20B	2		C
VCCIO	VCCIO2	-			VCCIO2	2		
J23	PR14A	2		T	PR20A	2		T
-	-	-			GNDIO2	-		
-	-	-			-	-		
J26	NC	-			PR17B	2	RDQ15	C (LVDS)*
H26	NC	-			PR17A	2	RDQ15	T (LVDS)*
H27	NC	-			PR16B	2	RDQ15	C
G26	NC	-			PR16A	2	RDQ15	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
GNDIO	GNDIO2	-		
M27	PR47B	2	RDQ45	C (LVDS)*
M28	PR47A	2	RDQ45	T (LVDS)*
H30	PR46B	2	RDQ45	C
G30	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2		
M25	PR45B	2	RDQ45	C (LVDS)*
M26	PR45A	2	RDQS45	T (LVDS)*
L30	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-		
L29	PR44A	2	RDQ45	T
L28	PR43B	2	RDQ45	C (LVDS)*
L27	PR43A	2	RDQ45	T (LVDS)*
H29	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2		
G29	PR42A	2	RDQ45	T
L22	PR41B	2	RDQ45	C (LVDS)*
M22	PR41A	2	RDQ45	T (LVDS)*
F30	PR40B	2		C
GNDIO	GNDIO2	-		
F29	PR40A	2		T
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E30	PR34B	2	RDQ32	C (LVDS)*
E29	PR34A	2	RDQ32	T (LVDS)*
-	-	-		
L25	PR33B	2	RDQ32	C
L26	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2		
H28	PR32B	2	RDQ32	C (LVDS)*
J28	PR32A	2	RDQS32	T (LVDS)*
G28	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-		
G27	PR31A	2	RDQ32	T
L24	PR30B	2	RDQ32	C (LVDS)*
L23	PR30A	2	RDQ32	T (LVDS)*
D30	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2		
D29	PR29A	2	RDQ32	T
K24	PR28B	2	RDQ32	C (LVDS)*
K25	PR28A	2	RDQ32	T (LVDS)*
J27	PR26B	2	RDQ23	C
GNDIO	GNDIO2	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M10	VCCIO7	7		
M7	VCCIO7	7		
N10	VCCIO7	7		
N3	VCCIO7	7		
P10	VCCIO7	7		
R6	VCCIO7	7		
AA25	VCCIO8	8		
AD28	VCCIO8	8		
AA10	VCCAUX	-		
AA11	VCCAUX	-		
AA20	VCCAUX	-		
AA21	VCCAUX	-		
K10	VCCAUX	-		
K11	VCCAUX	-		
K20	VCCAUX	-		
K21	VCCAUX	-		
L10	VCCAUX	-		
L11	VCCAUX	-		
L20	VCCAUX	-		
L21	VCCAUX	-		
Y10	VCCAUX	-		
Y11	VCCAUX	-		
Y20	VCCAUX	-		
Y21	VCCAUX	-		
A1	GND	-		
A13	GND	-		
A18	GND	-		
A24	GND	-		
A30	GND	-		
A7	GND	-		
AA14	GND	-		
AA15	GND	-		
AA16	GND	-		
AA17	GND	-		
AA24	GND	-		
AA27	GND	-		
AA4	GND	-		
AB24	GND	-		
AB7	GND	-		
AD12	GND	-		
AD19	GND	-		
AD27	GND	-		
AE22	GND	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA8	PL65A	6	LDQ64	T	PL73A	6	LDQ72	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y9	PL65B	6	LDQ64	C	PL73B	6	LDQ72	C
AA6	PL66A	6	LDQ64	T (LVDS)*	PL74A	6	LDQ72	T (LVDS)*
AA7	PL66B	6	LDQ64	C (LVDS)*	PL74B	6	LDQ72	C (LVDS)*
AA4	PL67A	6	LDQ64	T	PL75A	6	LDQ72	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA3	PL67B	6	LDQ64	C	PL75B	6	LDQ72	C
AA9	PL69A	6	LDQ73	T (LVDS)*	PL77A	6	LDQ81	T (LVDS)*
AA10	PL69B	6	LDQ73	C (LVDS)*	PL77B	6	LDQ81	C (LVDS)*
AA5	PL70A	6	LDQ73	T	PL78A	6	LDQ81	T
AB6	PL70B	6	LDQ73	C	PL78B	6	LDQ81	C
AB1	PL71A	6	LDQ73	T (LVDS)*	PL79A	6	LDQ81	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AB2	PL71B	6	LDQ73	C (LVDS)*	PL79B	6	LDQ81	C (LVDS)*
AC8	PL72A	6	LDQ73	T	PL80A	6	LDQ81	T
AB10	PL72B	6	LDQ73	C	PL80B	6	LDQ81	C
AC1	PL73A	6	LDQS73	T (LVDS)*	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AC2	PL73B	6	LDQ73	C (LVDS)*	PL81B	6	LDQ81	C (LVDS)*
AB7	PL74A	6	LDQ73	T	PL82A	6	LDQ81	T
AB5	PL74B	6	LDQ73	C	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6			VCCIO6	6		
AC3	PL75A	6	LDQ73	T (LVDS)*	PL83A	6	LDQ81	T (LVDS)*
AC4	PL75B	6	LDQ73	C (LVDS)*	PL83B	6	LDQ81	C (LVDS)*
AC10	PL76A	6	LDQ73	T	PL84A	6	LDQ81	T
AC9	PL76B	6	LDQ73	C	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-			GNDIO6	-		
AC7	NC	-			PL86A	6	LDQ90	T (LVDS)*
AC5	NC	-			PL86B	6	LDQ90	C (LVDS)*
AC6	NC	-			PL87A	6	LDQ90	T
AD5	NC	-			PL87B	6	LDQ90	C
-	-	-			VCCIO6	6		
AD4	NC	-			PL88A	6	LDQ90	T (LVDS)*
AD3	NC	-			PL88B	6	LDQ90	C (LVDS)*
AD10	NC	-			PL89A	6	LDQ90	T
AD8	NC	-			PL89B	6	LDQ90	C
-	-	-			GNDIO6	-		
AD2	NC	-			PL90A	6	LDQS90	T (LVDS)*
AD1	NC	-			PL90B	6	LDQ90	C (LVDS)*
AD9	NC	-			PL91A	6	LDQ90	T
-	-	-			VCCIO6	6		
AC11	NC	-			PL91B	6	LDQ90	C
AD6	NC	-			PL92A	6	LDQ90	T (LVDS)*
AD7	NC	-			PL92B	6	LDQ90	C (LVDS)*
AE1	NC	-			PL93A	6	LDQ90	T
-	-	-			GNDIO6	-		
AE2	NC	-			PL93B	6	LDQ90	C
AF2	PL78A	6	LDQ82	T (LVDS)*	PL95A	6	LDQ99	T (LVDS)*

LatticeECP2 S-Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	Com	6
LFE2-6SE-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	Com	6
LFE2-6SE-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	Com	6
LFE2-6SE-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	Com	6
LFE2-6SE-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	Com	6
LFE2-6SE-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	Com	12
LFE2-12SE-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	Com	12
LFE2-12SE-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	Com	12
LFE2-12SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	12
LFE2-12SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	12
LFE2-12SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	12
LFE2-12SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	12
LFE2-12SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	12
LFE2-12SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	12
LFE2-12SE-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	Com	12
LFE2-12SE-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	Com	12
LFE2-12SE-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	20
LFE2-20SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	20
LFE2-20SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	20
LFE2-20SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2-20SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2-20SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	20
LFE2-20SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2-20SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2-20SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2-20SE-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	Com	20
LFE2-20SE-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	Com	20
LFE2-20SE-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100