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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	750
Number of Logic Elements/Cells	6000
Total RAM Bits	56320
Number of I/O	90
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-6se-5t144c

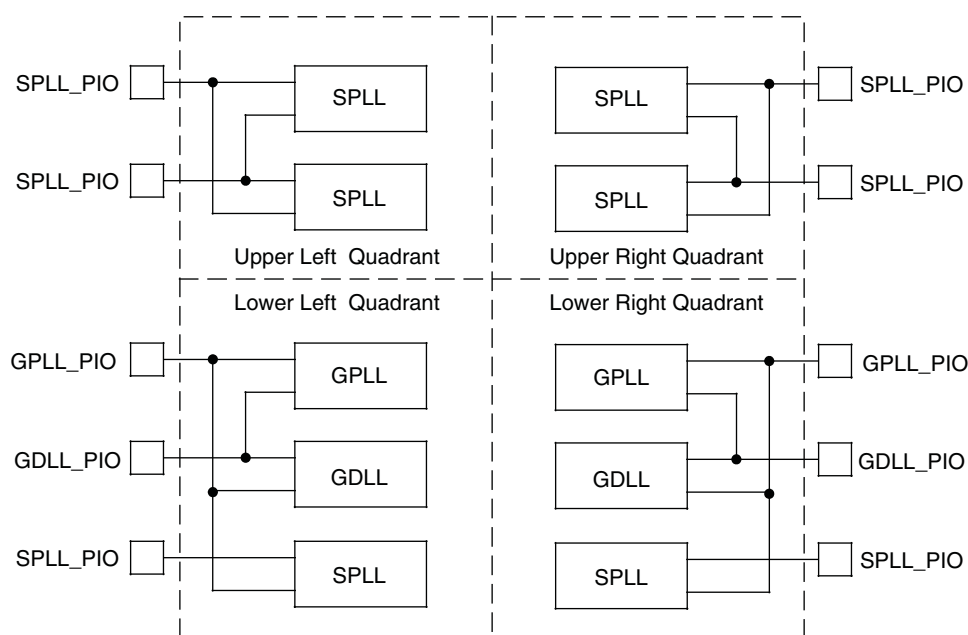
The DLLs in the LatticeECP2/M are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of additional technical documentation at the end of this data sheet.

GPLL/SPLL/GDLL PIO Input Pin Connections (LatticeECP2M Family Only)

All LatticeECP2M devices contain two GDLLs, two GPLLs and six SPLLs, arranged in quadrants as shown in Figure 2-8. In the LatticeECP2M devices GPLLs, SPLLs and GDLLs share their input pins. Figure 2-8 shows the sharing of SPLLs input pin connections in the upper two quadrants and the sharing of GDLL, GPLL and SPLL input pin connections in the lower two quadrants.

Figure 2-8. Sharing of PIO Pins by GPLL, SPLL and GDLL in LatticeECP2M Devices



Clock Dividers

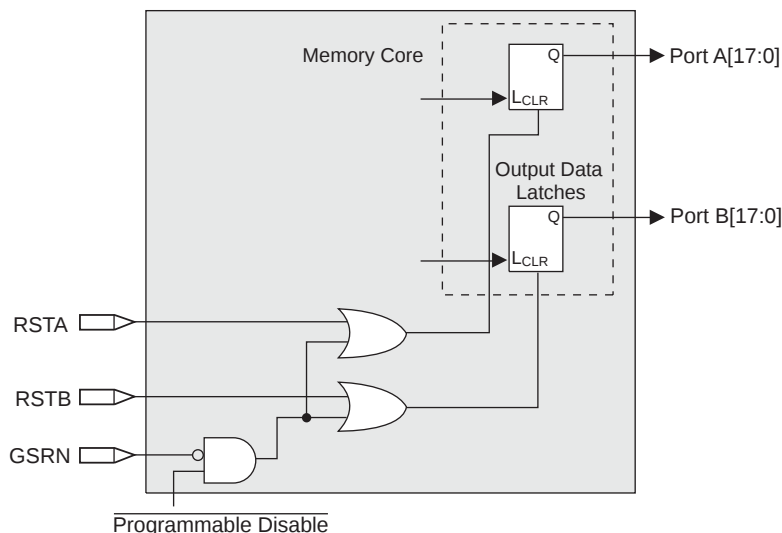
LatticeECP2/M devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 4$ or $\div 8$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL-DELA delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information about clock dividers, please see the list of additional technical documentation at the end of this data sheet. Figure 2-9 shows the clock divider connections.

2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

Figure 2-20. Memory Core Reset

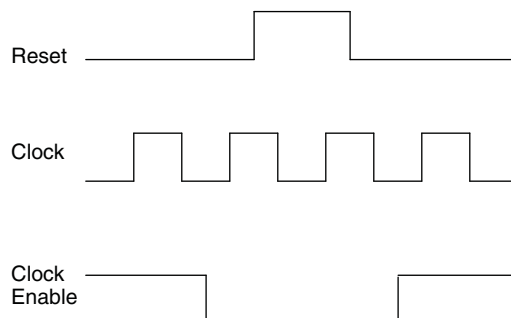


For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram

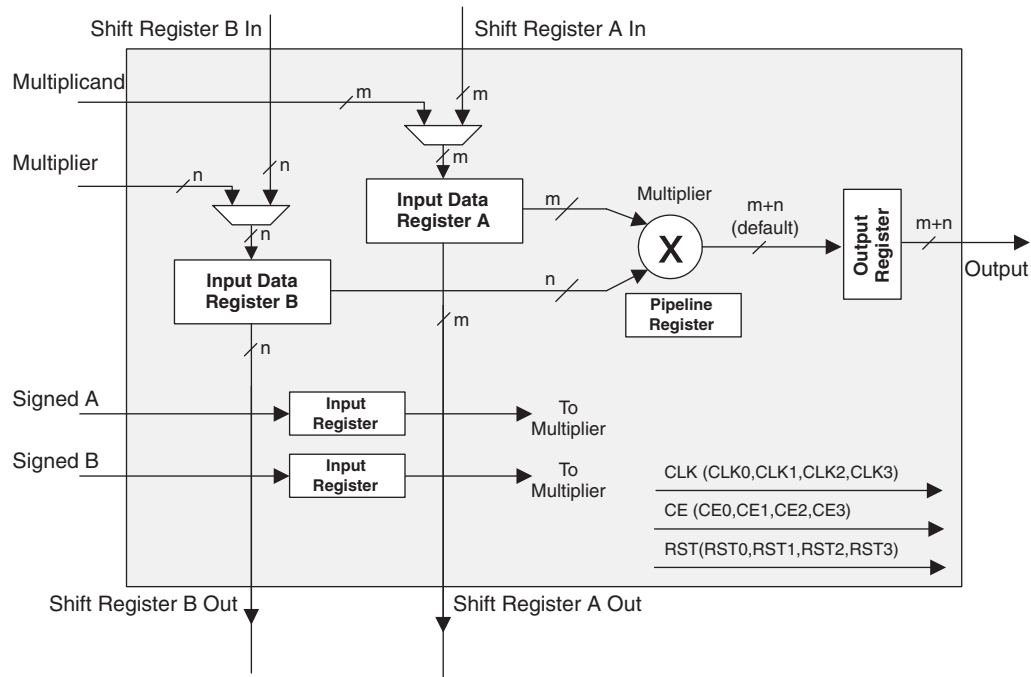


If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-23 shows the MULT sysDSP element.

Figure 2-23. MULT sysDSP Element



LatticeECP2M Initialization Supply Current^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ^{5, 6, 7}	Units
I_{CC}	Core Power Supply Current	ECP2M20	41	mA
		ECP2M35	107	mA
		ECP2M50	169	mA
		ECP2M70	254	mA
		ECP2M100	378	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	30	mA
		ECP2M35	30	mA
		ECP2M50	30	mA
		ECP2M70	30	mA
		ECP2M100	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. $T_J = 25^{\circ}\text{C}$, power supplies at nominal voltage.

6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

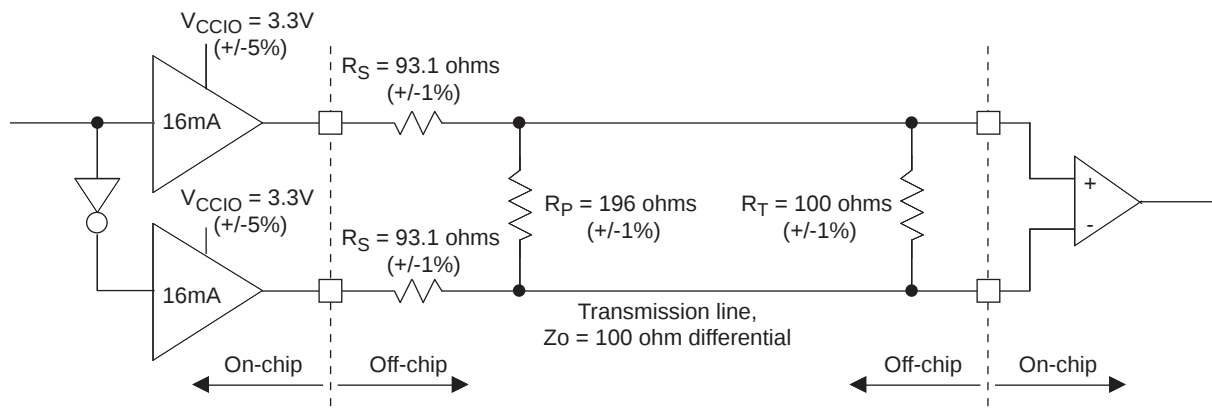


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LatticeECP2/M Family Timing Adders^{1, 2, 3}

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.04	-0.02	0.00	ns
BLVDS25	BLVDS	-0.04	-0.09	-0.15	ns
MLVDS	LVDS	-0.15	-0.15	-0.15	ns
RSDS	RSDS	-0.15	-0.15	-0.15	ns
LVPECL33	LVPECL	0.16	0.15	0.13	ns
HSTL18_I	HSTL_18 class I	0.01	-0.01	-0.04	ns
HSTL18_II	HSTL_18 class II	0.01	-0.01	-0.04	ns
HSTL18D_I	Differential HSTL 18 class I	0.01	-0.01	-0.04	ns
HSTL18D_II	Differential HSTL 18 class II	0.01	-0.01	-0.04	ns
HSTL15_I	HSTL_15 class I	0.01	-0.01	-0.04	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	-0.01	-0.04	ns
SSTL33_I	SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33_II	SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL33D_I	Differential SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33D_II	Differential SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL25_I	SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25_II	SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25D_II	Differential SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL18_I	SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18_II	SSTL_18 class II	-0.01	-0.04	-0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18D_II	Differential SSTL_18 class II	-0.01	-0.04	-0.07	ns
LVTTTL33	LVTTTL	-0.16	-0.16	-0.16	ns
LVC MOS33	LVC MOS 3.3	-0.08	-0.12	-0.16	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	-0.16	-0.17	-0.17	ns
LVC MOS15	LVC MOS 1.5	-0.14	-0.14	-0.14	ns
LVC MOS12	LVC MOS 1.2	-0.04	-0.01	0.01	ns
PCI33	PCI	-0.08	-0.12	-0.16	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁴	0.25	0.19	0.13	ns
LVDS25	LVDS 2.5	0.10	0.13	0.17	ns
BLVDS25	BLVDS 2.5	0.00	-0.01	-0.03	ns
MLVDS	MLVDS 2.5 ⁴	0.00	-0.01	-0.03	ns
RSDS	RSDS 2.5 ⁴	0.25	0.19	0.13	ns
LVPECL33	LVPECL 3.3 ⁴	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18_II	HSTL_18 class II	-0.30	-0.34	-0.37	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.34	-0.37	ns

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
91	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	
92	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	
93	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
94	VCC	-			VCC	-			
95	GND	-			GND	-			
96	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	
97	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	
98	PR16B	3	VREF2_3	C	PR16B	3	VREF2_3	C	
99	PR16A	3	VREF1_3	T	PR16A	3	VREF1_3	T	
100	PR15B	3	PCLKC3_0	C (LVDS)*	PR15B	3	PCLKC3_0	C (LVDS)*	
101	PR15A	3	PCLKT3_0	T (LVDS)*	PR15A	3	PCLKT3_0	T (LVDS)*	
102	VCC	-			VCC	-			
103	PR13B	2	PCLKC2_0/RDQ10	C	PR13B	2	PCLKC2_0/RDQ10	C	
104	PR13A	2	PCLKT2_0/RDQ10	T	PR13A	2	PCLKT2_0/RDQ10	T	
105	GND	-			GND	-			
106	VCCIO2	2			VCCIO2	2			
107	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
108	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
109	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C	
110	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T	
111	PT26B	1		C	PT54B	1		C	
112	PT26A	1		T	PT54A	1		T	
113	PT24B	1		C	PT52B	1		C	
114	PT24A	1		T	PT52A	1		T	
115	PT22B	1		C	PT50B	1		C	
116	PT22A	1		T	PT50A	1		T	
117	VCCIO1	1			VCCIO1	1			
118	PT20B	1		C	PT48B	1		C	
119	PT20A	1		T	PT48A	1		T	
120	GND	-			GND	-			
121	PT18B	1		C	PT44B	1		C	
122	PT18A	1		T	PT44A	1		T	
123	PT16A	1			PT40B	1		C	
124	NC	1			PT40A	1		T	
125	PT14B	1		C	PT34B	1		C	
126	PT14A	1		T	PT34A	1		T	
127	NC	1			NC	1			
128	VCC	-			VCC	-			
129	PT12B	1	PCLKC1_0	C	PT30B	1	PCLKC1_0	C	
130	PT12A	1	PCLKT1_0	T	PT30A	1	PCLKT1_0	T	
131	PT10B	0	PCLKC0_0	C	PT28B	0	PCLKC0_0	C	
132	XRES	0			XRES	0			
133	GND	-			GND	-			
134	PT10A	0	PCLKT0_0	T	PT28A	0	PCLKT0_0	T	
135	VCC	-			VCC	-			

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
184	GND	-			GND	-			
185	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T	
186	PT26B	0		C	PT36B	0		C	
187	PT26A	0		T	PT36A	0		T	
188	VCC	-			VCC	-			
189	PT20B	0		C	PT30B	0		C	
190	VCCAUX	-			VCCAUX	-			
191	PT20A	0		T	PT30A	0		T	
192	GND	-			GND	-			
193	PT18B	0		C	PT26B	0		C	
194	PT18A	0		T	PT26A	0		T	
195	VCCIO0	0			VCCIO0	0			
196	PT16B	0		C	PT20B	0		C	
197	PT16A	0		T	PT20A	0		T	
198	VCC	-			VCC	-			
199	PT12B	0		C	PT12B	0		C	
200	PT12A	0		T	PT12A	0		T	
201	GND	-			GND	-			
202	PT8B	0		C	PT8B	0		C	
203	PT8A	0		T	PT8A	0		T	
204	PT6B	0		C	PT6B	0		C	
205	PT6A	0		T	PT6A	0		T	
206	VCCIO0	0			VCCIO0	0			
207	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
208	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
Y21	PB64A	4	VREF2_4/BDQ60	T	PB73A	4	VREF2_4/BDQ69	T	
AB23	PB64B	4	VREF1_4/BDQ60	C	PB73B	4	VREF1_4/BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AD24	CFG2	8			CFG2	8			
W20	CFG1	8			CFG1	8			
AC24	CFG0	8			CFG0	8			
V19	PROGRAMN	8			PROGRAMN	8			
AA22	CCLK	8			CCLK	8			
AB24	INITN	8			INITN	8			
AD25	DONE	8			DONE	8			
GND	GNDIO8	-			GNDIO8	-			
W21	PR44B	8	WRITEN	C	PR58B	8	WRITEN	C	
Y22	PR44A	8	CS1N	T	PR58A	8	CS1N	T	
AC25	PR43B	8	CSN	C	PR57B	8	CSN	C	
AB25	PR43A	8	D0/SPIFASTN	T	PR57A	8	D0/SPIFASTN	T	
VCCIO	VCCIO8	8			VCCIO8	8			
AD26	PR42B	8	D1	C	PR56B	8	D1	C	
AC26	PR42A	8	D2	T	PR56A	8	D2	T	
Y23	PR41B	8	D3	C	PR55B	8	D3	C	
GND	GNDIO8	-			GNDIO8	-			
W22	PR41A	8	D4	T	PR55A	8	D4	T	
AA25	PR40B	8	D5	C	PR54B	8	D5	C	
AB26	PR40A	8	D6	T	PR54A	8	D6	T	
W23	PR39B	8	D7/SPID0	C	PR53B	8	D7/SPID0	C	
VCCIO	VCCIO8	8			VCCIO8	8			
V22	PR39A	8	DI/CSSPI0N	T	PR53A	8	DI/CSSPI0N	T	
Y24	PR38B	8	DOU/CSON	C	PR52B	8	DOU/CSON	C	
Y25	PR38A	8	BUSY/SISPI	T	PR52A	8	BUSY/SISPI	T	
W24	PR37B	3	RDQ34	C	PR51B	3	RDQ48	C	
GND	GNDIO3	-			GNDIO3	-			
V23	PR37A	3	RDQ34	T	PR51A	3	RDQ48	T	
AA26	PR36B	3	RDQ34	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*	
Y26	PR36A	3	RDQ34	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*	
U21	PR35B	3	RDQ34	C	PR49B	3	RDQ48	C	
VCCIO	VCCIO3	3			VCCIO3	3			
U19	PR35A	3	RDQ34	T	PR49A	3	RDQ48	T	
W25	PR34B	3	RDQ34	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*	
W26	PR34A	3	RDQS34	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
V24	PR33B	3	RDQ34	C	PR47B	3	RDQ48	C	
V25	PR33A	3	RDQ34	T	PR47A	3	RDQ48	T	
V26	PR32B	3	RDQ34	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*	
U26	PR32A	3	RDQ34	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
U22	PR31B	3	RLM0_GPLL_C_FB_A/RDQ34	C	PR45B	3	RLM0_GPLL_C_FB_A/RDQ48	C	
U23	PR31A	3	RLM0_GPLL_T_FB_A/RDQ34	T	PR45A	3	RLM0_GPLL_T_FB_A/RDQ48	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
AB19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AE19	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AA17	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	
AF18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T	
AF19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T	
W17	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C	
Y19	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
Y17	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
AF20	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
AA20	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
W18	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
AD20	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
GND	GNDIO4	-			GNDIO4	-			
AE21	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
AF21	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
AF22	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T	
AD22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C	
AF23	PB75A	4	BDQ78	T	PB93A	4	BDQ96	T	
AE23	PB75B	4	BDQ78	C	PB93B	4	BDQ96	C	
AD23	PB76A	4	BDQ78	T	PB94A	4	BDQ96	T	
AC23	PB76B	4	BDQ78	C	PB94B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T	
AC20	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T	
AC22	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C	
W19	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T	
AA21	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C	
AF24	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T	
AE24	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T	
AB22	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO1	-			GNDIO1	-		
C15	PT54B	1		C	PT63B	1		C
A15	PT54A	1		T	PT63A	1		T
A13	PT53B	1		C	PT62B	1		C
B13	PT53A	1		T	PT62A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
H17	PT52B	1		C	PT61B	1		C
H15	PT52A	1		T	PT61A	1		T
D13	PT51B	1		C	PT60B	1		C
C14	PT51A	1		T	PT60A	1		T
GND	GNDIO1	-			GNDIO1	-		
G14	PT50B	1		C	PT59B	1		C
E14	PT50A	1		T	PT59A	1		T
A12	PT49B	1		C	PT58B	1		C
B12	PT49A	1		T	PT58A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
F14	PT48B	1	PCLKC1_0	C	PT57B	1	PCLKC1_0	C
D14	PT48A	1	PCLKT1_0	T	PT57A	1	PCLKT1_0	T
H16	XRES	1			XRES	1		
H14	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C
GND	GNDIO0	-			GNDIO0	-		
H13	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T
A11	PT45B	0		C	PT54B	0		C
B11	PT45A	0		T	PT54A	0		T
C13	PT44B	0		C	PT53B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
E13	PT44A	0		T	PT53A	0		T
D12	PT43B	0		C	PT52B	0		C
F13	PT43A	0		T	PT52A	0		T
A10	PT42B	0		C	PT51B	0		C
B10	PT42A	0		T	PT51A	0		T
C12	PT41B	0		C	PT50B	0		C
GND	GNDIO0	-			GNDIO0	-		
C10	PT41A	0		T	PT50A	0		T
G13	PT40B	0		C	PT49B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
H12	PT40A	0		T	PT49A	0		T
A9	PT39B	0		C	PT48B	0		C
B9	PT39A	0		T	PT48A	0		T
E12	PT38B	0		C	PT47B	0		C
G12	PT38A	0		T	PT47A	0		T
A8	PT37B	0		C	PT46B	0		C
B8	PT37A	0		T	PT46A	0		T
GND	GNDIO0	-			GNDIO0	-		
E11	PT36B	0		C	PT45B	0		C
C9	PT36A	0		T	PT45A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W7	PL72B	6	LDQ71	C
W4	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*
W3	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*
W6	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T
GND	GNDIO6	-		
W8	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C
Y8	LLM0_PLLCAP	6		
Y1	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*
Y2	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*
Y5	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T
Y6	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C
Y4	PL78A	6	LDQ80	T (LVDS)*
VCCIO	VCCIO6	6		
Y3	PL78B	6	LDQ80	C (LVDS)*
AA6	PL79A	6	LDQ80	T
AA8	PL79B	6	LDQ80	C
AA2	PL80A	6	LDQS80	T (LVDS)*
GND	GNDIO6	-		
AA1	PL80B	6	LDQ80	C (LVDS)*
AA7	PL81A	6	LDQ80	T
AA5	PL81B	6	LDQ80	C
VCCIO	VCCIO6	6		
AA4	PL82A	6	LDQ80	T (LVDS)*
AA3	PL82B	6	LDQ80	C (LVDS)*
AB7	PL83A	6	LDQ80	T
AB5	PL83B	6	LDQ80	C
GND	GNDIO6	-		
AB2	PL84A	6	LDQ88	T (LVDS)*
AB1	PL84B	6	LDQ88	C (LVDS)*
AB8	PL85A	6	LDQ88	T
AB6	PL85B	6	LDQ88	C
VCCIO	VCCIO6	6		
AB4	PL86A	6	LDQ88	T (LVDS)*
AB3	PL86B	6	LDQ88	C (LVDS)*
AC7	PL87A	6	LDQ88	T
AC5	PL87B	6	LDQ88	C
GND	GNDIO6	-		
AC2	PL88A	6	LDQS88	T (LVDS)*
AC1	PL88B	6	LDQ88	C (LVDS)*
AC6	PL89A	6	LDQ88	T
VCCIO	VCCIO6	6		
AD6	PL89B	6	LDQ88	C
AD1	PL90A	6	LDQ88	T (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AD18	PB66A	4	BDQ69	T
AF18	PB66B	4	BDQ69	C
AC18	PB67A	4	BDQ69	T
AE18	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4		
AG19	PB68A	4	BDQ69	T
AH19	PB68B	4	BDQ69	C
GND	GNDIO4	-		
AE19	PB69A	4	BDQS69	T
AF19	PB69B	4	BDQ69	C
AC19	PB70A	4	BDQ69	T
AD19	PB70B	4	BDQ69	C
AJ19	PB71A	4	BDQ69	T
AK19	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4		
AF20	PB72A	4	BDQ69	T
AH20	PB72B	4	BDQ69	C
AE20	PB73A	4	BDQ69	T
AG20	PB73B	4	BDQ69	C
GND	GNDIO4	-		
AD20	PB74A	4	BDQ78	T
AC20	PB74B	4	BDQ78	C
AH21	PB75A	4	BDQ78	T
AF21	PB75B	4	BDQ78	C
AJ20	PB76A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK20	PB76B	4	BDQ78	C
AG21	PB77A	4	BDQ78	T
AE21	PB77B	4	BDQ78	C
AD21	PB78A	4	BDQS78	T
GND	GNDIO4	-		
AC21	PB78B	4	BDQ78	C
AD22	PB79A	4	BDQ78	T
AB21	PB79B	4	BDQ78	C
AJ21	PB80A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK21	PB80B	4	BDQ78	C
GND	GNDIO4	-		
VCCIO	VCCIO4	4		
AJ25	PB87A	4	BDQS87***	T
AK24	PB87B	4	BDQ87	C
AJ24	PB88A	4	BDQ87	T
AK25	PB88B	4	BDQ87	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K28	PR25A	2	RDQ29	T (LVDS)*
J24	PR24B	2	RDQ21	C
J26	PR24A	2	RDQ21	T
GND	GNDIO2	-		
K29	PR23B	2	RDQ21	C (LVDS)*
K30	PR23A	2	RDQ21	T (LVDS)*
J23	PR22B	2	RDQ21	C
J25	PR22A	2	RDQ21	T
VCCIO	VCCIO2	99		
J27	PR21B	2	RDQ21	C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2	RDQ21	C
GND	GNDIO2	-		
H24	PR20A	2	RDQ21	T
J29	PR19B	2	RDQ21	C (LVDS)*
J30	PR19A	2	RDQ21	T (LVDS)*
H25	PR18B	2	RDQ21	C
VCCIO	VCCIO2	2		
H23	PR18A	2	RDQ21	T
G27	PR15B	2	RUM1_SPLLC_FB_A/RDQ12	C
GND	GNDIO2	-		
H27	PR15A	2	RUM1_SPLLT_FB_A/RDQ12	T
G29	PR14B	2	RUM1_SPLLC_IN_A/RDQ12	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A/RDQ12	T (LVDS)*
VCCIO	VCCIO2	2		
GND	GNDIO2	-		
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
VCCIO	VCCIO2	2		
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO2	-		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
VCCIO	VCCIO2	2		
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO1	-		
C25	PT99B	1		C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
W17	PB65A	4	BDQ69	T	PB56A	4	BDQ60	T	
AA19	PB65B	4	BDQ69	C	PB56B	4	BDQ60	C	
AC15	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T	
Y18	PB68B	4	BDQ69	C	PB57B	4	BDQ60	C	
AB15	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T	
AC16	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AA17	PB60A	4	BDQS60****	T	PB59A	4	BDQ60	T	
AB16	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA15	PB51A	4	BDQS51****	T	PB60A	4	BDQS60	T	
W16	PB59B	4	BDQ60	C	PB60B	4	BDQ60	C	
Y15	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AC17	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
AA18	PB61A	4	BDQ60	T	PB62A	4	BDQ60	T	
Y17	PB61B	4	BDQ60	C	PB62B	4	BDQ60	C	
-	-	-			VCCIO4	4			
GNDIO	GNDIO4	-			-	-			
W15	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
AB17	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
VCCIO	VCCIO4	4			VCCIO4	4			
V17	PB73A	4	BDQ69	T	PB72A	4	BDQ69	T	
AA20	PB73B	4	BDQ69	C	PB72B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AD13	VCC	-			LRC_SQ_VCCR3	13			
AF14	PB47A	4	BDQ51	T	LRC_SQ_HDINP3	13		T	
AE13	NC	-			LRC_SQ_VCCIB3	13			
AE14	PB41A	4	VREF2_4/BDQ42	T	LRC_SQ_HDINN3	13		C	
AD16	VCC	-			LRC_SQ_VCCTX3	13			
AF17	PB51B	4	BDQ51	C	LRC_SQ_HDOUPT3	13		T	
AF16	NC	-			LRC_SQ_VCCOB3	13			
AE17	PB50A	4	BDQ51	T	LRC_SQ_HDOUPTN3	13		C	
AD17	VCC	-			LRC_SQ_VCCTX2	13			
AE18	PB53B	4	BDQ51	C	LRC_SQ_HDOUPTN2	13		C	
AD18	NC	-			LRC_SQ_VCCOB2	13			
AF18	PB53A	4	BDQ51	T	LRC_SQ_HDOUPT2	13		T	
AD14	VCC	-			LRC_SQ_VCCR2	13			
AE15	PB48B	4	BDQ51	C	LRC_SQ_HDINN2	13		C	
AD15	NC	-			LRC_SQ_VCCIB2	13			
AF15	PB47B	4	BDQ51	C	LRC_SQ_HDINP2	13		T	
AD19	VCC	-			LRC_SQ_VCCP	13			
AC19	PB57B	4	BDQ60	C	LRC_SQ_REFCLKP	13		T	
AB19	PB59A	4	BDQ60	T	LRC_SQ_REFCLKN	13		C	
AE19	VCCAUX	-			LRC_SQ_VCCAUX33	13			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A12	PT35B	0		C	PT44B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
A11	PT35A	0		T	PT44A	0		T	
D12	PT34B	0		C	PT43B	0		C	
H16	PT34A	0		T	PT43A	0		T	
H18	PT33B	0		C	PT42B	0		C	
H15	PT33A	0		T	PT42A	0		T	
A10	PT32B	0		C	PT41B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
B10	PT32A	0		T	PT41A	0		T	
D11	PT31B	0		C	PT40B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
G14	PT31A	0		T	PT40A	0		T	
E11	PT30B	0		C	PT39B	0		C	
F13	PT30A	0		T	PT39A	0		T	
D10	PT29B	0		C	PT38B	0		C	
H14	PT29A	0		T	PT38A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
A9	PT24B	0		C	PT24B	0		C	
C10	PT23B	0		C	PT23B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E8	PT23A	0		T	PT23A	0		T	
B9	PT22B	0		C	PT22B	0		C	
A8	PT22A	0		T	PT22A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F12	PT21B	0		C	PT21B	0		C	
E10	PT21A	0		T	PT21A	0		T	
G13	PT20B	0		C	PT20B	0		C	
C9	PT20A	0		T	PT20A	0		T	
B8	PT19B	0		C	PT19B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
A7	PT19A	0		T	PT19A	0		T	
D9	PT18B	0		C	PT18B	0		C	
H13	PT18A	0		T	PT18A	0		T	
D6	PT17B	0		C	PT17B	0		C	
C7	PT17A	0		T	PT17A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
C8	PT16B	0		C	PT16B	0		C	
G12	PT16A	0		T	PT16A	0		T	
D8	PT15B	0		C	PT15B	0		C	
H12	PT15A	0		T	PT15A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
A6	PT14B	0		C	PT14B	0		C	
A5	PT14A	0		T	PT14A	0		T	
A4	PT13B	0		C	PT13B	0		C	
A3	PT13A	0		T	PT13A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L13	VCC	-			VCC	-			
L18	VCC	-			VCC	-			
L19	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M13	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
M17	VCC	-			VCC	-			
M18	VCC	-			VCC	-			
M19	VCC	-			VCC	-			
M20	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N12	VCC	-			VCC	-			
N19	VCC	-			VCC	-			
N20	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P19	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R19	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T19	VCC	-			VCC	-			
U12	VCC	-			VCC	-			
U19	VCC	-			VCC	-			
V11	VCC	-			VCC	-			
V12	VCC	-			VCC	-			
V19	VCC	-			VCC	-			
V20	VCC	-			VCC	-			
W11	VCC	-			VCC	-			
W12	VCC	-			VCC	-			
W13	VCC	-			VCC	-			
W14	VCC	-			VCC	-			
W15	VCC	-			VCC	-			
W16	VCC	-			VCC	-			
W17	VCC	-			VCC	-			
W18	VCC	-			VCC	-			
W19	VCC	-			VCC	-			
W20	VCC	-			VCC	-			
Y12	VCC	-			VCC	-			
Y13	VCC	-			VCC	-			
Y18	VCC	-			VCC	-			
Y19	VCC	-			VCC	-			
D14	VCCIO0	0			VCCIO0	0			
E6	VCCIO0	0			VCCIO0	0			
E9	VCCIO0	0			VCCIO0	0			
F12	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB16	GND	-			GND	-		
AB17	GND	-			GND	-		
AB18	GND	-			GND	-		
AB19	GND	-			GND	-		
AB26	GND	-			GND	-		
AB31	GND	-			GND	-		
AB4	GND	-			GND	-		
AB9	GND	-			GND	-		
AC16	GND	-			GND	-		
AC17	GND	-			GND	-		
AC18	GND	-			GND	-		
AC19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE27	GND	-			GND	-		
AE31	GND	-			GND	-		
AE4	GND	-			GND	-		
AE8	GND	-			GND	-		
AF12	GND	-			GND	-		
AF16	GND	-			GND	-		
AF19	GND	-			GND	-		
AF23	GND	-			GND	-		
AG31	GND	-			GND	-		
AH31	GND	-			GND	-		
AH4	GND	-			GND	-		
AJ14	GND	-			GND	-		
AJ21	GND	-			GND	-		
AK27	GND	-			GND	-		
AK8	GND	-			GND	-		
AL10	GND	-			GND	-		
AL16	GND	-			GND	-		
AL19	GND	-			GND	-		
AL2	GND	-			GND	-		
AL25	GND	-			GND	-		
AL33	GND	-			GND	-		
AP1	GND	-			GND	-		
AP10	GND	-			GND	-		
AP13	GND	-			GND	-		
AP22	GND	-			GND	-		
AP25	GND	-			GND	-		
AP34	GND	-			GND	-		
D10	GND	-			GND	-		
D16	GND	-			GND	-		
D19	GND	-			GND	-		
D2	GND	-			GND	-		
D25	GND	-			GND	-		
D33	GND	-			GND	-		
E27	GND	-			GND	-		
E8	GND	-			GND	-		
F14	GND	-			GND	-		

LatticeECP2 S-Series Devices, Lead-Free Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	Com	6
LFE2-6SE-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	Com	6
LFE2-6SE-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	Com	6
LFE2-6SE-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	Com	6
LFE2-6SE-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	Com	6
LFE2-6SE-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	Com	12
LFE2-12SE-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	Com	12
LFE2-12SE-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	Com	12
LFE2-12SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	12
LFE2-12SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	12
LFE2-12SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	12
LFE2-12SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	12
LFE2-12SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	12
LFE2-12SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	12
LFE2-12SE-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	Com	12
LFE2-12SE-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	Com	12
LFE2-12SE-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	20
LFE2-20SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	20
LFE2-20SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	20
LFE2-20SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2-20SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2-20SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	20
LFE2-20SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2-20SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2-20SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2-20SE-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	Com	20
LFE2-20SE-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	Com	20
LFE2-20SE-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	Com	20