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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	750
Number of Logic Elements/Cells	6000
Total RAM Bits	56320
Number of I/O	90
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-6se-5tn144c

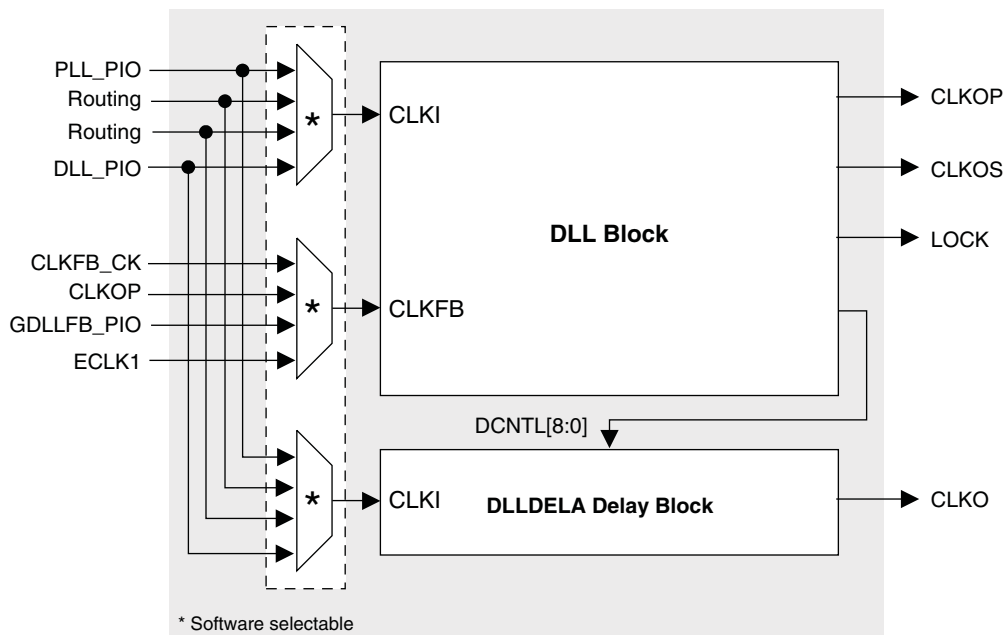
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-7. DLLDELA Delay Block

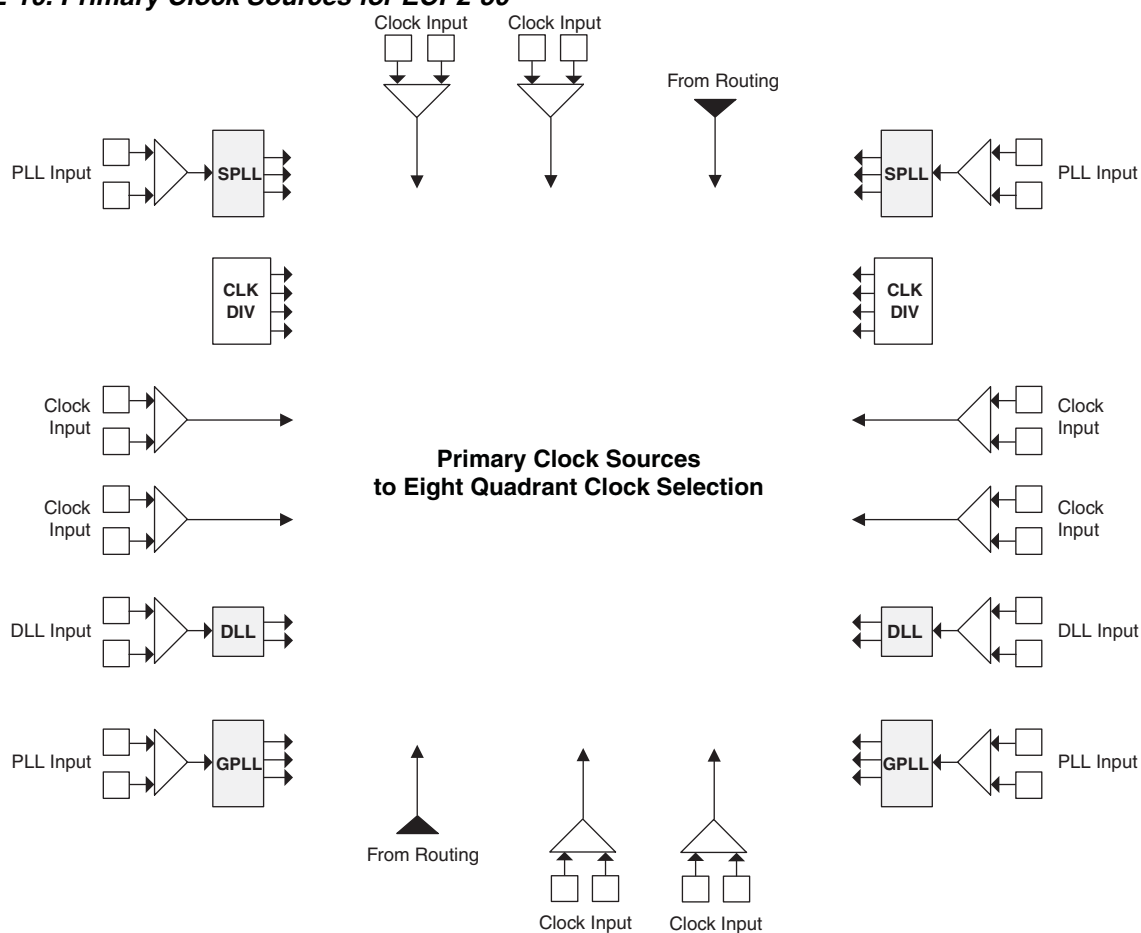


PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

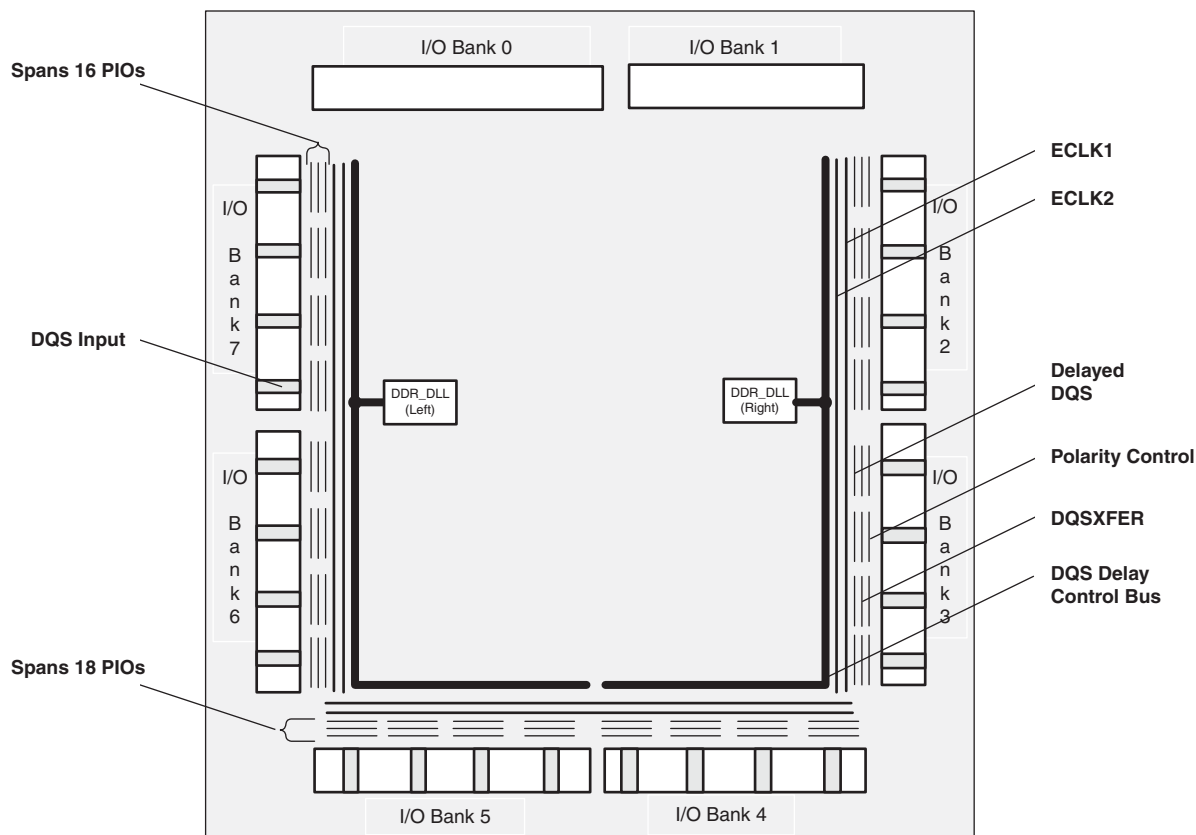
- PLL to PLL supported
- PLL to DLL supported

Figure 2-10. Primary Clock Sources for ECP2-50



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

LatticeECP2M Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply Current	ECP2M20	25	mA
		ECP2M35	50	mA
		ECP2M50	85	mA
		ECP2M70	100	mA
		ECP2M100	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	24	mA
		ECP2M35	24	mA
		ECP2M50	24	mA
		ECP2M70	24	mA
		ECP2M100	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2M20	2	mA
		ECP2M35	2	mA
		ECP2M50	2	mA
		ECP2M70	2	mA
		ECP2M100	2	mA
I_{CCJ}	V_{CCJ} Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 25^{\circ}\text{C}$, power supplies at normal voltage.

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

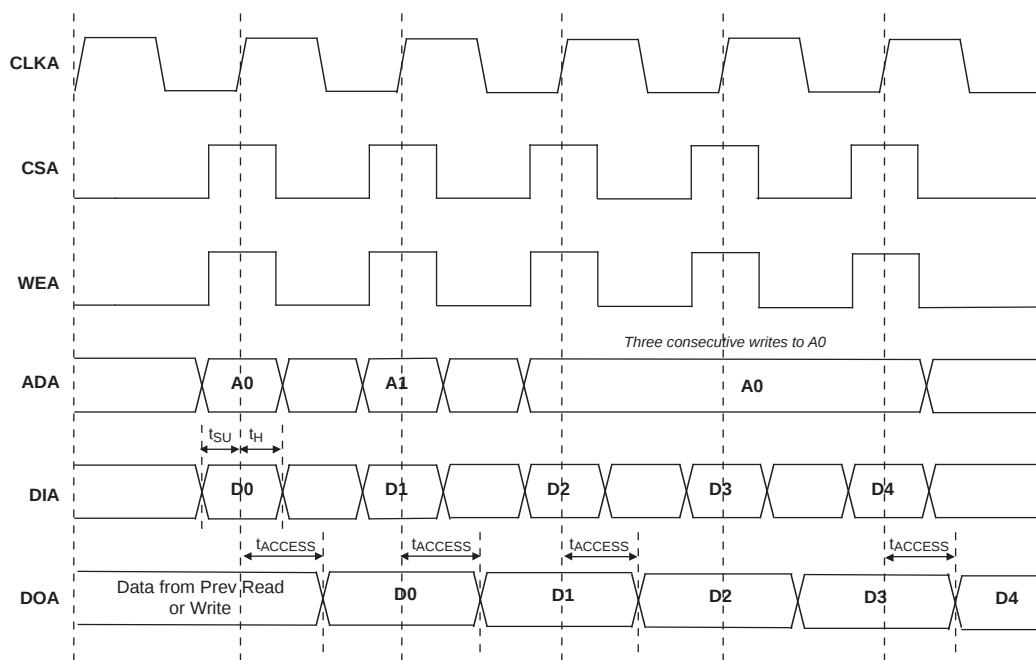
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP} V_{INM}$	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	μ A
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM})$, $R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, $R_T = 100$ Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Bottom Edge of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:

1. "n" is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
46	NC	5			PB16B	5	BDQ15	C
47	GND	-			GND	-		
48	VCC				VCC	-		
49	PB8A	5	PCLKT5_0/BDQ6	T	PB26A	5	PCLKT5_0/BDQ24	T
50	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
51	GND	-			GND	-		
52	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
53	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
54	VCC	-			VCC	-		
55	PB14A	4	BDQ15	T	PB34A	4	BDQ33	T
56	PB14B	4	BDQ15	C	PB34B	4	BDQ33	C
57	PB16A	4	BDQ15	T	PB40A	4	BDQ42	T
58	PB16B	4	BDQ15	C	PB40B	4	BDQ42	C
59	PB18A	4	BDQ15	T	PB44A	4	BDQ42	T
60	PB18B	4	BDQ15	C	PB44B	4	BDQ42	C
61	GND	-			GND	-		
62	PB20A	4	BDQ24	T	PB48A	4	BDQ51	T
63	PB20B	4	BDQ24	C	PB48B	4	BDQ51	C
64	VCCIO4	4			VCCIO4	4		
65	PB22A	4	BDQ24	T	PB50A	4	BDQ51	T
66	PB22B	4	BDQ24	C	PB50B	4	BDQ51	C
67	PB24A	4	BDQS24	T	PB52A	4	BDQ51	T
68	PB24B	4	BDQ24	C	PB52B	4	BDQ51	C
69	PB26A	4	BDQ24	T	PB54A	4	BDQ51	T
70	PB26B	4	BDQ24	C	PB54B	4	BDQ51	C
71	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
72	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
73	CFG1	8			CFG1	8		
74	CFG2	8			CFG2	8		
75	PROGRAMN	8			PROGRAMN	8		
76	INITN	8			INITN	8		
77	CFG0	8			CFG0	8		
78	CCLK	8			CCLK	8		
79	DONE	8			DONE	8		
80	PR29A	8	D0/SPIFASTN		PR29A	8	D0/SPIFASTN	
81	GND	-			GND	-		
82	PR26A	8	D6		PR26A	8	D6	
83	VCC	-			VCC	-		
84	PR25B	8	D7/SPID0	C	PR25B	8	D7/SPID0	C
85	VCCIO8	8			VCCIO8	8		
86	PR25A	8	DI/CSSPI0N	T	PR25A	8	DI/CSSPI0N	T
87	PR24B	8	DOOUT/CSON	C	PR24B	8	DOOUT/CSON	C
88	PR24A	8	BUSY/SISPI	T	PR24A	8	BUSY/SISPI	T
89	VCCIO3	3			VCCIO3	3		
90	VCCAUX	-			VCCAUX	-		

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
B15	PT40B	1		C	PT49B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
A15	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A14	PT39A	1		T	PT48A	1		T
B14	PT39B	1		C	PT48B	1		C
D14	PT37B	1		C	PT46B	1		C
E14	PT36B	1		C	PT45B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
C13	PT37A	1		T	PT46A	1		T
F14	PT36A	1		T	PT45A	1		T
A13	PT35B	1		C	PT44B	1		C
E13	PT34B	1		C	PT43B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B13	PT35A	1		T	PT44A	1		T
D13	PT34A	1		T	PT43A	1		T
E12	PT33B	1		C	PT42B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
D12	PT33A	1		T	PT42A	1		T
A12	PT31B	1		C	PT40B	1		C
B12	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C
VCCIO	VCCIO1	1			VCCIO1	1		
A11	PT31A	1		T	PT40A	1		T
C12	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T
F12	XRES	1			XRES	1		
B10	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
B11	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
C11	PT26B	0		C	PT35B	0		C
A10	PT27B	0		C	PT36B	0		C
C10	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
A9	PT27A	0		T	PT36A	0		T
A8	PT24B	0		C	PT33B	0		C
E11	PT25B	0		C	PT34B	0		C
A7	PT24A	0		T	PT33A	0		T
F11	PT25A	0		T	PT34A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
B8	PT23B	0		C	PT32B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B9	PT23A	0		T	PT32A	0		T
C8	PT20B	0		C	PT29B	0		C
B7	PT21B	0		C	PT30B	0		C
D8	PT20A	0		T	PT29A	0		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7/LDQ6	T (LVDS)*	
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7/LDQ6	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
F6	PL3A	7		T	PL3A	7	LDQ6	T	
F5	PL3B	7		C	PL3B	7	LDQ6	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E4	NC	-			PL4A	7	LDQ6	T (LVDS)*	
E3	NC	-			PL4B	7	LDQ6	C (LVDS)*	
E2	NC	-			PL5A	7	LDQ6	T	
E1	NC	-			PL5B	7	LDQ6	C	
GND	GNDIO7	-			GNDIO7	-			
H6	NC	-			PL6A	7	LDQS6	T (LVDS)*	
H5	NC	-			PL6B	7	LDQ6	C (LVDS)*	
F2	NC	-			PL7A	7	LDQ6	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F1	NC	-			PL7B	7	LDQ6	C	
H8	NC	-			PL8A	7	LDQ6	T (LVDS)*	
J9	NC	-			PL8B	7	LDQ6	C (LVDS)*	
G4	NC	-			PL9A	7	LDQ6	T	
GND	GNDIO7	-			GNDIO7	-			
G3	NC	-			PL9B	7	LDQ6	C	
H7	PL4A	7	LDQ8	T (LVDS)*	PL10A	7	LDQ14	T (LVDS)*	
J8	PL4B	7	LDQ8	C (LVDS)*	PL10B	7	LDQ14	C (LVDS)*	
G2	PL5A	7	LDQ8	T	PL11A	7	LDQ14	T	
G1	PL5B	7	LDQ8	C	PL11B	7	LDQ14	C	
H3	PL6A	7	LDQ8	T (LVDS)*	PL12A	7	LDQ14	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
H4	PL6B	7	LDQ8	C (LVDS)*	PL12B	7	LDQ14	C (LVDS)*	
J5	PL7A	7	LDQ8	T	PL13A	7	LDQ14	T	
J4	PL7B	7	LDQ8	C	PL13B	7	LDQ14	C	
J3	PL8A	7	LDQS8	T (LVDS)*	PL14A	7	LDQS14	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
K4	PL8B	7	LDQ8	C (LVDS)*	PL14B	7	LDQ14	C (LVDS)*	
H1	PL9A	7	LDQ8	T	PL15A	7	LDQ14	T	
H2	PL9B	7	LDQ8	C	PL15B	7	LDQ14	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K6	PL10A	7	LDQ8	T (LVDS)*	PL16A	7	LDQ14	T (LVDS)*	
K7	PL10B	7	LDQ8	C (LVDS)*	PL16B	7	LDQ14	C (LVDS)*	
J1	PL11A	7	LDQ8	T	PL17A	7	LDQ14	T	
J2	PL11B	7	LDQ8	C	PL17B	7	LDQ14	C	
GND	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K3	NC	-			NC	-			
K2	NC	-			NC	-			
GND	GNDIO7	-			GNDIO7	-			
K1	NC	-			NC	-			

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GND	GNDIO5	-			GNDIO5	-			
W10	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
Y10	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AA10	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AC8	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD8	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AB8	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AB10	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AE6	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
AF6	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
AA11	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AC9	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AB9	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	
AD9	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y11	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AB11	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
AE7	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
AF7	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AC10	PB20A	5	BDQ24	T	PB20A	5	BDQ24	T	
AD10	PB20B	5	BDQ24	C	PB20B	5	BDQ24	C	
AA12	PB21A	5	BDQ24	T	PB21A	5	BDQ24	T	
W12	PB21B	5	BDQ24	C	PB21B	5	BDQ24	C	
AB12	PB22A	5	BDQ24	T	PB22A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
Y12	PB22B	5	BDQ24	C	PB22B	5	BDQ24	C	
AD12	PB23A	5	BDQ24	T	PB23A	5	BDQ24	T	
AC12	PB23B	5	BDQ24	C	PB23B	5	BDQ24	C	
AC13	PB24A	5	BDQS24	T	PB24A	5	BDQS24	T	
GND	GNDIO5	-			GNDIO5	-			
AA13	PB24B	5	BDQ24	C	PB24B	5	BDQ24	C	
AD13	PB25A	5	BDQ24	T	PB25A	5	BDQ24	T	
AC14	PB25B	5	BDQ24	C	PB25B	5	BDQ24	C	
AE8	PB26A	5	BDQ24	T	PB26A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB26B	5	BDQ24	C	PB26B	5	BDQ24	C	
AB15	PB27A	5	BDQ24	T	PB27A	5	BDQ24	T	
Y13	PB27B	5	BDQ24	C	PB27B	5	BDQ24	C	
AE9	PB28A	5	BDQ24	T	PB28A	5	BDQ24	T	
GND	GNDIO5	-			GNDIO5	-			
AF9	PB28B	5	BDQ24	C	PB28B	5	BDQ24	C	
W13	PB29A	5	BDQ33	T	PB29A	5	BDQ33	T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*	PR44B	3	RLM0_GPLL_C_IN_A**/RDQ48	C (LVDS)*	
U25	PR30A	3	RLM0_GPLL_T_IN_A**/RDQ34	T (LVDS)*	PR44A	3	RLM0_GPLL_T_IN_A**/RDQ48	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCC	3			VCCPLL	3			
T19	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C	PR42B	3	RLM0_GDLLC_FB_A/RDQ39	C	
U20	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T	PR42A	3	RLM0_GDLLT_FB_A/RDQ39	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*	PR41B	3	RLM0_GDLLC_IN_A**/RDQ39	C (LVDS)*	
T26	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*	PR41A	3	RLM0_GDLLT_IN_A**/RDQ39	T (LVDS)*	
T20	PR26B	3	RDQ25	C	PR40B	3	RDQ39	C	
T22	PR26A	3	RDQ25	T	PR40A	3	RDQ39	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR25B	3	RDQ25	C (LVDS)*	PR39B	3	RDQ39	C (LVDS)*	
R25	PR25A	3	RDQS25***	T (LVDS)*	PR39A	3	RDQS39***	T (LVDS)*	
R22	NC	-			PR38B	3	RDQ39	C	
GND	GNDIO3	-			GNDIO3	-			
T21	NC	-			PR38A	3	RDQ39	T	
P26	NC	-			NC	-			
P25	NC	-			NC	-			
R24	NC	-			NC	-			
VCCIO	VCCIO3	3			VCCIO3	3			
R23	NC	-			NC	-			
P20	NC	-			NC	-			
R19	NC	-			NC	-			
P21	NC	-			PR34B	3	RDQ31	C	
GND	GNDIO3	-			GNDIO3	-			
P19	NC	-			PR34A	3	RDQ31	T	
P23	NC	-			PR33B	3	RDQ31	C (LVDS)*	
P22	NC	-			PR33A	3	RDQ31	T (LVDS)*	
N22	NC	-			PR32B	3	RDQ31	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	NC	-			PR32A	3	RDQ31	T	
N26	NC	-			PR31B	3	RDQ31	C (LVDS)*	
N25	NC	-			PR31A	3	RDQS31	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR24B	3	RDQ25	C	PR30B	3	RDQ31	C	
N20	PR24A	3	RDQ25	T	PR30A	3	RDQ31	T	
M26	PR23B	3	RDQ25	C (LVDS)*	PR29B	3	RDQ31	C (LVDS)*	
M25	PR23A	3	RDQ25	T (LVDS)*	PR29A	3	RDQ31	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR22B	3	VREF2_3/RDQ25	C	PR28B	3	VREF2_3/RDQ31	C	
N21	PR22A	3	VREF1_3/RDQ25	T	PR28A	3	VREF1_3/RDQ31	T	
L26	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	
L25	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	
N24	PR19B	2	PCLKC2_0/RDQ16	C	PR25B	2	PCLKC2_0/RDQ22	C	
M23	PR19A	2	PCLKT2_0/RDQ16	T	PR25A	2	PCLKT2_0/RDQ22	T	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U9	PL67B	6	LDQ66	C	PL72B	6	LDQ71	C	
AA5	PL68A	6	LDQ66	T (LVDS)*	PL73A	6	LDQ71	T*	
AA6	PL68B	6	LDQ66	C (LVDS)*	PL73B	6	LDQ71	C*	
Y7	PL69A	6	LDQ66	T	PL74A	6	LDQ71	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V9	PL69B	6	LDQ66	C	PL74B	6	LDQ71	C	
AC3	TCK	-			TCK	-			
W8	TDI	-			TDI	-			
AC4	TMS	-			TMS	-			
V8	TDO	-			TDO	-			
AA7	VCCJ	-			VCCJ	-			
AB6	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T	
Y8	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C	
AD1	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD2	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AC5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AA8	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC6	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
AB7	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
Y9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AD3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA9	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
W10	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC7	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
Y10	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AE2	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO5	-			
AE4	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
AE3	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AB8	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AE5	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD6	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AA10	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AC8	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
W12	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC9	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
W13	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AB10	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AF3	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U20	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V27	GND	-		
V4	GND	-		
W23	GND	-		
W8	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
AA26	NC	-		
AB10	NC	-		
AB11	NC	-		
AB12	NC	-		
AB13	NC	-		
AB14	NC	-		
AB15	NC	-		
AB16	NC	-		
AB17	NC	-		
AB19	NC	-		
AB20	NC	-		
AB21	NC	-		
AB9	NC	-		
AC10	NC	-		
AC11	NC	-		
AC21	NC	-		
AC22	NC	-		
AC8	NC	-		
AC9	NC	-		
AD21	NC	-		
AD22	NC	-		
AD4	NC	-		
AD5	NC	-		
AD6	NC	-		
AD7	NC	-		
AD8	NC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AN29	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AM28	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AL27	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AM29	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AL29	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AL30	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AK30	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AK29	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AM30	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AL31	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AM31	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AN30	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AP30	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T
AL32	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AP31	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AN31	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AP32	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AM34	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AP33	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AN32	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AM32	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AN34	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AM33	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AN33	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AH28	CFG2	8			CFG2	8		
AD24	CFG1	8			CFG1	8		
AJ29	CFG0	8			CFG0	8		
AF25	PROGRAMN	8			PROGRAMN	8		
AJ28	CCLK	8			CCLK	8		
AE25	INITN	8			INITN	8		
AK31	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE24	WRITEN***	8			WRITEN***	8		
AJ30	CS1N***	8			CS1N***	8		
AD25	CSN***	8			CSN***	8		
AG29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG28	D1***	8			D1***	8		
AG30	D2***	8			D2***	8		
AH29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF26	D4***	8			D4***	8		
AH30	D5***	8			D5***	8		
AE26	D6***	8			D6***	8		
AJ31	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG27	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AK32	DOUT/CSN/ CSSPI1N***	8			DOUT/CSN/ CSSPI1N***	8		
AK33	BUSY/SISPI***	8			BUSY/SISPI***	8		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO1	-			GNDIO1	-		
F19	PT59B	1		C	PT68B	1		C
D18	PT59A	1		T	PT68A	1		T
L18	NC	-			PT67B	1		C
K19	NC	-			PT67A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A18	PT57B	1	VREF2_1	C	PT66B	1	VREF2_1	C
B18	PT57A	1	VREF1_1	T	PT66A	1	VREF1_1	T
G18	PT56B	1	PCLKC1_0	C	PT65B	1	PCLKC1_0	C
E18	PT56A	1	PCLKT1_0	T	PT65A	1	PCLKT1_0	T
F18	PT55B	0	PCLKC0_0	C	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G19	PT55A	0	PCLKT0_0	T	PT64A	0	PCLKT0_0	T
H18	PT54B	0	VREF2_0	C	PT63B	0	VREF2_0	C
K18	PT54A	0	VREF1_0	T	PT63A	0	VREF1_0	T
VCCIO	VCCIO0	0			VCCIO0	0		
J18	PT53B	0		C	PT60B	0		C
L17	PT53A	0		T	PT60A	0		T
G17	PT52B	0		C	PT59B	0		C
-	-	-			GNDIO0	-		
J17	PT52A	0		T	PT59A	0		T
H17	PT51B	0		C	PT58B	0		C
-	-	-			VCCIO0	0		
K17	PT51A	0		T	PT58A	0		T
B17	PT50B	0		C	PT57B	0		C
GNDIO	GNDIO0	-			-	-		
A17	PT50A	0		T	PT57A	0		T
D17	PT49B	0		C	PT56B	0		C
VCCIO	VCCIO0	0			-	-		
F17	PT49A	0		T	PT56A	0		T
B16	PT48B	0		C	PT55B	0		C
A16	PT48A	0		T	PT55A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
E17	PT47B	0		C	PT52B	0		C
C17	PT47A	0		T	PT52A	0		T
K16	PT46B	0		C	PT51B	0		C
J15	PT46A	0		T	PT51A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
G16	PT45B	0		C	PT50B	0		C
H15	PT45A	0		T	PT50A	0		T
A15	PT44B	0		C	PT49B	0		C
B15	PT44A	0		T	PT49A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
L16	PT43B	0		C	PT48B	0		C
K15	PT43A	0		T	PT48A	0		T
F16	PT42B	0		C	PT47B	0		C
E16	PT42A	0		T	PT47A	0		T
E15	PT41B	0		C	PT46B	0		C

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152C	436	1.2V	-5	fpBGA	1152	Com	70
LFE2M70SE-6F1152C	436	1.2V	-6	fpBGA	1152	Com	70
LFE2M70SE-7F1152C	436	1.2V	-7	fpBGA	1152	Com	70
LFE2M70SE-5F900C	416	1.2V	-5	fpBGA	900	Com	70
LFE2M70SE-6F900C	416	1.2V	-6	fpBGA	900	Com	70
LFE2M70SE-7F900C	416	1.2V	-7	fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152C	520	1.2V	-5	fpBGA	1152	Com	100
LFE2M100SE-6F1152C	520	1.2V	-6	fpBGA	1152	Com	100
LFE2M100SE-7F1152C	520	1.2V	-7	fpBGA	1152	Com	100
LFE2M100SE-5F900C	416	1.2V	-5	fpBGA	900	Com	100
LFE2M100SE-6F900C	416	1.2V	-6	fpBGA	900	Com	100
LFE2M100SE-7F900C	416	1.2V	-7	fpBGA	900	Com	100