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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

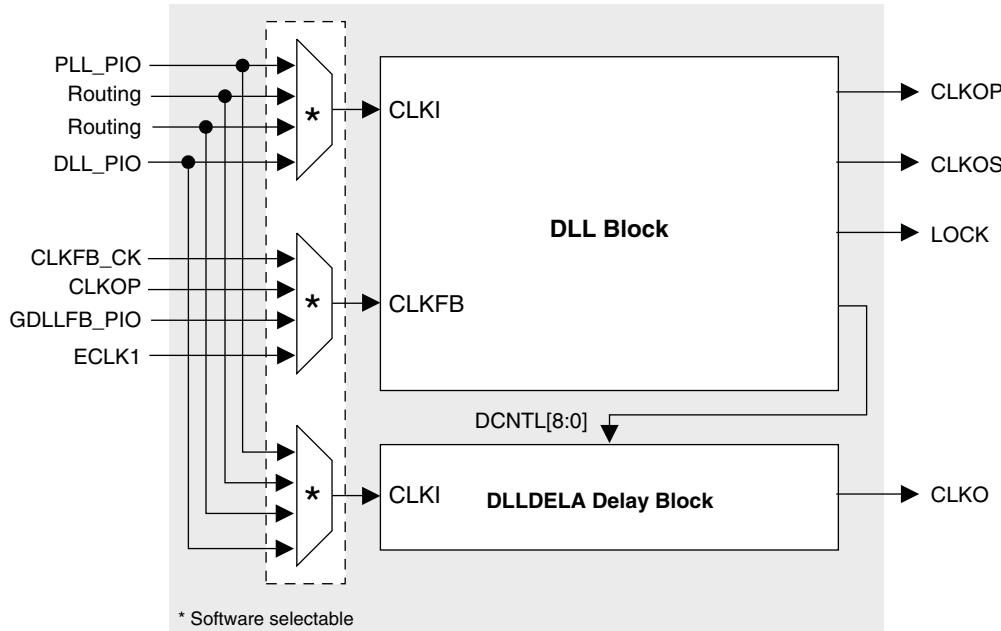
Product Status	Active
Number of LABs/CLBs	750
Number of Logic Elements/Cells	6000
Total RAM Bits	56320
Number of I/O	90
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-6se-5tn144i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-6se-5tn144i</a>

**Table 2-5. DLL Signals**

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

### DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

**Figure 2-7. DLLDELA Delay Block**


### PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

## SERDES Power Supply Requirements (LatticeECP2M Family Only)<sup>1</sup>

Over Recommended Operating Conditions

Symbol	Description	Typ. <sup>2</sup>	Units
<b>Standby (Power Down)</b>			
I <sub>CCTX-SB</sub>	V <sub>CCTX</sub> current (per channel)	10	µA
I <sub>CCRX-SB</sub>	V <sub>CCRX</sub> current (per channel)	75	µA
I <sub>CCIB-SB</sub>	Input buffer current (per channel)	0	µA
I <sub>CCOB-SB</sub>	Output buffer current (per channel)	0	µA
I <sub>CCP-SB</sub>	SERDES PLL current (per quad)	30	µA
I <sub>CCAX33-SB</sub>	SERDES termination current (per quad)	10	µA
<b>Operating (Data Rate = 3.125 Gbps)</b>			
I <sub>CCTX-OP</sub>	V <sub>CCTX</sub> current (per channel)	19	mA
I <sub>CCRX-OP</sub>	V <sub>CCRX</sub> current (per channel)	34	mA
I <sub>CCIB-OP</sub>	Input buffer current (per channel)	4	mA
I <sub>CCOB-OP</sub>	Output buffer current (per channel)	13	mA
I <sub>CCP-OP</sub>	SERDES PLL current (per quad)	26	mA
I <sub>CCAX33-OP</sub>	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.

2. T<sub>J</sub> = 25°C, power supplies at nominal voltage.

## SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

**Table 3-1. SERDES Power<sup>1</sup>**

Symbol	Description	Typ. <sup>2</sup>	Units
P <sub>S-1CH-31</sub>	SERDES power (one channel @ 3.125 Gbps)	90	mW
P <sub>S-1CH-25</sub>	SERDES power (one channel @ 2.5 Gbps)	87	mW
P <sub>S-1CH-12</sub>	SERDES power (one channel @ 1.25 Gbps)	86	mW
P <sub>S-1CH-02</sub>	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

2. Typical values measured at 25°C and 1.2V.

## sys/I/O Recommended Operating Conditions

Standard	$V_{CCIO}$			$V_{REF}$ (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3 <sup>2</sup>	3.135	3.3	3.465	—	—	—
LVCMOS 2.5 <sup>2</sup>	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2 <sup>2</sup>	1.14	1.2	1.26	—	—	—
LVTTL <sup>2</sup>	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 <sup>2</sup> Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 <sup>2</sup> Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 <sup>2</sup> Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL <sup>2</sup> 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL <sup>2</sup> 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS <sup>2</sup>	2.375	2.5	2.625	—	—	—
MLVDS25 <sup>1</sup>	2.375	2.5	2.625	—	—	—
LVPECL33 <sup>1,2</sup>	3.135	3.3	3.465	—	—	—
BLVDS25 <sup>1,2</sup>	2.375	2.5	2.625	—	—	—
RSDS <sup>1,2</sup>	2.375	2.5	2.625	—	—	—
SSTL18D_I <sup>2</sup> , II <sup>2</sup>	1.71	1.8	1.89	—	—	—
SSTL25D_I <sup>2</sup> , II <sup>2</sup>	2.375	2.5	2.625	—	—	—
SSTL33D_I <sup>2</sup> , II <sup>2</sup>	3.135	3.3	3.465	—	—	—
HSTL15D_I <sup>2</sup>	1.425	1.5	1.575	—	—	—
HSTL18D_I <sup>2</sup> , II <sup>2</sup>	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of  $V_{CCIO}$ .

## SERDES External Reference Clock (LatticeECP2M Family Only)

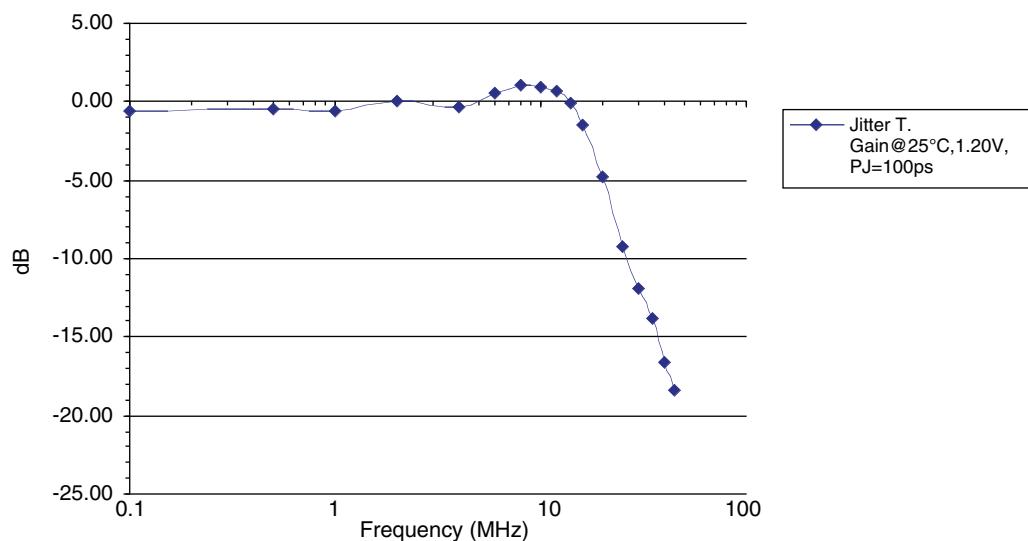
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

**Table 3-14. External Reference Clock Specification (refclkp/refclkn)**

Symbol	Description	Min.	Typ.	Max.	Units
$F_{REF}$	Frequency range	25	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance	-300	—	300	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock <sup>1</sup>	100	—	1200	mV, p-p
$V_{REF-IN}$	Input levels	0	—	$V_{CCP} + 0.8$	V
$V_{REF-CM-DC}$	Input common mode range (DC coupled)	0.5	—	1.2	V
$V_{REF-CM-AC}$	Input common mode range (AC coupled) <sup>2</sup>	0	—	1.5	V
$D_{REF}$	Duty cycle <sup>3</sup>	40	—	60	%
$T_{REF-R}$	Rise time (20% to 80%)		500	1000	ps
$T_{REF-F}$	Fall time (80% to 20%)		500	1000	ps
$Z_{REF-IN-TERM}$	Input termination		50/2K		Ohms
$C_{REF-IN-CAP}$	Input capacitance <sup>4</sup>	—	—	1.5	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:  
 $(\text{Min input level}) + (\text{Peak-to-peak input swing})/2 \leq (\text{Input common mode voltage}) \leq (\text{Max input level}) - (\text{Peak-to-peak input swing})/2$
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

**Figure 3-13. Jitter Transfer**



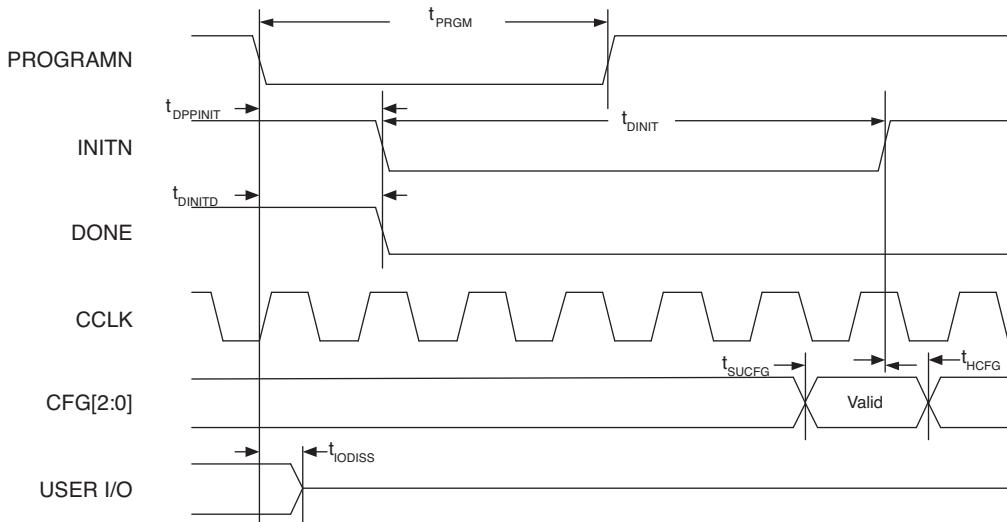
Note: This graph is for a nominal device.

## SERDES Power-Down/Power-Up Specification

**Table 3-15. Power-Down and Power-Up Specification**

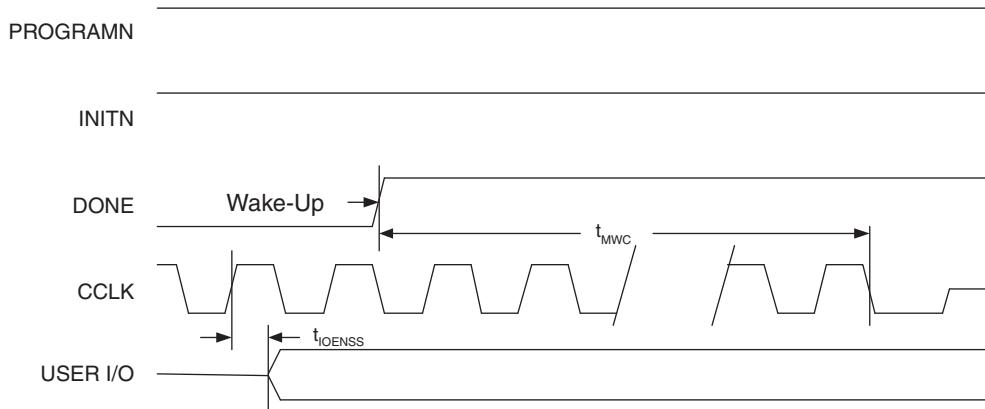
Symbol	Description	Max.	Units
$t_{PWRDN}$	Power-down time after all power down register bits set to '0'	10	$\mu s$
$t_{PWRUP}$	Power-up time after all power down register bits set to '1'	100	$\mu s$

**Figure 3-18. Configuration from PROGRAMN Timing**

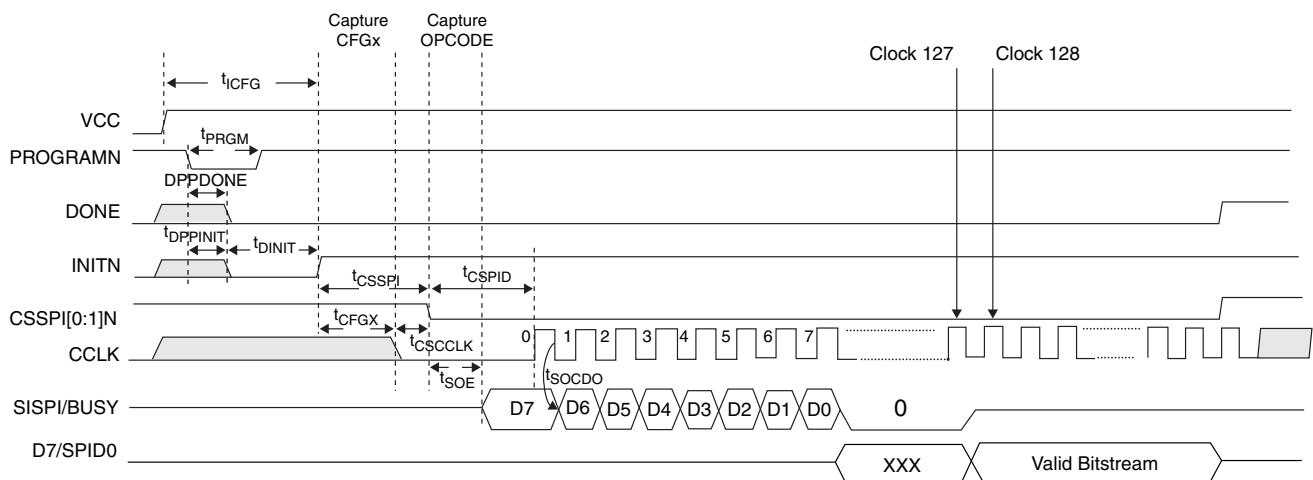


1. The CFG pins are normally static (hard wired)

**Figure 3-19. Wake-Up Timing**



**Figure 3-20. SPI/SPI<sub>M</sub> Configuration Waveforms**



**LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70 (Cont.)**

Pin Type	LFE2-50		LFE2-70	
	484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Available DDR-Interfaces per I/O Bank <sup>1</sup>	Bank0	0	0	0
	Bank1	0	0	0
	Bank2	2	3	3
	Bank3	0	3	3
	Bank4	3	4	4
	Bank5	3	4	4
	Bank6	1	4	4
	Bank7	2	3	3
	Bank8	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0
	Bank1	0	0	0
	Bank2	0	0	0
	Bank3	0	0	0
	Bank4	46	62	62
	Bank5	46	68	68
	Bank6	0	0	0
	Bank7	0	0	0
	Bank8	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## LatticeECP2M Power Supply and NC

Signal	256 fpBGA	484 fpBGA
V <sub>CC</sub>	G7, G9, H7, J10, K10, K8	J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
V <sub>CCIO0</sub>	E7	B5, B9, E7, H9
V <sub>CCIO1</sub>	E10	D13, E16, H14
V <sub>CCIO2</sub>	E14, G12	E21, G18, J15, K19
V <sub>CCIO3</sub>	K12, M14	N19, P15, T18, V21
V <sub>CCIO4</sub>	M10, P12	AA18, R14, V16, W13
V <sub>CCIO5</sub>	M7, P5	AA5, R9, V7, W10
V <sub>CCIO6</sub>	K5, M3	N4, P8, T5, V2
V <sub>CCIO7</sub>	E3, G5	E2, G5, J8, K4
V <sub>CCIO8</sub>	T15	AA22, U19
V <sub>CCJ</sub>	K7	W4
V <sub>CCAUX</sub>	G8, H10, J7, K9	H11, H12, L15, L8, M15, M8, R11, R12
V <sub>CCPLL</sub>	G10	R8, H15, H8, R15
SERDES Power <sup>3</sup>	C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3	C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10
GND <sup>1</sup>	A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13
NC <sup>2</sup>	D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9	<b>LFE2M20:</b> D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15 <b>LFE2M35:</b> D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15, U6 <b>LFE2M50:</b> Y15, W15, AB20, AB21, AA20, AB19, AB18, Y22, Y21, Y17, Y18, Y16, W17, Y19, Y20, W19, W18, V17, V18, D15, G14, G15, D14, E15, E14, F15, F14, F13, G12, G13

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

**LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)**

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			GNDIO1	1			
-	-	-			VCCIO	1			
D10	PT19B	1		C	PT37B	1		C	
C10	PT19A	1		T	PT37A	1		T	
GND	GNDIO1	-			GNDIO1	-			
B10	PT18B	1		C	PT36B	1		C	
A9	PT17B	1		C	PT35B	1		C	
A10	PT18A	1		T	PT36A	1		T	
B9	PT17A	1		T	PT35A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A8	PT16B	1		C	PT34B	1		C	
D9	PT15B	1		C	PT33B	1		C	
B8	PT16A	1		T	PT34A	1		T	
C9	PT15A	1		T	PT33A	1		T	
GND	GNDIO1	-			GNDIO1	-			
B7	PT14B	1		C	PT32B	1		C	
E9	PT13B	1		C	PT31B	1		C	
A7	PT14A	1		T	PT32A	1		T	
D8	PT13A	1		T	PT31A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A6	PT12B	1	PCLKC1_0	C	PT30B	1	PCLKC1_0	C	
B6	PT12A	1	PCLKT1_0	T	PT30A	1	PCLKT1_0	T	
E6	XRES	-			XRES	1			
F8	PT10B	0	PCLKC0_0	C	PT28B	0	PCLKC0_0	C	
GND	GNDIO0	-			GNDIO0	-			
E8	PT10A	0	PCLKT0_0	T	PT28A	0	PCLKT0_0	T	
A5	PT9B	0		C	PT27B	0		C	
A3	PT8B	0		C	PT26B	0		C	
A4	PT9A	0		T	PT27A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
B3	PT8A	0		T	PT26A	0		T	
A2	PT7B	0		C	PT25B	0		C	
C7	PT6B	0		C	PT24B	0		C	
B2	PT7A	0		T	PT25A	0		T	
D7	PT6A	0		T	PT24A	0		T	
D6	PT5B	0		C	PT23B	0		C	
GND	GNDIO0	-			GNDIO0	-			
F7	PT4B	0		C	PT22B	0		C	
C6	PT5A	0		T	PT23A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F6	PT4A	0		T	PT22A	0		T	
C4	PT3B	0		C	PT21B	0		C	
B4	PT3A	0		T	PT21A	0		T	
-	-	-			GNDIO0	0			
-	-	-			VCCIO	0			

**LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)**

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO	VCCIO1	1		
D12	D12	PT62A	1		T
B14	B14	PT61B	1		C
C14	C14	PT60B	1		C
A14	A14	PT61A	1		T
D13	D13	PT60A	1		T
C13	C13	PT59B	1		C
GND	GND	GNDIO1	-		
A13	A13	PT58B	1		C
B13	B13	PT59A	1		T
VCCIO	VCCIO	VCCIO1	1		
A12	A12	PT58A	1		T
B11	B11	PT57B	1		C
D11	D11	PT56B	1		C
A11	A11	PT57A	1		T
C11	C11	PT56A	1		T
-	GND	GNDIO1	1		
-	VCC	VCCIO	1		
D10	D10	PT46B	1		C
C10	C10	PT46A	1		T
GND	GND	GNDIO1	-		
B10	B10	PT45B	1		C
A9	A9	PT44B	1		C
A10	A10	PT45A	1		T
B9	B9	PT44A	1		T
VCCIO	VCCIO	VCCIO1	1		
A8	A8	PT43B	1		C
D9	D9	PT42B	1		C
B8	B8	PT43A	1		T
C9	C9	PT42A	1		T
GND	GND	GNDIO1	-		
B7	B7	PT41B	1		C
E9	E9	PT40B	1		C
A7	A7	PT41A	1		T
D8	D8	PT40A	1		T
VCCIO	VCCIO	VCCIO1	1		
A6	A6	PT39B	1	PCLKC1_0	C
B6	B6	PT39A	1	PCLKT1_0	T
E6	E6	XRES	1		
F8	F8	PT37B	0	PCLKC0_0	C
GND	GND	GNDIO0	-		
E8	E8	PT37A	0	PCLKT0_0	T

**LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)**

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C2	PT3A	0		T	PT3A	0		T	
J10	VCC	-			VCC	-			
J11	VCC	-			VCC	-			
J12	VCC	-			VCC	-			
J13	VCC	-			VCC	-			
K14	VCC	-			VCC	-			
K9	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L9	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M9	VCC	-			VCC	-			
N14	VCC	-			VCC	-			
N9	VCC	-			VCC	-			
P10	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P13	VCC	-			VCC	-			
G10	VCCIO0	0			VCCIO0	0			
G9	VCCIO0	0			VCCIO0	0			
H9	VCCIO0	0			VCCIO0	0			
H8	VCCIO0	0			VCCIO0	0			
G11	VCCIO1	1			VCCIO1	1			
G12	VCCIO1	1			VCCIO1	1			
G13	VCCIO1	1			VCCIO1	1			
G14	VCCIO1	1			VCCIO1	1			
H14	VCCIO2	2			VCCIO2	2			
H15	VCCIO2	2			VCCIO2	2			
J15	VCCIO2	2			VCCIO2	2			
K16	VCCIO2	2			VCCIO2	2			
L16	VCCIO3	3			VCCIO3	3			
M16	VCCIO3	3			VCCIO3	3			
N16	VCCIO3	3			VCCIO3	3			
P16	VCCIO3	3			VCCIO3	3			
R14	VCCIO4	4			VCCIO4	4			
T12	VCCIO4	4			VCCIO4	4			
T13	VCCIO4	4			VCCIO4	4			
T14	VCCIO4	4			VCCIO4	4			
R9	VCCIO5	5			VCCIO5	5			
T10	VCCIO5	5			VCCIO5	5			
T11	VCCIO5	5			VCCIO5	5			
T9	VCCIO5	5			VCCIO5	5			
N7	VCCIO6	6			VCCIO6	6			
P7	VCCIO6	6			VCCIO6	6			
P8	VCCIO6	6			VCCIO6	6			

**LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)**

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB29B	5	BDQ33	C	PB29B	5	BDQ33	C	
AE10	PB30A	5	BDQ33	T	PB30A	5	BDQ33	T	
AF10	PB30B	5	BDQ33	C	PB30B	5	BDQ33	C	
W14	PB31A	5	BDQ33	T	PB31A	5	BDQ33	T	
AB13	PB31B	5	BDQ33	C	PB31B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB32A	5	BDQ33	T	PB32A	5	BDQ33	T	
AB14	PB32B	5	BDQ33	C	PB32B	5	BDQ33	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB33A	5	BDQS33	T	PB33A	5	BDQS33	T	
AF11	PB33B	5	BDQ33	C	PB33B	5	BDQ33	C	
AD14	PB34A	5	BDQ33	T	PB34A	5	BDQ33	T	
AA15	PB34B	5	BDQ33	C	PB34B	5	BDQ33	C	
AE12	PB35A	5	PCLKT5_0/BDQ33	T	PB35A	5	PCLKT5_0/BDQ33	T	
AF12	PB35B	5	PCLKC5_0/BDQ33	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB40A	4	PCLKT4_0/BDQ42	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB40B	4	PCLKC4_0/BDQ42	C	PB40B	4	PCLKC4_0/BDQ42	C	
AE13	PB41A	4	BDQ42	T	PB41A	4	BDQ42	T	
AF13	PB41B	4	BDQ42	C	PB41B	4	BDQ42	C	
AB17	PB42A	4	BDQS42	T	PB42A	4	BDQS42	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB42B	4	BDQ42	C	PB42B	4	BDQ42	C	
AE14	PB43A	4	BDQ42	T	PB43A	4	BDQ42	T	
AF14	PB43B	4	BDQ42	C	PB43B	4	BDQ42	C	
AA16	PB44A	4	BDQ42	T	PB44A	4	BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB44B	4	BDQ42	C	PB44B	4	BDQ42	C	
AC17	PB45A	4	BDQ42	T	PB45A	4	BDQ42	T	
AB16	PB45B	4	BDQ42	C	PB45B	4	BDQ42	C	
AE15	PB46A	4	BDQ42	T	PB46A	4	BDQ42	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB46B	4	BDQ42	C	PB46B	4	BDQ42	C	
AE16	PB47A	4	BDQ51	T	PB47A	4	BDQ51	T	
AF16	PB47B	4	BDQ51	C	PB47B	4	BDQ51	C	
Y16	PB48A	4	BDQ51	T	PB48A	4	BDQ51	T	
AB18	PB48B	4	BDQ51	C	PB48B	4	BDQ51	C	
AD17	PB49A	4	BDQ51	T	PB49A	4	BDQ51	T	
AD18	PB49B	4	BDQ51	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB50A	4	BDQ51	T	PB50A	4	BDQ51	T	
AD19	PB50B	4	BDQ51	C	PB50B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB51A	4	BDQS51	T	PB51A	4	BDQS51	T	

**LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)**

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L2	PL24B	7	LDQ24	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
L1	PL25A	7	LUM0_SPLL_IN_A/LDQ24	T	PL38A	7	LUM0_SPLL_IN_A/LDQ37	T	
VCCIO	VCCIO7	7			VCCIO7	7			
M2	PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C	
M1	PL26A	7	LUM0_SPLLFB_IN_A/LDQ24	T	PL39A	7	LUM0_SPLLFB_IN_A/LDQ37	T	
N2	PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
M8	VCCPLL	7			NC	-			
VCCIO	VCCIO7	7			VCCIO7	7			
GND	GNDIO7	-			GNDIO7	-			
N1	PL37A	7	LDQ41		PL50A	7	LDQ54		
L8	PL38A	7	LDQ41	T	PL51A	7	LDQ54	T	
K8	PL38B	7	LDQ41	C	PL51B	7	LDQ54	C	
VCCIO	VCCIO7	7			VCCIO7	7			
L6	PL39A	7	LDQ41	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*	
K5	PL39B	7	LDQ41	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*	
L7	PL40A	7	LDQ41	T	PL53A	7	LDQ54	T	
L5	PL40B	7	LDQ41	C	PL53B	7	LDQ54	C	
GND	GNDIO7	-			GNDIO7	-			
P1	PL41A	7	LDQS41	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*	
P2	PL41B	7	LDQ41	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*	
M6	PL42A	7	LDQ41	T	PL55A	7	LDQ54	T	
VCCIO	VCCIO7	7			VCCIO7	7			
N8	PL42B	7	LDQ41	C	PL55B	7	LDQ54	C	
R1	PL43A	7	LDQ41	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*	
R2	PL43B	7	LDQ41	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*	
M7	PL44A	7	PCLKT7_0/LDQ41	T	PL57A	7	PCLKT7_0/LDQ54	T	
GND	GNDIO7	-			GNDIO7	-			
N9	PL44B	7	PCLKC7_0/LDQ41	C	PL57B	7	PCLKC7_0/LDQ54	C	
M4	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*	
M5	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*	
N7	PL47A	6	VREF2_6/LDQ50	T	PL60A	6	VREF2_6/LDQ63	T	
P9	PL47B	6	VREF1_6/LDQ50	C	PL60B	6	VREF1_6/LDQ63	C	
N3	PL48A	6	LDQ50	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
N4	PL48B	6	LDQ50	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*	
N5	PL49A	6	LDQ50	T	PL62A	6	LDQ63	T	
P7	PL49B	6	LDQ50	C	PL62B	6	LDQ63	C	
T1	PL50A	6	LDQS50	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
T2	PL50B	6	LDQ50	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*	
P8	PL51A	6	LDQ50	T	PL64A	6	LDQ63	T	
P6	PL51B	6	LDQ50	C	PL64B	6	LDQ63	C	
VCCIO	VCCIO6	6			VCCIO6	6			
P5	PL52A	6	LDQ50	T (LVDS)*	PL65A	6	LDQ63	T (LVDS)*	
P4	PL52B	6	LDQ50	C (LVDS)*	PL65B	6	LDQ63	C (LVDS)*	

**LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)**

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W5	PL71B	6	LDQ75	C (LVDS)*	PL84B	6	LDQ88	C (LVDS)*	
AC1	PL72A	6	LDQ75	T	PL85A	6	LDQ88	T	
AD1	PL72B	6	LDQ75	C	PL85B	6	LDQ88	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y6	PL73A	6	LDQ75	T (LVDS)*	PL86A	6	LDQ88	T (LVDS)*	
Y5	PL73B	6	LDQ75	C (LVDS)*	PL86B	6	LDQ88	C (LVDS)*	
AE2	PL74A	6	LDQ75	T	PL87A	6	LDQ88	T	
AD2	PL74B	6	LDQ75	C	PL87B	6	LDQ88	C	
GND	GNDIO6	-			GNDIO6	-			
AB3	PL75A	6	LDQS75	T (LVDS)*	PL88A	6	LDQS88	T (LVDS)*	
AB2	PL75B	6	LDQ75	C (LVDS)*	PL88B	6	LDQ88	C (LVDS)*	
W7	PL76A	6	LDQ75	T	PL89A	6	LDQ88	T	
VCCIO	VCCIO6	6			VCCIO6	6			
W8	PL76B	6	LDQ75	C	PL89B	6	LDQ88	C	
Y7	PL77A	6	LDQ75	T (LVDS)*	PL90A	6	LDQ88	T (LVDS)*	
Y8	PL77B	6	LDQ75	C (LVDS)*	PL90B	6	LDQ88	C (LVDS)*	
AC2	PL78A	6	LDQ75	T	PL91A	6	LDQ88	T	
GND	GNDIO6	-			GNDIO6	-			
AD3	PL78B	6	LDQ75	C	PL91B	6	LDQ88	C	
AC3	TCK	-			TCK	-			
AA8	TDI	-			TDI	-			
AB4	TMS	-			TMS	-			
AA5	TDO	-			TDO	-			
AB5	VCCJ	-			VCCJ	-			
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
GND	GNDIO5	-			GNDIO5	-			
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			

**LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)**

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GND	GNDIO2	-			GNDIO2	-			
L21	PR43B	2	RDQ41	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*	
K22	PR43A	2	RDQ41	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*	
M24	PR42B	2	RDQ41	C	PR55B	2	RDQ54	C	
N23	PR42A	2	RDQ41	T	PR55A	2	RDQ54	T	
VCCIO	VCCIO2	2			VCCIO2	2			
K26	PR41B	2	RDQ41	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*	
K25	PR41A	2	RDQS41	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*	
M20	PR40B	2	RDQ41	C	PR53B	2	RDQ54	C	
GND	GNDIO2	-			GNDIO2	-			
M19	PR40A	2	RDQ41	T	PR53A	2	RDQ54	T	
L22	PR39B	2	RDQ41	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*	
M22	PR39A	2	RDQ41	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*	
K21	PR38B	2	RDQ41	C	PR51B	2	RDQ54	C	
VCCIO	VCCIO2	2			VCCIO2	2			
M21	PR38A	2	RDQ41	T	PR51A	2	RDQ54	T	
K24	PR37B	2	RDQ41	C (LVDS)*	PR50B	2	RDQ54	C (LVDS)*	
J24	PR37A	2	RDQ41	T (LVDS)*	PR50A	2	RDQ54	T (LVDS)*	
GND	GNDIO2	-			GNDIO2	-			
VCCIO	VCCIO2	2			VCCIO2	2			
L20	VCCPLL	2			NC	-			
GND	GNDIO2	-			GNDIO2	-			
J26	PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C	
J25	PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T	
J23	PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C	
K23	PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H26	PR24B	2	RDQ24	C (LVDS)*	PR37B	2	RDQ37	C (LVDS)*	
H25	PR24A	2	RDQS24***	T (LVDS)*	PR37A	2	RDQS37***	T (LVDS)*	
H24	PR23B	2	RDQ24	C	PR36B	2	RDQ37	C	
GND	GNDIO2	-			GNDIO2	-			
H23	PR23A	2	RDQ24	T	PR36A	2	RDQ37	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G26	PR19B	2	RDQ16	C	PR32B	2	RDQ29	C	
GND	GNDIO2	-			GNDIO2	-			
G25	PR19A	2	RDQ16	T	PR32A	2	RDQ29	T	
F26	PR18B	2	RDQ16	C (LVDS)*	PR31B	2	RDQ29	C (LVDS)*	
F25	PR18A	2	RDQ16	T (LVDS)*	PR31A	2	RDQ29	T (LVDS)*	
K20	PR17B	2	RDQ16	C	PR30B	2	RDQ29	C	
VCCIO	VCCIO2	2			VCCIO2	2			
L19	PR17A	2	RDQ16	T	PR30A	2	RDQ29	T	
E26	PR16B	2	RDQ16	C (LVDS)*	PR29B	2	RDQ29	C (LVDS)*	
E25	PR16A	2	RDQS16	T (LVDS)*	PR29A	2	RDQS29	T (LVDS)*	
GND	GNDIO2	-			GNDIO2	-			
J22	PR15B	2	RDQ16	C	PR28B	2	RDQ29	C	
H22	PR15A	2	RDQ16	T	PR28A	2	RDQ29	T	

**LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)**

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T7	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
T8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C	
L7	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T	
L8	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C	
GNDIO	GNDIO4	-			GNDIO4	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
P8	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T	
N8	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C	
R7	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T	
R8	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C	
N7	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T	
M8	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
R9	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T	
T9	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
T10	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T	
R10	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C	
N9	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T	
P10	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
L9	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T	
M9	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C	
T11	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T	
R11	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T12	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T	
T13	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
P11	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T	
N10	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C	
T14	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T	
R13	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C	
R15	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T	
R16	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
R14	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T	
P15	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C	
P16	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T	
P14	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
L11	CFG2	8			CFG2	8			
L10	CFG1	8			CFG1	8			
P13	CFG0	8			CFG0	8			
N12	PROGRAMN	8			PROGRAMN	8			

**LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)**

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C12	URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCRX2	12		
A15	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
E13	PT55B	1		C
D12	PT55A	1		T
GNDIO	GNDIO1	-		
A9	PT54B	1		C
A8	PT54A	1		T
A7	PT53B	1		C
A6	PT53A	1		T
VCCIO	VCCIO1	1		
E12	PT52B	1		C
F12	PT52A	1		T
A5	PT51B	1		C
A4	PT51A	1		T
GNDIO	GNDIO1	-		
B7	PT50B	1		C
B8	PT50A	1		T
G11	PT49B	1		C
E11	PT49A	1		T
VCCIO	VCCIO1	1		
D11	PT48B	1	VREF2_1	C
D10	PT48A	1	VREF1_1	T
G10	PT47B	1	PCLKC1_0	C
F11	PT47A	1	PCLKT1_0	T
G9	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
F9	PT46A	0	PCLKT0_0	T
C9	PT45B	0	VREF2_0	C

**LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)**

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF17	GND	-			GND	-			
AF25	GND	-			GND	-			
AF6	GND	-			GND	-			
AJ10	GND	-			GND	-			
AJ21	GND	-			GND	-			
AJ27	GND	-			GND	-			
AJ4	GND	-			GND	-			
AK1	GND	-			GND	-			
AK13	GND	-			GND	-			
AK18	GND	-			GND	-			
AK24	GND	-			GND	-			
AK30	GND	-			GND	-			
AK7	GND	-			GND	-			
B10	GND	-			GND	-			
B21	GND	-			GND	-			
B27	GND	-			GND	-			
B4	GND	-			GND	-			
D25	GND	-			GND	-			
D6	GND	-			GND	-			
E14	GND	-			GND	-			
E17	GND	-			GND	-			
F22	GND	-			GND	-			
F27	GND	-			GND	-			
F4	GND	-			GND	-			
F9	GND	-			GND	-			
G12	GND	-			GND	-			
G19	GND	-			GND	-			
J24	GND	-			GND	-			
J7	GND	-			GND	-			
K14	GND	-			GND	-			
K15	GND	-			GND	-			
K16	GND	-			GND	-			
K17	GND	-			GND	-			
K27	GND	-			GND	-			
K4	GND	-			GND	-			
L14	GND	-			GND	-			
L15	GND	-			GND	-			
L16	GND	-			GND	-			
L17	GND	-			GND	-			
M23	GND	-			GND	-			
M8	GND	-			GND	-			
N14	GND	-			GND	-			
N15	GND	-			GND	-			
N16	GND	-			GND	-			
N17	GND	-			GND	-			
N27	GND	-			GND	-			
N4	GND	-			GND	-			
P11	GND	-			GND	-			

**LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)**

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G7	PL8A	7	LDQ6	T (LVDS)*	NC	-			
G8	PL6A	7	LDQS6****	T (LVDS)*	NC	-			
G9	PL5A	7	LDQ6	T	NC	-			
H19	NC	-			NC	-			
H20	NC	-			NC	-			
H21	NC	-			NC	-			
H22	NC	-			NC	-			
H6	PL8B	7	LDQ6	C (LVDS)*	NC	-			
H8	PL5B	7	LDQ6	C	NC	-			
H9	PL2A	7	LDQ6	T (LVDS)*	NC	-			
J10	PL2B	7	LDQ6	C (LVDS)*	NC	-			
J20	NC	-			NC	-			
J21	NC	-			NC	-			
J9	PL4A	7	LDQ6	T (LVDS)*	NC	-			
K9	PL4B	7	LDQ6	C (LVDS)*	NC	-			
R9	NC	-			NC	-			
U22	NC	-			NC	-			
W9	NC	-			NC	-			
N13	VCCPLL	-			VCCPLL	-			
N18	VCCPLL	-			VCCPLL	-			
V13	VCCPLL	-			VCCPLL	-			
V18	VCCPLL	-			VCCPLL	-			

\* Supports true LVDS. Other differential signals must be emulated with external resistors.

\*\* These dedicated input pins can be used for GPLLS or GDLLs within the respective quadrant.

\*\*\* These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

\*\*\*\*Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

**LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)**

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLL_T_F_B_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLL_T_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLL_T_F_B_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLL_T_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

**LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)**

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA8	PL65A	6	LDQ64	T	PL73A	6	LDQ72	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y9	PL65B	6	LDQ64	C	PL73B	6	LDQ72	C
AA6	PL66A	6	LDQ64	T (LVDS)*	PL74A	6	LDQ72	T (LVDS)*
AA7	PL66B	6	LDQ64	C (LVDS)*	PL74B	6	LDQ72	C (LVDS)*
AA4	PL67A	6	LDQ64	T	PL75A	6	LDQ72	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA3	PL67B	6	LDQ64	C	PL75B	6	LDQ72	C
AA9	PL69A	6	LDQ73	T (LVDS)*	PL77A	6	LDQ81	T (LVDS)*
AA10	PL69B	6	LDQ73	C (LVDS)*	PL77B	6	LDQ81	C (LVDS)*
AA5	PL70A	6	LDQ73	T	PL78A	6	LDQ81	T
AB6	PL70B	6	LDQ73	C	PL78B	6	LDQ81	C
AB1	PL71A	6	LDQ73	T (LVDS)*	PL79A	6	LDQ81	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AB2	PL71B	6	LDQ73	C (LVDS)*	PL79B	6	LDQ81	C (LVDS)*
AC8	PL72A	6	LDQ73	T	PL80A	6	LDQ81	T
AB10	PL72B	6	LDQ73	C	PL80B	6	LDQ81	C
AC1	PL73A	6	LDQS73	T (LVDS)*	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AC2	PL73B	6	LDQ73	C (LVDS)*	PL81B	6	LDQ81	C (LVDS)*
AB7	PL74A	6	LDQ73	T	PL82A	6	LDQ81	T
AB5	PL74B	6	LDQ73	C	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6			VCCIO6	6		
AC3	PL75A	6	LDQ73	T (LVDS)*	PL83A	6	LDQ81	T (LVDS)*
AC4	PL75B	6	LDQ73	C (LVDS)*	PL83B	6	LDQ81	C (LVDS)*
AC10	PL76A	6	LDQ73	T	PL84A	6	LDQ81	T
AC9	PL76B	6	LDQ73	C	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-			GNDIO6	-		
AC7	NC	-			PL86A	6	LDQ90	T (LVDS)*
AC5	NC	-			PL86B	6	LDQ90	C (LVDS)*
AC6	NC	-			PL87A	6	LDQ90	T
AD5	NC	-			PL87B	6	LDQ90	C
-	-	-			VCCIO6	6		
AD4	NC	-			PL88A	6	LDQ90	T (LVDS)*
AD3	NC	-			PL88B	6	LDQ90	C (LVDS)*
AD10	NC	-			PL89A	6	LDQ90	T
AD8	NC	-			PL89B	6	LDQ90	C
-	-	-			GNDIO6	-		
AD2	NC	-			PL90A	6	LDQS90	T (LVDS)*
AD1	NC	-			PL90B	6	LDQ90	C (LVDS)*
AD9	NC	-			PL91A	6	LDQ90	T
-	-	-			VCCIO6	6		
AC11	NC	-			PL91B	6	LDQ90	C
AD6	NC	-			PL92A	6	LDQ90	T (LVDS)*
AD7	NC	-			PL92B	6	LDQ90	C (LVDS)*
AE1	NC	-			PL93A	6	LDQ90	T
-	-	-			GNDIO6	-		
AE2	NC	-			PL93B	6	LDQ90	C
AF2	PL78A	6	LDQ82	T (LVDS)*	PL95A	6	LDQ99	T (LVDS)*