Lattice Semiconductor Corporation - LFE2-6SE-6T144I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

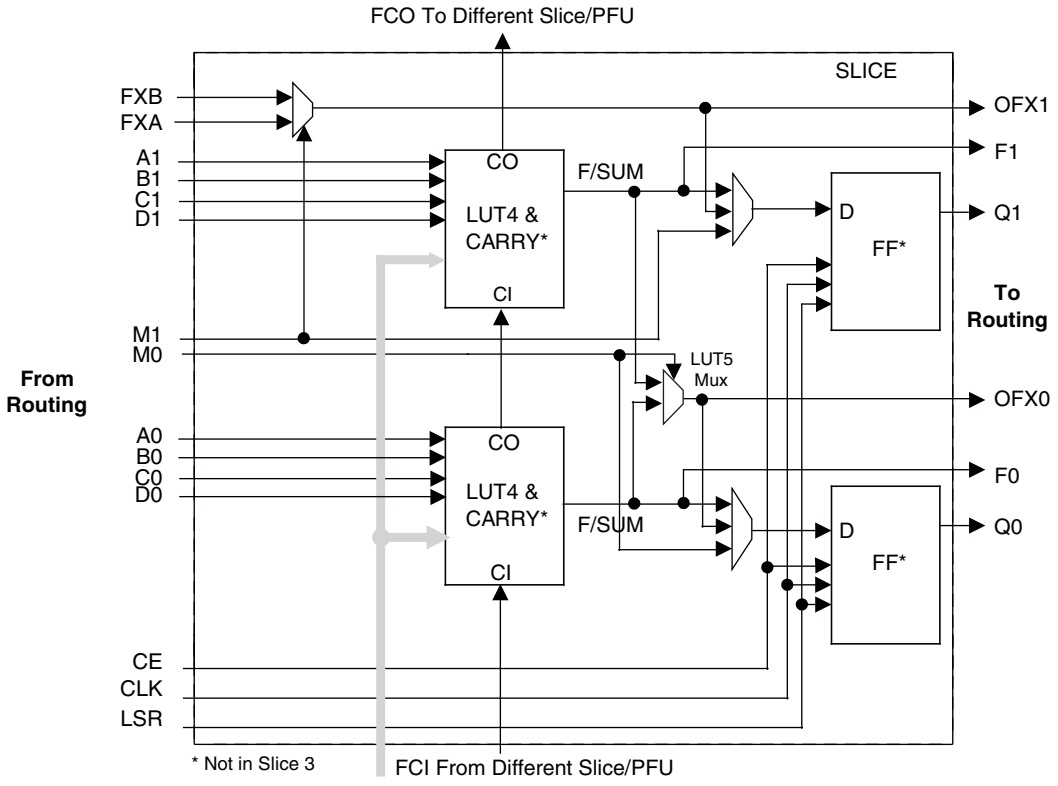
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	750
Number of Logic Elements/Cells	6000
Total RAM Bits	56320
Number of I/O	90
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-6se-6t144i

Figure 2-4. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
36x36 Multiplier (All Registers)	372	MHz
18x18 Multiplier/Accumulate (Input and Output Registers)	295	MHz
18x18 Multiplier-Add/Sub-Sum (All Registers)	420	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	304	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	227	MHz
8x8 Matrix Multiplier	223	MHz

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeECP2/M Internal Switching Characteristics[1] (Continued)

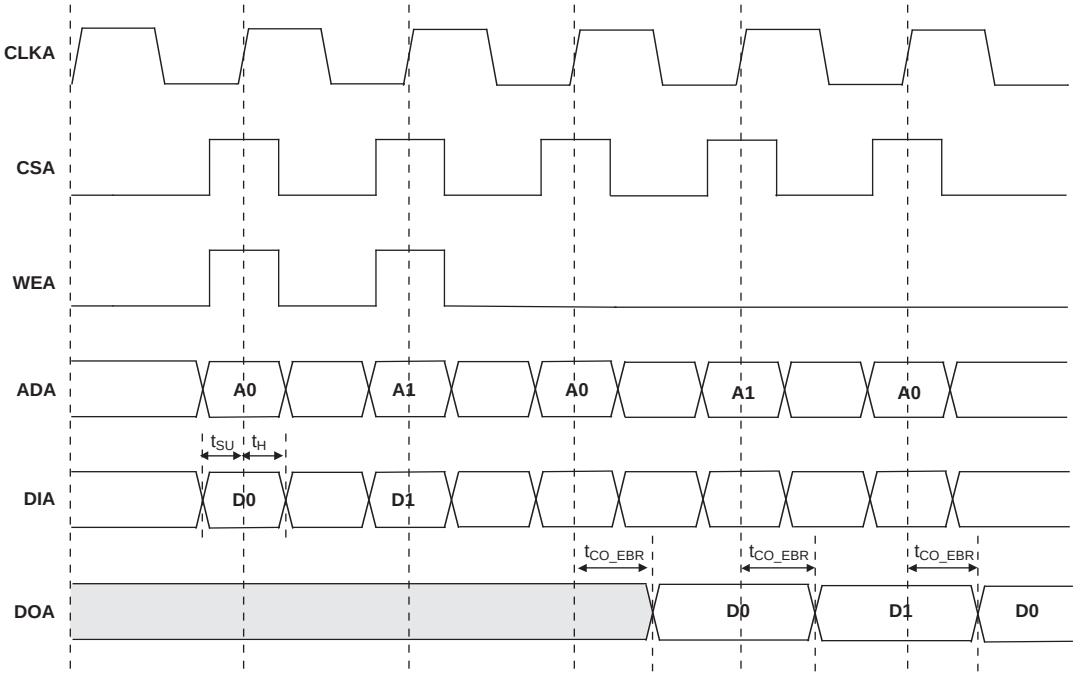
Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t_{RSTREC_SPLL}	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing[2,3]								
t_{SUI_DSP}	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t_{HI_DSP}	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t_{tHP_DSP}	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t_{SUO_DSP}	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
$t_{SUADDSUB}$	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
$t_{HADDSUB}$	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

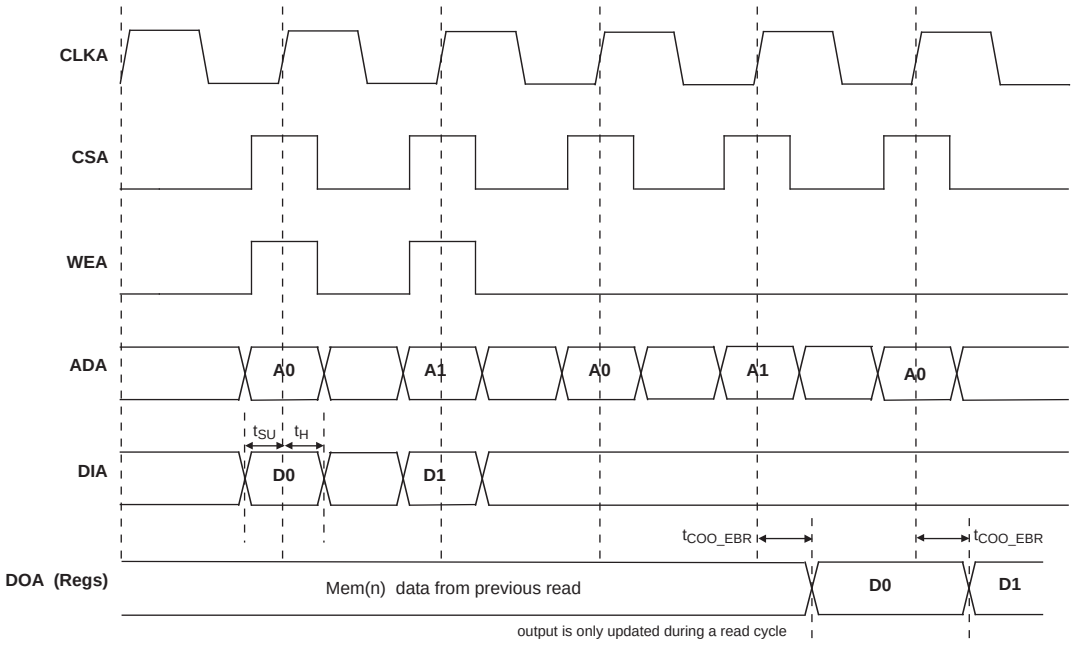
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI or SPIm mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating.
D[1:6]	I/O	sysCONFIG Port Data I/O for Parallel
D[7]/SPID0	I/O	sysCONFIG Port Data I/O for Parallel, SPI, SPIm
DOUT/CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPI0N	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes.
Dedicated SERDES Signals[1, 2, 3]		
[LOC]_SQ_VCCAUX33	—	Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused.
[LOC]_SQ_REFCLKN	I	Negative Reference Clock Input
[LOC]_SQ_REFCLKP	I	Positive Reference Clock Input
[LOC]_SQ_VCCP	—	PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused.

LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

Pin Type		LFE2-50		LFE2-70	
		484 fpBGA	672 fpBGA	672 fpBGA	900 fpBGA
Single Ended User I/O		339	500	500	583
Differential Pair User I/O		169	249	249	290
Configuration	TAP Pins	5	5	5	5
	Muxed Pins	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7
Non Configuration	Muxed Pins	68	79	79	89
	Dedicated Pins	3	3	3	3
VCC		16	20	20	26
VCCAUX		16	16	16	17
VCCPLL		4	4	2	4
VCCIO	Bank0	4	5	5	6
	Bank1	4	5	5	6
	Bank2	4	5	5	6
	Bank3	4	5	5	6
	Bank4	4	5	5	6
	Bank5	4	5	5	6
	Bank6	4	5	5	6
	Bank7	4	5	5	6
	Bank8	2	2	2	2
GND, GND0 to GND7		60	72	72	104
NC		0	3	5	101
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	50/25	67/33	67/33	84/42
	Bank1	46/23	66/33	66/33	76/38
	Bank2	38/19	56/28	56/28	74/37
	Bank3	22/11	48/24	48/24	48/24
	Bank4	46/23	62/31	62/31	72/35
	Bank5	46/23	68/34	68/34	80/40
	Bank6	40/20	64/32	64/32	64/32
	Bank7	37/18	55/27	55/27	71/35
	Bank8	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0
	Bank2 (Right Edge)	9	13	13	18
	Bank3 (Right Edge)	5	12	12	12
	Bank4 (Bottom Edge)	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0
	Bank6 (Left Edge)	10	16	16	16
	Bank7 (Left Edge)	8	12	12	16
	Bank8 (Right Edge)	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	L11	PB61B	4	BDQ60	C
T13	T13	PB62A	4	BDQ60	T
R13	R13	PB63A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
T14	T14	PB62B	4	BDQ60	C
P13	P13	PB63B	4	BDQ60	C
GND	GND	GNDIO4	-		
N12	N12	PB64A	4	VREF2_4/BDQ60	T
M12	M12	PB64B	4	VREF1_4/BDQ60	C
R15	R15	CFG2	8		
N14	N14	CFG1	8		
N13	N13	PROGRAMN	8		
N15	N15	CFG0	8		
P15	P15	PR44B	8	WRITEN	C
L12	L12	INITN	8		
N16	N16	PR43B	8	CSN	C
GND	GND	GNDIO8	-		
R14	R14	CCLK	8		
P14	P14	PR44A	8	CS1N	T
M13	M13	DONE	8		
R16	R16	PR42B	8	D1	C
VCCIO	VCCIO	VCCIO8	8		
M16	M16	PR43A	8	D0/SPIFASTN	T
P16	P16	PR42A	8	D2	T
L15	L15	PR41B	8	D3	C
GND	GND	GNDIO8	-		
L14	L14	PR40A	8	D6	T
L16	L16	PR41A	8	D4	T
L10	L10	PR39B	8	D7/SPID0	C
L13	L13	PR40B	8	D5	C
VCCIO	VCCIO	VCCIO8	8		
K11	K11	PR39A	8	DI/CSSPI0N	T
K14	K14	PR38B	8	DOUT/CSON	C
K13	K13	PR38A	8	BUSY/SISPI	T
GND	GND	GNDIO8	-		
K15	K15	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C
VCCIO	VCCIO	VCCIO3	3		
K16	K16	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
GND	GND	GNDIO3	-		
J16	J16	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
J15	J15	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
J14	J14	RLM0_PLLCAP	3		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		
V20	PROGRAMN	8			PROGRAMN	8		
W20	CFG0	8			CFG0	8		
U22	PR28B	8	D1	C	PR42B	8	D1	C
V22	INITN	8			INITN	8		
R16	PR30B	8	WRITEN	C	PR44B	8	WRITEN	C
GNDIO	GNDIO8	-			GNDIO8	-		
W22	CCLK	8			CCLK	8		
R17	PR30A	8	CS1N	T	PR44A	8	CS1N	T
V21	DONE	8			DONE	8		
VCCIO	VCCIO8	8			VCCIO8	8		
U19	PR29B	8	CSN	C	PR43B	8	CSN	C
T17	PR26B	8	D5	C	PR40B	8	D5	C
U20	PR29A	8	D0/SPIFASTN	T	PR43A	8	D0/SPIFASTN	T
U21	PR28A	8	D2	T	PR42A	8	D2	T
GNDIO	GNDIO8	-			GNDIO8	-		
T18	PR26A	8	D6	T	PR40A	8	D6	T
T20	PR27B	8	D3	C	PR41B	8	D3	C
T21	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
T19	PR27A	8	D4	T	PR41A	8	D4	T
VCCIO	VCCIO8	8			VCCIO8	8		
T22	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
R18	PR24B	8	DOUT/CSON	C	PR38B	8	DOUT/CSON	C
R19	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
-	-	-			VCCIO3	3		
GNDIO	GNDIO3	-			GNDIO3	-		
P18	PR22B	3		C (LVDS)*	PR32B	3	RDQ34	C (LVDS)*
R22	PR23B	3		C	PR33B	3	RDQ34	C
P19	PR22A	3		T (LVDS)*	PR32A	3	RDQ34	T (LVDS)*
R21	PR23A	3		T	PR33A	3	RDQ34	T
VCCIO	VCCIO3	3			VCCIO3	3		
R20	PR21B	3	RLM0_GPLLC_FB_A	C	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
P21	PR20B	3	RLM0_GPLLC_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLLC_IN_A**/RDQ34	C (LVDS)*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR18B	3	RLM0_GDLLC_FB_A	C	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
M22	PR17B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
N19	NC	-			PR26B	3	RDQ25	C
-	-	-			VCCIO3	3		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C2	PT3A	0		T	PT3A	0		T
J10	VCC	-			VCC	-		
J11	VCC	-			VCC	-		
J12	VCC	-			VCC	-		
J13	VCC	-			VCC	-		
K14	VCC	-			VCC	-		
K9	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L9	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M9	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N9	VCC	-			VCC	-		
P10	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
G10	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
H9	VCCIO0	0			VCCIO0	0		
H8	VCCIO0	0			VCCIO0	0		
G11	VCCIO1	1			VCCIO1	1		
G12	VCCIO1	1			VCCIO1	1		
G13	VCCIO1	1			VCCIO1	1		
G14	VCCIO1	1			VCCIO1	1		
H14	VCCIO2	2			VCCIO2	2		
H15	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K16	VCCIO2	2			VCCIO2	2		
L16	VCCIO3	3			VCCIO3	3		
M16	VCCIO3	3			VCCIO3	3		
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K1	PL23B	7	LDQ22	C	PL42B	7	LDQ41	C
L4	PL24A	7	LDQ22	T (LVDS)*	PL43A	7	LDQ41	T (LVDS)*
L3	PL24B	7	LDQ22	C (LVDS)*	PL43B	7	LDQ41	C (LVDS)*
L2	PL25A	7	PCLKT7_0/LDQ22	T	PL44A	7	PCLKT7_0/LDQ41	T
GNDIO	GNDIO7	-			GNDIO7	-		
L1	PL25B	7	PCLKC7_0/LDQ22	C	PL44B	7	PCLKC7_0/LDQ41	C
M5	PL27A	6	PCLKT6_0/LDQ31	T (LVDS)*	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*
M6	PL27B	6	PCLKC6_0/LDQ31	C (LVDS)*	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*
M3	PL28A	6	VREF2_6/LDQ31	T	PL47A	6	VREF2_6/LDQ50	T
M4	PL28B	6	VREF1_6/LDQ31	C	PL47B	6	VREF1_6/LDQ50	C
M2	PL29A	6	LDQ31	T (LVDS)*	PL48A	6	LDQ50	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	6		
M1	PL29B	6	LDQ31	C (LVDS)*	PL48B	6	LDQ50	C (LVDS)*
N1	PL30A	6	LDQ31	T	PL49A	6	LDQ50	T
N2	PL30B	6	LDQ31	C	PL49B	6	LDQ50	C
GNDIO	GNDIO6	-			GNDIO6	-		
VCCIO	VCCIO6	6			VCCIO	6		
N3	PL39A	6	LDQS39***	T (LVDS)*	PL58A	6	LDQS58***	T (LVDS)*
N4	PL39B	6	LDQ39	C (LVDS)*	PL58B	6	LDQ58	C (LVDS)*
N5	PL40A	6	LDQ39	T	PL59A	6	LDQ58	T
VCCIO	VCCIO6	6			VCCIO	6		
P5	PL40B	6	LDQ39	C	PL59B	6	LDQ58	C
P1	PL41A	6	LLM0_GDLLT_IN_A**/LDQ39	T (LVDS)*	PL60A	6	LLM0_GDLLT_IN_A**/LDQ58	T (LVDS)*
P2	PL41B	6	LLM0_GDLLC_IN_A**/LDQ39	C (LVDS)*	PL60B	6	LLM0_GDLLC_IN_A**/LDQ58	C (LVDS)*
P4	PL42A	6	LLM0_GDLLT_FB_A/LDQ39	T	PL61A	6	LLM0_GDLLT_FB_A/LDQ58	T
GNDIO	GNDIO6	-			GNDIO6	-		
R4	PL42B	6	LLM0_GDLLC_FB_A/LDQ39	C	PL61B	6	LLM0_GDLLC_FB_D/LDQ58	C
P6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
R1	PL44A	6	LLM0_GPLLT_IN_A**/LDQ48	T (LVDS)*	PL63A	6	LLM0_GPLLT_IN_A**/LDQ67	T (LVDS)*
R2	PL44B	6	LLM0_GPLLC_IN_A**/LDQ48	C (LVDS)*	PL63B	6	LLM0_GPLLC_IN_A**/LDQ67	C (LVDS)*
R3	PL45A	6	LLM0_GPLLT_FB_A/LDQ48	T	PL64A	6	LLM0_GPLLT_FB_A/LDQ67	T
T4	PL45B	6	LLM0_GPLLC_FB_A/LDQ48	C	PL64B	6	LLM0_GPLLC_FB_A/LDQ67	C
T1	PL46A	6	LDQ48	T (LVDS)*	PL65A	6	LDQ67	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	6		
T2	PL46B	6	LDQ48	C (LVDS)*	PL65B	6	LDQ67	C (LVDS)*
T5	PL47A	6	LDQ48	T	PL66A	6	LDQ67	T
T3	PL47B	6	LDQ48	C	PL66B	6	LDQ67	C
GNDIO	GNDIO6	-			VCCIO	6		
VCCIO	VCCIO6	-			GNDIO6	-		
U1	PL52A	6	LDQ56	T (LVDS)*	PL71A	6	LDQ75	T (LVDS)*
U2	PL52B	6	LDQ56	C (LVDS)*	PL71B	6	LDQ75	C (LVDS)*
V1	PL53A	6	LDQ56	T	PL72A	6	LDQ75	T
V2	PL53B	6	LDQ56	C	PL72B	6	LDQ75	C
VCCIO	VCCIO6	6			VCCIO	6		
R6	PL54A	6	LDQ56	T (LVDS)*	PL73A	6	LDQ75	T (LVDS)*
T6	PL54B	6	LDQ56	C (LVDS)*	PL73B	6	LDQ75	C (LVDS)*

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA14	PB29B	5	BDQ33	C	PB29B	5	BDQ33	C
AE10	PB30A	5	BDQ33	T	PB30A	5	BDQ33	T
AF10	PB30B	5	BDQ33	C	PB30B	5	BDQ33	C
W14	PB31A	5	BDQ33	T	PB31A	5	BDQ33	T
AB13	PB31B	5	BDQ33	C	PB31B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y14	PB32A	5	BDQ33	T	PB32A	5	BDQ33	T
AB14	PB32B	5	BDQ33	C	PB32B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AE11	PB33A	5	BDQS33	T	PB33A	5	BDQS33	T
AF11	PB33B	5	BDQ33	C	PB33B	5	BDQ33	C
AD14	PB34A	5	BDQ33	T	PB34A	5	BDQ33	T
AA15	PB34B	5	BDQ33	C	PB34B	5	BDQ33	C
AE12	PB35A	5	PCLKT5_0/BDQ33	T	PB35A	5	PCLKT5_0/BDQ33	T
AF12	PB35B	5	PCLKC5_0/BDQ33	C	PB35B	5	PCLKC5_0/BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GND	GNDIO5	-			GNDIO5	-		
AD15	PB40A	4	PCLKT4_0/BDQ42	T	PB40A	4	PCLKT4_0/BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AC15	PB40B	4	PCLKC4_0/BDQ42	C	PB40B	4	PCLKC4_0/BDQ42	C
AE13	PB41A	4	BDQ42	T	PB41A	4	BDQ42	T
AF13	PB41B	4	BDQ42	C	PB41B	4	BDQ42	C
AB17	PB42A	4	BDQS42	T	PB42A	4	BDQS42	T
GND	GNDIO4	-			GNDIO4	-		
Y15	PB42B	4	BDQ42	C	PB42B	4	BDQ42	C
AE14	PB43A	4	BDQ42	T	PB43A	4	BDQ42	T
AF14	PB43B	4	BDQ42	C	PB43B	4	BDQ42	C
AA16	PB44A	4	BDQ42	T	PB44A	4	BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
W15	PB44B	4	BDQ42	C	PB44B	4	BDQ42	C
AC17	PB45A	4	BDQ42	T	PB45A	4	BDQ42	T
AB16	PB45B	4	BDQ42	C	PB45B	4	BDQ42	C
AE15	PB46A	4	BDQ42	T	PB46A	4	BDQ42	T
GND	GNDIO4	-			GNDIO4	-		
AF15	PB46B	4	BDQ42	C	PB46B	4	BDQ42	C
AE16	PB47A	4	BDQ51	T	PB47A	4	BDQ51	T
AF16	PB47B	4	BDQ51	C	PB47B	4	BDQ51	C
Y16	PB48A	4	BDQ51	T	PB48A	4	BDQ51	T
AB18	PB48B	4	BDQ51	C	PB48B	4	BDQ51	C
AD17	PB49A	4	BDQ51	T	PB49A	4	BDQ51	T
AD18	PB49B	4	BDQ51	C	PB49B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
AC18	PB50A	4	BDQ51	T	PB50A	4	BDQ51	T
AD19	PB50B	4	BDQ51	C	PB50B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
AC19	PB51A	4	BDQS51	T	PB51A	4	BDQS51	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AB24	PR87B	8	D3	C
GND	GNDIO4	-		
AB23	PR87A	8	D4	T
AB25	PR86B	8	D5	C
AB26	PR86A	8	D6	T
AC27	PR85B	8	D7/SPID0	C
VCCIO	VCCIO8	8		
AB27	PR85A	8	DI/CSSPI0N	T
AD29	PR84B	8	DOUT/CSON	C
AD30	PR84A	8	BUSY/SISPI	T
AA25	PR83B	3	RDQ80	C
GND	GNDIO3	-		
AA23	PR83A	3	RDQ80	T
AC29	PR82B	3	RDQ80	C (LVDS)*
AC30	PR82A	3	RDQ80	T (LVDS)*
AA26	PR81B	3	RDQ80	C
VCCIO	VCCIO3	3		
AA24	PR81A	3	RDQ80	T
AB29	PR80B	3	RDQ80	C (LVDS)*
AB30	PR80A	3	RDQS80	T (LVDS)*
GND	GNDIO3	-		
Y23	PR79B	3	RDQ80	C
Y25	PR79A	3	RDQ80	T
AA27	PR78B	3	RDQ80	C (LVDS)*
AA28	PR78A	3	RDQ80	T (LVDS)*
VCCIO	VCCIO3	3		
Y24	PR77B	3	RLM0_GPLLC_FB_A/RDQ80	C
Y26	PR77A	3	RLM0_GPLLT_FB_A/RDQ80	T
AA29	PR76B	3	RLM0_GPLLC_IN_A**/RDQ80	C (LVDS)*
AA30	PR76A	3	RLM0_GPLLT_IN_A**/RDQ80	T (LVDS)*
R22	RLM0_PLLCAP	3		
W23	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C
W25	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T
GND	GNDIO3	-		
Y27	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*
Y28	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*
W24	PR72B	3	RDQ71	C
W26	PR72A	3	RDQ71	T
VCCIO	VCCIO3	3		
Y29	PR71B	3	RDQ71	C (LVDS)*
Y30	PR71A	3	RDQS71	T (LVDS)*
V25	PR70B	3	RDQ71	C
GND	GNDIO3	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
T7	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
T8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C
L7	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T
L8	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
P8	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T
N8	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C
R7	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T
R8	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C
N7	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T
M8	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
R9	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T
T9	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C
GNDIO	GNDIO4	-			GNDIO4	-		
T10	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T
R10	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C
N9	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T
P10	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
L9	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T
M9	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C
T11	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T
R11	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
T12	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T
T13	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
P11	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T
N10	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C
T14	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T
R13	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C
R15	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T
R16	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
R14	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T
P15	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C
P16	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T
P14	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
L11	CFG2	8			CFG2	8		
L10	CFG1	8			CFG1	8		
P13	CFG0	8			CFG0	8		
N12	PROGRAMN	8			PROGRAMN	8		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
F20	PR30A	2	RDQ27	T
GNDIO	GNDIO2	-		
G17	PR29B	2	RDQ27	C (LVDS)*
F17	PR29A	2	RDQ27	T (LVDS)*
VCCIO	VCCIO2	2		
GNDIO	GNDIO2	-		
E22	PR14B	2		C
D22	PR14A	2		T
VCCIO	VCCIO2	-		
E20	PR13B	2		C (LVDS)*
D20	PR13A	2		T (LVDS)*
D19	PR12B	2	RUM0_SPLLC_FB_A	C
GNDIO	GNDIO2	-		
E19	PR12A	2	RUM0_SPLLT_FB_A	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*
F19	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*
VCCIO	VCCIO2	-		
E18	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-		
D18	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
F16	XRES	-		
C22	URC_SQ_VCCRX0	12		
A21	URC_SQ_HDINP0	12		T
B22	URC_SQ_VCCIB0	12		
B21	URC_SQ_HDINN0	12		C
C19	URC_SQ_VCCTX0	12		
A18	URC_SQ_HDOUTP0	12		T
A19	URC_SQ_VCCOB0	12		
B18	URC_SQ_HDOUTN0	12		C
C18	URC_SQ_VCCTX1	12		
B17	URC_SQ_HDOUTN1	12		C
C17	URC_SQ_VCCOB1	12		
A17	URC_SQ_HDOUTP1	12		T
C21	URC_SQ_VCCRX1	12		
B20	URC_SQ_HDINN1	12		C
C20	URC_SQ_VCCIB1	12		
A20	URC_SQ_HDINP1	12		T
B16	URC_SQ_VCCAUX33	12		
E17	URC_SQ_REFCLKN	12		C
D17	URC_SQ_REFCLKP	12		T
C16	URC_SQ_VCCP	12		
A12	URC_SQ_HDINP2	12		T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AJ17	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AF26	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T
AE25	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
AD24	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T
AE24	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C
AD18	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AC18	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
AE18	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
AG19	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
AC19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
AD20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
AB18	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
AC20	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
AE20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
AE21	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO4	4		
AC23	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
AD23	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
AH18	LRC_SQ_VCCRX3	13			LRC_SQ_VCCRX3	13		
AK19	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T
AK21	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C
AH22	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C
AH23	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T
AH19	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AJ20	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AK25	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AA1	PL81A	6	LDQS81	T (LVDS)*
GNDIO	GNDIO6	-		
AA2	PL81B	6	LDQ81	C (LVDS)*
Y3	PL82A	6	LDQ81	T
AB1	PL82B	6	LDQ81	C
VCCIO	VCCIO6	6		
Y9	PL83A	6	LDQ81	T (LVDS)*
Y8	PL83B	6	LDQ81	C (LVDS)*
Y7	PL84A	6	LDQ81	T
AA7	PL84B	6	LDQ81	C
GNDIO	GNDIO6	-		
VCCIO	VCCIO6	6		
AB2	PL95A	6	LDQ99	T (LVDS)*
AB3	PL95B	6	LDQ99	C (LVDS)*
AA5	PL96A	6	LDQ99	T
AA6	PL96B	6	LDQ99	C
AB4	PL97A	6	LDQ99	T (LVDS)*
VCCIO	VCCIO6	6		
AB5	PL97B	6	LDQ99	C (LVDS)*
AA8	PL98A	6	LDQ99	T
AA9	PL98B	6	LDQ99	C
AC1	PL99A	6	LLM0_GPLLT_IN_A**/LDQS99	T (LVDS)*
GNDIO	GNDIO6	-		
AC2	PL99B	6	LLM0_GPLLC_IN_A**/LDQ99	C (LVDS)*
AC4	PL100A	6	LLM0_GPLLT_FB_A/LDQ99	T
AC3	PL100B	6	LLM0_GPLLC_FB_A/LDQ99	C
VCCIO	VCCIO6	6		
AC7	PL101A	6	LLM0_GDLLT_IN_A**/LDQ99	T (LVDS)*
AC6	PL101B	6	LLM0_GDLLC_IN_A**/LDQ99	C (LVDS)*
AC5	PL102A	6	LLM0_GDLLT_FB_A/LDQ99	T
AD3	PL102B	6	LLM0_GDLLC_FB_A/LDQ99	C
GNDIO	GNDIO6	-		
AB8	LLM0_PLLCAP	6		
AD2	PL104A	6		T
AD1	PL104B	6		C
AE2	TCK	-		
AE1	TDI	-		
AF2	TMS	-		
AF1	TDO	-		
AG1	VCCJ	-		
AH1	LLC_SQ_VCCRX3	14		
AK2	LLC_SQ_HDINP3	14		T
AJ1	LLC_SQ_VCCIB3	14		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF1	PL78B	6	LDQ82	C (LVDS)*	PL95B	6	LDQ99	C (LVDS)*
AE5	PL79A	6	LDQ82	T	PL96A	6	LDQ99	T
AE6	PL79B	6	LDQ82	C	PL96B	6	LDQ99	C
AF4	PL80A	6	LDQ82	T (LVDS)*	PL97A	6	LDQ99	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AF3	PL80B	6	LDQ82	C (LVDS)*	PL97B	6	LDQ99	C (LVDS)*
AF5	PL81A	6	LDQ82	T	PL98A	6	LDQ99	T
AF6	PL81B	6	LDQ82	C	PL98B	6	LDQ99	C
AG1	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	PL99A	6	LLM0_GPLLT_IN_A**/ LDQS99	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AG2	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	PL99B	6	LLM0_GPLLC_IN_A**/LDQ99	C (LVDS)*
AE9	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	PL100A	6	LLM0_GPLLT_FB_A/LDQ99	T
AF7	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	PL100B	6	LLM0_GPLLC_FB_A/LDQ99	C
VCCIO	VCCIO6	6			VCCIO6	6		
AH1	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	PL101A	6	LLM0_GDLLT_IN_A**/LDQ99	T (LVDS)*
AH2	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	PL101B	6	LLM0_GDLLC_IN_A**/ LDQ99	C (LVDS)*
AG5	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	PL102A	6	LLM0_GDLLT_FB_A/LDQ99	T
AG4	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	PL102B	6	LLM0_GDLLC_FB_A/LDQ99	C
GNDIO	GNDIO6	-			GNDIO6	-		
AG6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
AJ1	PL87A	6		T	PL104A	6		T
AJ2	PL87B	6		C	PL104B	6		C
AK2	TCK	-			TCK	-		
AK1	TDI	-			TDI	-		
AL1	TMS	-			TMS	-		
AF10	TDO	-			TDO	-		
AK3	VCCJ	-			VCCJ	-		
AN2	LLC_SQ_VCCRX3	14			LLC_SQ_VCCRX3	14		
AM2	LLC_SQ_HDINP3	14		T	LLC_SQ_HDINP3	14		T
AN1	LLC_SQ_VCCIB3	14			LLC_SQ_VCCIB3	14		
AM3	LLC_SQ_HDINN3	14		C	LLC_SQ_HDINN3	14		C
AN3	LLC_SQ_VCCTX3	14			LLC_SQ_VCCTX3	14		
AP2	LLC_SQ_HDOUTP3	14		T	LLC_SQ_HDOUTP3	14		T
AM1	LLC_SQ_VCCOB3	14			LLC_SQ_VCCOB3	14		
AP3	LLC_SQ_HDOUTN3	14		C	LLC_SQ_HDOUTN3	14		C
AN4	LLC_SQ_VCCTX2	14			LLC_SQ_VCCTX2	14		
AP4	LLC_SQ_HDOUTN2	14		C	LLC_SQ_HDOUTN2	14		C
AL3	LLC_SQ_VCCOB2	14			LLC_SQ_VCCOB2	14		
AP5	LLC_SQ_HDOUTP2	14		T	LLC_SQ_HDOUTP2	14		T
AN5	LLC_SQ_VCCRX2	14			LLC_SQ_VCCRX2	14		
AM4	LLC_SQ_HDINN2	14		C	LLC_SQ_HDINN2	14		C
AL4	LLC_SQ_VCCIB2	14			LLC_SQ_VCCIB2	14		
AM5	LLC_SQ_HDINP2	14		T	LLC_SQ_HDINP2	14		T
AL6	LLC_SQ_VCCP	14			LLC_SQ_VCCP	14		
AL5	LLC_SQ_REFCLKP	14		T	LLC_SQ_REFCLKP	14		T
AK5	LLC_SQ_REFCLKN	14		C	LLC_SQ_REFCLKN	14		C
AK6	LLC_SQ_VCCAUX33	14			LLC_SQ_VCCAUX33	14		
AM6	LLC_SQ_HDINP1	14		T	LLC_SQ_HDINP1	14		T

LatticeECP2/M Family Data Sheet Revision History

September 2013 **Data Sheet DS1006**

Date	Version	Section	Change Summary
February 2006	01.0	—	Initial release.
August 2006	01.1	Introduction	
			Updated Table 1-1 “LatticeECP2 Family Selection Guide”.
		Architecture	Updated Figure 2-2 “PFU Diagram”.
			Updated Figure 2-13 “Secondary Clock Regions ECP2-50”.
			Updated Figure 2-25 “PIC Diagram”.
			Updated Figure 2-26 “Input Register Block for Left, Right and Bottom Edges”.
			Updated Figure 2-28 “Output Register Block for Left, Right and Bottom Edges”.
			Updated Figure 2-30 “DQS Input Routing for Left and Right Edges”.
			Updated Figure 2-32 “Edge Clock, DLL Calibration and DQS Local Bus Distribution”.
			Table 2-15 Selectable Master Clock (CCLK) Frequencies - Removed frequencies 15, 20, 21, 22, 23, 30, 34, 41, 45, 51, 55, 60.
			Replaced “CLKINDEL” with “CLKO”.
			Updated SED section.
			Qualified device migration capability when using DQS banks for DDR interfaces.
		DC and Switching Characteristics	Added VCCPLL to the Recommended Operating Conditions table.
			Removed note 5 from “Hot Specifications” section.
			Added notes 7 and 8 to “Initialization Supply” Current table.
			Change note 6 - “...down to 95MHz” to “...down to 95MHz for DDR and 133MHz for DDR2” .
			New “Typical Building Block Function Performance” numbers.
			New External Switching Characteristics numbers.
			New Internal Switching Characteristics numbers.
			New Family Timing Adders numbers.
			Updated Timings for GPLLs, SPLLs and DLLs.
			Added sysCONFIG waveforms.
			Remove HSTL15D_II from sysIO Recommended Operating Conditions table.
			Updated Supply and Initialization Currents for ECP2-50.
		Pinout Information	Added VCCPLL to the Signal Descriptions table.
			Updated Logic Signal Connections tables to include 484-fpBGA for the ECP2-50.
			Added Logic Signal Connections tables for ECP2-12 devices.
			Updated Pin Information Summary table to include ECP2-12.
			Updated Power Supply and NC Connections table to include ECP2-12.
			Added note 2 to DDR Strobe (DQS) Pin table.
			Added Information on: PCI, DDR & SPI4.2 Capabilities of the device-Package combination.

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL}, I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT}.
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.