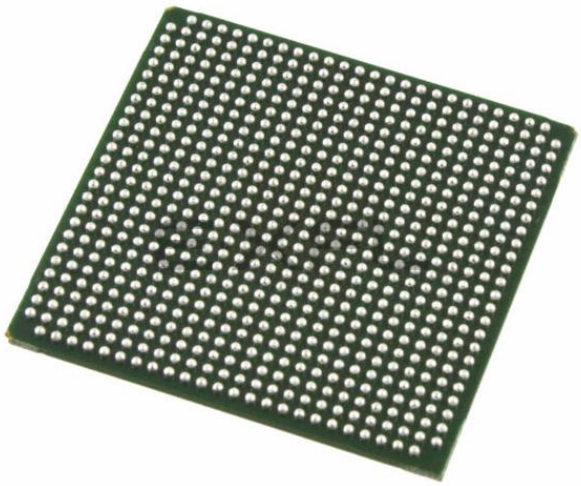
# Lattice Semiconductor Corporation - LFE2-70E-5FN672I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 8500 |
| Number of Logic Elements/Cells | 68000 |
| Total RAM Bits | 1056768 |
| Number of I/O | 500 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70e-5fn672i |

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

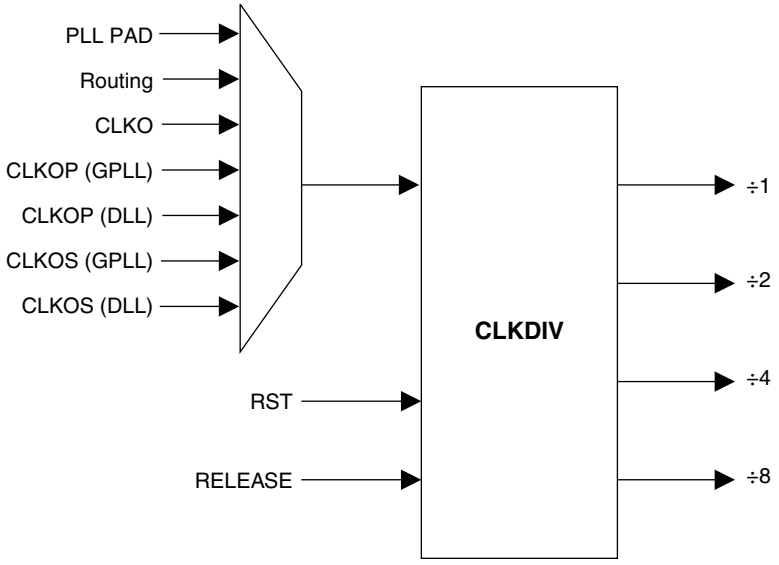
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP2/M devices, please see the list of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required to Implement Distributed RAM***

| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

*Figure 2-9. Clock Divider Connections*




## Clock Distribution Network

LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

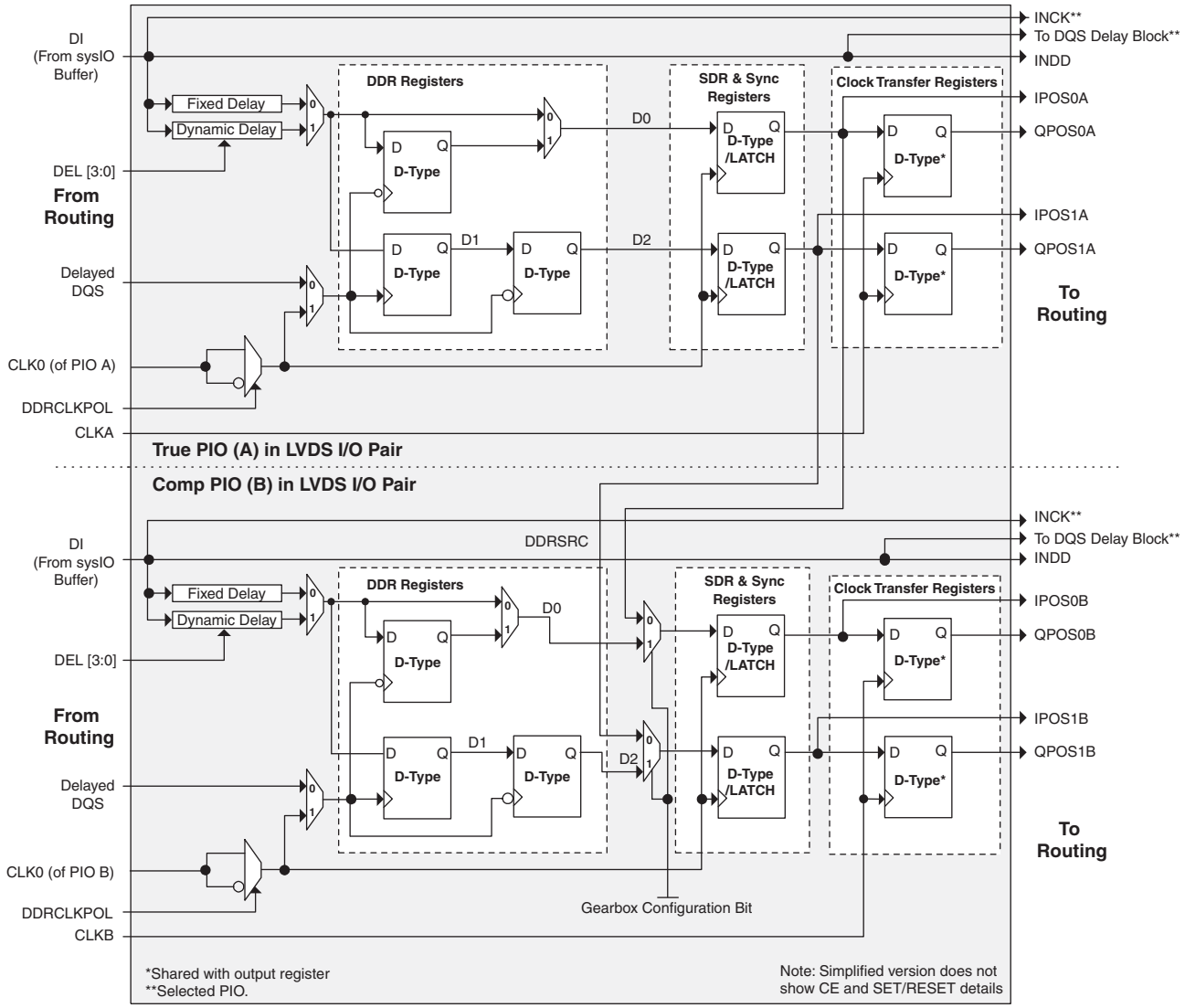
### Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

***Figure 2-29. Input Register Block for Left, Right and Bottom Edges***



## Signal Descriptions (Cont.)

| Signal Name | I/O | Description |
|---|---|---|
| [LOC]DQS[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number. |
| [LOC]DQ[num] | I/O | DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number. |
| **Test and Programming (Dedicated Pins)** | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |
| TDO | O | Output pin. Test Data Out pin used to shift data out of a device using 1149.1. |
| VCCJ | — | Power supply pin for JTAG Test Access Port. |
| **Configuration Pads** (Used During sysCONFIG) | | |
| CFG[2:0] | I | Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY/SISPI | I/O | Read control command in SPI or SPIm mode. |
| CSN | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| CS1N | I | sysCONFIG chip select (active low). During configuration, a pull-up is enabled. |
| WRITEN | I | Write Data on Parallel port (active low). |
| D[0]/SPIFASTN | I/O | sysCONFIG Port Data I/O for Parallel mode.<br>sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. |
| D[1:6] | I/O | sysCONFIG Port Data I/O for Parallel |
| D[7]/SPID0 | I/O | sysCONFIG Port Data I/O for Parallel, SPI, SPIm |
| DOUT/CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. |
| DI/CSSPI0N | I/O | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes. |
| **Dedicated SERDES Signals**[1, 2, 3] | | |
| [LOC]_SQ_VCCAUX33 | — | Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused. |
| [LOC]_SQ_REFCLKN | I | Negative Reference Clock Input |
| [LOC]_SQ_REFCLKP | I | Positive Reference Clock Input |
| [LOC]_SQ_VCCP | — | PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused. |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M8 | PB8B | 5 | PCLKC5_0/BDQ6 | C | PB26B | 5 | PCLKC5_0/BDQ24 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| P7 | PB13A | 4 | PCLKT4_0/BDQ15 | T | PB31A | 4 | PCLKT4_0/BDQ33 | T |
| R8 | PB13B | 4 | PCLKC4_0/BDQ15 | C | PB31B | 4 | PCLKC4_0/BDQ33 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T5 | PB14A | 4 | BDQ15 | T | PB32A | 4 | BDQ33 | T |
| T6 | PB14B | 4 | BDQ15 | C | PB32B | 4 | BDQ33 | C |
| T8 | PB15A | 4 | BDQS15 | T | PB33A | 4 | BDQS33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R7 | PB16A | 4 | BDQ15 | T | PB34A | 4 | BDQ33 | T |
| T9 | PB15B | 4 | BDQ15 | C | PB33B | 4 | BDQ33 | C |
| T7 | PB16B | 4 | BDQ15 | C | PB34B | 4 | BDQ33 | C |
| L8 | PB17A | 4 | BDQ15 | T | PB35A | 4 | BDQ33 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| P8 | PB18A | 4 | BDQ15 | T | PB36A | 4 | BDQ33 | T |
| L9 | PB17B | 4 | BDQ15 | C | PB35B | 4 | BDQ33 | C |
| N8 | PB18B | 4 | BDQ15 | C | PB36B | 4 | BDQ33 | C |
| R9 | PB19A | 4 | BDQ15 | T | PB37A | 4 | BDQ33 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| R10 | PB19B | 4 | BDQ15 | C | PB37B | 4 | BDQ33 | C |
| - | - | - | | | VCCIO | 4 | | |
| - | - | - | | | GNDIO4 | 4 | | |
| N9 | PB20A | 4 | BDQ24 | T | PB47A | 4 | BDQ51 | T |
| T10 | PB21A | 4 | BDQ24 | T | PB48A | 4 | BDQ51 | T |
| M9 | PB20B | 4 | BDQ24 | C | PB47B | 4 | BDQ51 | C |
| R11 | PB21B | 4 | BDQ24 | C | PB48B | 4 | BDQ51 | C |
| P10 | PB22A | 4 | BDQ24 | T | PB49A | 4 | BDQ51 | T |
| N11 | PB23A | 4 | BDQ24 | T | PB50A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| N10 | PB22B | 4 | BDQ24 | C | PB49B | 4 | BDQ51 | C |
| P11 | PB23B | 4 | BDQ24 | C | PB50B | 4 | BDQ51 | C |
| T11 | PB24A | 4 | BDQS24 | T | PB51A | 4 | BDQS51 | T |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| M11 | PB25A | 4 | BDQ24 | T | PB52A | 4 | BDQ51 | T |
| T12 | PB24B | 4 | BDQ24 | C | PB51B | 4 | BDQ51 | C |
| L11 | PB25B | 4 | BDQ24 | C | PB52B | 4 | BDQ51 | C |
| T13 | PB26A | 4 | BDQ24 | T | PB53A | 4 | BDQ51 | T |
| R13 | PB27A | 4 | BDQ24 | T | PB54A | 4 | BDQ51 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| T14 | PB26B | 4 | BDQ24 | C | PB53B | 4 | BDQ51 | C |
| P13 | PB27B | 4 | BDQ24 | C | PB54B | 4 | BDQ51 | C |
| GND | GNDIO4 | - | | | GNDIO4 | - | | |
| N12 | PB28A | 4 | VREF2_4/BDQ24 | T | PB55A | 4 | VREF2_4/BDQ51 | T |
| M12 | PB28B | 4 | VREF1_4/BDQ24 | C | PB55B | 4 | VREF1_4/BDQ51 | C |
| R15 | CFG2 | 8 | | | CFG2 | 8 | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D15 | PT52A | 1 | | T | PT61A | 1 | | T |
| E15 | PT51B | 1 | | C | PT60B | 1 | | C |
| F15 | PT51A | 1 | | T | PT60A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B15 | PT49B | 1 | | C | PT58B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| A15 | PT49A | 1 | | T | PT58A | 1 | | T |
| B14 | PT48B | 1 | | C | PT57B | 1 | | C |
| A14 | PT48A | 1 | | T | PT57A | 1 | | T |
| D14 | PT46B | 1 | | C | PT55B | 1 | | C |
| C13 | PT46A | 1 | | T | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E14 | PT45B | 1 | | C | PT54B | 1 | | C |
| F14 | PT45A | 1 | | T | PT54A | 1 | | T |
| A13 | PT44B | 1 | | C | PT53B | 1 | | C |
| B13 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| E13 | PT43B | 1 | | C | PT52B | 1 | | C |
| D13 | PT43A | 1 | | T | PT52A | 1 | | T |
| E12 | PT42B | 1 | | C | PT51B | 1 | | C |
| D12 | PT42A | 1 | | T | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A12 | PT40B | 1 | | C | PT49B | 1 | | C |
| A11 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| B12 | PT39B | 1 | PCLKC1_0 | C | PT48B | 1 | PCLKC1_0 | C |
| C12 | PT39A | 1 | PCLKT1_0 | T | PT48A | 1 | PCLKT1_0 | T |
| F12 | XRES | 1 | | | XRES | 1 | | |
| B10 | PT37B | 0 | PCLKC0_0 | C | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B11 | PT37A | 0 | PCLKT0_0 | T | PT46A | 0 | PCLKT0_0 | T |
| A10 | PT36B | 0 | | C | PT45B | 0 | | C |
| A9 | PT36A | 0 | | T | PT45A | 0 | | T |
| C11 | PT35B | 0 | | C | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| C10 | PT35A | 0 | | T | PT44A | 0 | | T |
| E11 | PT34B | 0 | | C | PT43B | 0 | | C |
| F11 | PT34A | 0 | | T | PT43A | 0 | | T |
| A8 | PT33B | 0 | | C | PT42B | 0 | | C |
| A7 | PT33A | 0 | | T | PT42A | 0 | | T |
| B8 | PT32B | 0 | | C | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B9 | PT32A | 0 | | T | PT41A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| B7 | PT30B | 0 | | C | PT39B | 0 | | C |
| A6 | PT30A | 0 | | T | PT39A | 0 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A7 | PT35B | 0 | | C | PT44B | 0 | | C |
| B7 | PT35A | 0 | | T | PT44A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F12 | PT34B | 0 | | C | PT43B | 0 | | C |
| D10 | PT34A | 0 | | T | PT43A | 0 | | T |
| H11 | PT33B | 0 | | C | PT42B | 0 | | C |
| G11 | PT33A | 0 | | T | PT42A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| A6 | PT32B | 0 | | C | PT41B | 0 | | C |
| B6 | PT32A | 0 | | T | PT41A | 0 | | T |
| D8 | PT31B | 0 | | C | PT40B | 0 | | C |
| C8 | PT31A | 0 | | T | PT40A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F11 | PT30B | 0 | | C | PT39B | 0 | | C |
| E10 | PT30A | 0 | | T | PT39A | 0 | | T |
| E9 | PT29B | 0 | | C | PT38B | 0 | | C |
| D9 | PT29A | 0 | | T | PT38A | 0 | | T |
| G10 | PT28B | 0 | | C | PT37B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H10 | PT28A | 0 | | T | PT37A | 0 | | T |
| A5 | PT27B | 0 | | C | PT36B | 0 | | C |
| B5 | PT27A | 0 | | T | PT36A | 0 | | T |
| C7 | PT26B | 0 | | C | PT35B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D7 | PT26A | 0 | | T | PT35A | 0 | | T |
| E8 | PT25B | 0 | | C | PT34B | 0 | | C |
| F10 | PT25A | 0 | | T | PT34A | 0 | | T |
| F8 | PT24B | 0 | | C | PT33B | 0 | | C |
| H9 | PT24A | 0 | | T | PT33A | 0 | | T |
| C5 | PT23B | 0 | | C | PT32B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| D5 | PT23A | 0 | | T | PT32A | 0 | | T |
| B4 | PT22B | 0 | | | PT31B | 0 | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| C4 | PT10B | 0 | | C | PT10B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C3 | PT10A | 0 | | T | PT10A | 0 | | T |
| A4 | PT9B | 0 | | C | PT9B | 0 | | C |
| A3 | PT9A | 0 | | T | PT9A | 0 | | T |
| B3 | PT8B | 0 | | C | PT8B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| B2 | PT8A | 0 | | T | PT8A | 0 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| AG4 | NC | - | | |
| AG8 | NC | - | | |
| AH1 | NC | - | | |
| AH16 | NC | - | | |
| AH2 | NC | - | | |
| AH26 | NC | - | | |
| AH27 | NC | - | | |
| AH29 | NC | - | | |
| AH30 | NC | - | | |
| AH4 | NC | - | | |
| AJ1 | NC | - | | |
| AJ2 | NC | - | | |
| AJ27 | NC | - | | |
| AJ28 | NC | - | | |
| AJ29 | NC | - | | |
| AJ3 | NC | - | | |
| AJ30 | NC | - | | |
| AK2 | NC | - | | |
| AK27 | NC | - | | |
| AK28 | NC | - | | |
| AK29 | NC | - | | |
| AK3 | NC | - | | |
| B1 | NC | - | | |
| B2 | NC | - | | |
| B3 | NC | - | | |
| B30 | NC | - | | |
| B4 | NC | - | | |
| B5 | NC | - | | |
| C1 | NC | - | | |
| C2 | NC | - | | |
| C29 | NC | - | | |
| C30 | NC | - | | |
| C4 | NC | - | | |
| D13 | NC | - | | |
| D18 | NC | - | | |
| D23 | NC | - | | |
| D28 | NC | - | | |
| D29 | NC | - | | |
| D3 | NC | - | | |
| D30 | NC | - | | |
| D4 | NC | - | | |
| E25 | NC | - | | |
| E26 | NC | - | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F14 | PR24B | 2 | RDQ22 | C (LVDS)* | PR34B | 2 | RDQ32 | C(LVDS)* |
| F13 | PR24A | 2 | RDQ22 | T (LVDS)* | PR34A | 2 | RDQ32 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H11 | PR14B | 2 | | C | PR14B | 2 | RDQ15 | C |
| G11 | PR14A | 2 | | T | PR14A | 2 | RDQ15 | T |
| E13 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C(LVDS)* |
| F12 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F11 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| E12 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| D16 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C(LVDS)* |
| D15 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| C16 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| B16 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F4 | XRES | - | | | XRES | - | | |
| C15 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A14 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B15 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B14 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C12 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A11 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A12 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B11 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C11 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B10 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C10 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A10 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C14 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B13 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C13 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A13 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B9 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| D8 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D9 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C9 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A5 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C5 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B5 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C4 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A8 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C8 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B8 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C7 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B7 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A6 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A21 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A22 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C21 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B19 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B18 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A19 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C18 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| D23 | PT73B | 1 | | C | PT82B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E21 | PT73A | 1 | | T | PT82A | 1 | | T |
| D26 | PT72B | 1 | | C | PT81B | 1 | | C |
| E26 | PT72A | 1 | | T | PT81A | 1 | | T |
| E23 | PT71B | 1 | | C | PT80B | 1 | | C |
| - | - | - | | | VCCIO1 | 1 | | |
| G22 | PT71A | 1 | | T | PT80A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | - | - | | |
| D22 | PT70B | 1 | | C | PT79B | 1 | | C |
| F21 | PT70A | 1 | | T | PT79A | 1 | | T |
| G18 | PT69B | 1 | | C | PT78B | 1 | | C |
| H18 | PT69A | 1 | | T | PT78A | 1 | | T |
| D20 | PT68B | 1 | | C | PT77B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| D21 | PT68A | 1 | | T | PT77A | 1 | | T |
| E20 | PT67B | 1 | | C | PT76B | 1 | | C |
| E19 | PT67A | 1 | | T | PT76A | 1 | | T |
| D19 | PT66B | 1 | | C | PT75B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E18 | PT66A | 1 | | T | PT75A | 1 | | T |
| D18 | PT65B | 1 | | C | PT74B | 1 | | C |
| C17 | PT65A | 1 | | T | PT74A | 1 | | T |
| A17 | PT64B | 1 | | C | PT73B | 1 | | C |
| B17 | PT64A | 1 | | T | PT73A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J18 | NC | - | | | PT66B | 1 | | C |
| J19 | NC | - | | | PT66A | 1 | | T |
| H17 | NC | - | | | PT65B | 1 | | C |
| J17 | NC | - | | | PT65A | 1 | | T |
| F18 | NC | - | | | PT64B | 1 | | C |
| F17 | NC | - | | | PT64A | 1 | | T |
| - | - | - | | | GNDIO1 | - | | |
| A16 | PT54B | 1 | | C | PT63B | 1 | | C |
| B16 | PT54A | 1 | | T | PT63A | 1 | | T |
| G17 | PT53B | 1 | | C | PT62B | 1 | | C |
| G16 | PT53A | 1 | | T | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H16 | PT52B | 1 | | C | PT61B | 1 | | C |
| F16 | PT52A | 1 | | T | PT61A | 1 | | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| E13 | PT28A | 0 | | T | PT37A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| J12 | PT5B | 0 | | C | PT31B | 0 | | C |
| GNDIO | GNDIO0 | - | | | - | - | | |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H10 | PT5A | 0 | | T | PT31A | 0 | | T |
| E12 | PT4B | 0 | | C | PT30B | 0 | | C |
| D11 | PT4A | 0 | | T | PT30A | 0 | | T |
| H11 | PT3B | 0 | | C | PT29B | 0 | | C |
| F11 | PT3A | 0 | | T | PT29A | 0 | | T |
| C13 | VCC | - | | | ULC_SQ_VCCRX0 | 11 | | |
| A12 | PT19A | 0 | | T | ULC_SQ_HDINP0 | 11 | | T |
| B13 | NC | - | | | ULC_SQ_VCCIB0 | 11 | | |
| B12 | PT19B | 0 | | C | ULC_SQ_HDINN0 | 11 | | C |
| C10 | VCC | - | | | ULC_SQ_VCCTX0 | 11 | | |
| A9 | PT17A | 0 | | T | ULC_SQ_HDOUTP0 | 11 | | T |
| A10 | NC | - | | | ULC_SQ_VCCOB0 | 11 | | |
| B9 | PT17B | 0 | | C | ULC_SQ_HDOUTN0 | 11 | | C |
| C9 | VCC | - | | | ULC_SQ_VCCTX1 | 11 | | |
| B8 | PT18B | 0 | | C | ULC_SQ_HDOUTN1 | 11 | | C |
| C8 | NC | - | | | ULC_SQ_VCCOB1 | 11 | | |
| A8 | PT18A | 0 | | T | ULC_SQ_HDOUTP1 | 11 | | T |
| C12 | VCC | - | | | ULC_SQ_VCCRX1 | 11 | | |
| B11 | PT16B | 0 | | C | ULC_SQ_HDINN1 | 11 | | C |
| C11 | NC | - | | | ULC_SQ_VCCIB1 | 11 | | |
| A11 | PT16A | 0 | | T | ULC_SQ_HDINP1 | 11 | | T |
| B7 | VCCAUX | - | | | ULC_SQ_VCCAUX33 | 11 | | |
| E7 | PT15B | 0 | | C | ULC_SQ_REFCLKN | 11 | | C |
| D7 | PT15A | 0 | | T | ULC_SQ_REFCLKP | 11 | | T |
| C7 | VCC | - | | | ULC_SQ_VCCP | 11 | | |
| A3 | PT12A | 0 | | T | ULC_SQ_HDINP2 | 11 | | T |
| C3 | NC | - | | | ULC_SQ_VCCIB2 | 11 | | |
| B3 | PT12B | 0 | | C | ULC_SQ_HDINN2 | 11 | | C |
| C2 | VCC | - | | | ULC_SQ_VCCRX2 | 11 | | |
| A6 | PT14A | 0 | | T | ULC_SQ_HDOUTP2 | 11 | | T |
| C6 | NC | - | | | ULC_SQ_VCCOB2 | 11 | | |
| B6 | PT14B | 0 | | C | ULC_SQ_HDOUTN2 | 11 | | C |
| C5 | VCC | - | | | ULC_SQ_VCCTX2 | 11 | | |
| B5 | PT13B | 0 | | C | ULC_SQ_HDOUTN3 | 11 | | C |
| A4 | NC | - | | | ULC_SQ_VCCOB3 | 11 | | |
| A5 | PT13A | 0 | | T | ULC_SQ_HDOUTP3 | 11 | | T |
| C4 | VCC | - | | | ULC_SQ_VCCTX3 | 11 | | |
| B2 | PT11B | 0 | | C | ULC_SQ_HDINN3 | 11 | | C |
| B1 | NC | - | | | ULC_SQ_VCCIB3 | 11 | | |
| A2 | PT11A | 0 | | T | ULC_SQ_HDINP3 | 11 | | T |
| C1 | VCC | - | | | ULC_SQ_VCCRX3 | 11 | | |
| L12 | VCC | - | | | VCC | - | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AA1 | PL81A | 6 | LDQS81 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AA2 | PL81B | 6 | LDQ81 | C (LVDS)* |
| Y3 | PL82A | 6 | LDQ81 | T |
| AB1 | PL82B | 6 | LDQ81 | C |
| VCCIO | VCCIO6 | 6 | | |
| Y9 | PL83A | 6 | LDQ81 | T (LVDS)* |
| Y8 | PL83B | 6 | LDQ81 | C (LVDS)* |
| Y7 | PL84A | 6 | LDQ81 | T |
| AA7 | PL84B | 6 | LDQ81 | C |
| GNDIO | GNDIO6 | - | | |
| VCCIO | VCCIO6 | 6 | | |
| AB2 | PL95A | 6 | LDQ99 | T (LVDS)* |
| AB3 | PL95B | 6 | LDQ99 | C (LVDS)* |
| AA5 | PL96A | 6 | LDQ99 | T |
| AA6 | PL96B | 6 | LDQ99 | C |
| AB4 | PL97A | 6 | LDQ99 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| AB5 | PL97B | 6 | LDQ99 | C (LVDS)* |
| AA8 | PL98A | 6 | LDQ99 | T |
| AA9 | PL98B | 6 | LDQ99 | C |
| AC1 | PL99A | 6 | LLM0_GPLLT_IN_A**/LDQS99 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AC2 | PL99B | 6 | LLM0_GPLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC4 | PL100A | 6 | LLM0_GPLLT_FB_A/LDQ99 | T |
| AC3 | PL100B | 6 | LLM0_GPLLC_FB_A/LDQ99 | C |
| VCCIO | VCCIO6 | 6 | | |
| AC7 | PL101A | 6 | LLM0_GDLLT_IN_A**/LDQ99 | T (LVDS)* |
| AC6 | PL101B | 6 | LLM0_GDLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC5 | PL102A | 6 | LLM0_GDLLT_FB_A/LDQ99 | T |
| AD3 | PL102B | 6 | LLM0_GDLLC_FB_A/LDQ99 | C |
| GNDIO | GNDIO6 | - | | |
| AB8 | LLM0_PLLCAP | 6 | | |
| AD2 | PL104A | 6 | | T |
| AD1 | PL104B | 6 | | C |
| AE2 | TCK | - | | |
| AE1 | TDI | - | | |
| AF2 | TMS | - | | |
| AF1 | TDO | - | | |
| AG1 | VCCJ | - | | |
| AH1 | LLC_SQ_VCCRX3 | 14 | | |
| AK2 | LLC_SQ_HDINP3 | 14 | | T |
| AJ1 | LLC_SQ_VCCIB3 | 14 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AG2 | PB34A | 5 | BDQ33 | T |
| AG3 | PB34B | 5 | BDQ33 | C |
| AD13 | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | |
| AC13 | PB35B | 5 | BDQ33 | C |
| AE14 | PB36A | 5 | BDQ33 | T |
| AC14 | PB36B | 5 | BDQ33 | C |
| AF3 | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | |
| AF4 | PB37B | 5 | BDQ33 | C |
| - | - | - | | |
| AG4 | PB38A | 5 | BDQ42 | T |
| AG5 | PB38B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AD11 | PB48A | 5 | BDQ51 | T |
| AF13 | PB48B | 5 | BDQ51 | C |
| AF12 | PB49A | 5 | BDQ51 | T |
| VCCIO | VCCIO5 | 5 | | |
| AD14 | PB49B | 5 | BDQ51 | C |
| AG8 | PB50A | 5 | BDQ51 | T |
| AF8 | PB50B | 5 | BDQ51 | C |
| AE15 | PB51A | 5 | BDQS51**** | T |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AC15 | PB51B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AD15 | PB56A | 5 | BDQ60 | T |
| AF15 | PB56B | 5 | BDQ60 | C |
| AG10 | PB57A | 5 | BDQ60 | T |
| AG9 | PB57B | 5 | BDQ60 | C |
| AH14 | PB58A | 5 | BDQ60 | T |
| AG12 | PB58B | 5 | BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | |
| AG15 | PB59A | 5 | BDQ60 | T |
| AG13 | PB59B | 5 | BDQ60 | C |
| GNDIO | GNDIO5 | - | | |
| AF16 | PB60A | 5 | BDQS60 | T |
| AH15 | PB60B | 5 | BDQ60 | C |
| AC16 | PB61A | 5 | VREF2_5/BDQ60 | T |
| AE16 | PB61B | 5 | VREF1_5/BDQ60 | C |
| AG11 | PB62A | 5 | PCLKT5_0/BDQ60 | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| M19 | VCC | - | | |
| M20 | VCC | - | | |
| N11 | VCC | - | | |
| N12 | VCC | - | | |
| N19 | VCC | - | | |
| N20 | VCC | - | | |
| P12 | VCC | - | | |
| P19 | VCC | - | | |
| R12 | VCC | - | | |
| R19 | VCC | - | | |
| T12 | VCC | - | | |
| T19 | VCC | - | | |
| U12 | VCC | - | | |
| U19 | VCC | - | | |
| V11 | VCC | - | | |
| V12 | VCC | - | | |
| V19 | VCC | - | | |
| V20 | VCC | - | | |
| W11 | VCC | - | | |
| W12 | VCC | - | | |
| W13 | VCC | - | | |
| W14 | VCC | - | | |
| W15 | VCC | - | | |
| W16 | VCC | - | | |
| W17 | VCC | - | | |
| W18 | VCC | - | | |
| W19 | VCC | - | | |
| W20 | VCC | - | | |
| Y12 | VCC | - | | |
| Y13 | VCC | - | | |
| Y18 | VCC | - | | |
| Y19 | VCC | - | | |
| D14 | VCCIO0 | 0 | | |
| E6 | VCCIO0 | 0 | | |
| E9 | VCCIO0 | 0 | | |
| F12 | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | |
| K13 | VCCIO0 | 0 | | |
| D17 | VCCIO1 | 1 | | |
| E22 | VCCIO1 | 1 | | |
| E25 | VCCIO1 | 1 | | |
| F19 | VCCIO1 | 1 | | |
| K18 | VCCIO1 | 1 | | |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AG23 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AK21 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AM19 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AM23 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC14 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AC15 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AG16 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AK14 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AM12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AM16 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA12 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AB8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AE3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AE7 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| AH3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W3 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W8 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y12 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| G3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| P12 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| R12 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T3 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T8 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AD28 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AG32 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AB12 | VCCAUX | - | | | VCCAUX | - | | |
| AB13 | VCCAUX | - | | | VCCAUX | - | | |
| AB22 | VCCAUX | - | | | VCCAUX | - | | |
| AB23 | VCCAUX | - | | | VCCAUX | - | | |
| AC13 | VCCAUX | - | | | VCCAUX | - | | |
| AC22 | VCCAUX | - | | | VCCAUX | - | | |
| M13 | VCCAUX | - | | | VCCAUX | - | | |
| M22 | VCCAUX | - | | | VCCAUX | - | | |
| N12 | VCCAUX | - | | | VCCAUX | - | | |
| N13 | VCCAUX | - | | | VCCAUX | - | | |
| N22 | VCCAUX | - | | | VCCAUX | - | | |
| N23 | VCCAUX | - | | | VCCAUX | - | | |
| A1 | GND | - | | | GND | - | | |
| A10 | GND | - | | | GND | - | | |
| A13 | GND | - | | | GND | - | | |
| A22 | GND | - | | | GND | - | | |
| A25 | GND | - | | | GND | - | | |
| A34 | GND | - | | | GND | - | | |

# LatticeECP2/M Family Data Sheet Ordering Information

July 2012 Data Sheet DS1006

## LatticeECP2 Part Number Description

LFE2 – XX XE – X XXXXXX X

**Device Family**
ECP2 (LatticeECP2 FPGA)

**Logic Capacity**
6 = 6K LUTs
12 = 12K LUTs
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs

**Encryption**
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

**Supply Voltage**
E = 1.2V

**Grade**
C = Commercial
I = Industrial

**Package**
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
TN144 = 144-pin Lead-Free TQFP
QN208 = 208-pin Lead-Free PQFP
FN256 = 256-ball Lead-Free fpBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN900 = 900-ball Lead-Free fpBGA

**Speed**
5 = Slowest
6
7 = Fastest

## Ordering Information

Note:þLatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:


| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35E-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | COM | 35 |
| LFE2-35E-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | COM | 35 |
| LFE2-35E-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | COM | 35 |
| LFE2-35E-5F672C | 450 | 1.2V | -5 | fpBGA | 672 | COM | 35 |
| LFE2-35E-6F672C | 450 | 1.2V | -6 | fpBGA | 672 | COM | 35 |
| LFE2-35E-7F672C | 450 | 1.2V | -7 | fpBGA | 672 | COM | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50E-5F484C | 339 | 1.2V | -5 | fpBGA | 484 | COM | 50 |
| LFE2-50E-6F484C | 339 | 1.2V | -6 | fpBGA | 484 | COM | 50 |
| LFE2-50E-7F484C | 339 | 1.2V | -7 | fpBGA | 484 | COM | 50 |
| LFE2-50E-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | COM | 50 |
| LFE2-50E-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | COM | 50 |
| LFE2-50E-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | COM | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70E-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | COM | 70 |
| LFE2-70E-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | COM | 70 |
| LFE2-70E-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | COM | 70 |
| LFE2-70E-5F900C | 583 | 1.2V | -5 | fpBGA | 900 | COM | 70 |
| LFE2-70E-6F900C | 583 | 1.2V | -6 | fpBGA | 900 | COM | 70 |
| LFE2-70E-7F900C | 583 | 1.2V | -7 | fpBGA | 900 | COM | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5T144I | 90 | 1.2V | -5 | TQFP | 144 | IND | 6 |
| LFE2-6E-6T144I | 90 | 1.2V | -6 | TQFP | 144 | IND | 6 |
| LFE2-6E-5F256I | 190 | 1.2V | -5 | fpBGA | 256 | IND | 6 |
| LFE2-6E-6F256I | 190 | 1.2V | -6 | fpBGA | 256 | IND | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5T144I | 93 | 1.2V | -5 | TQFP | 144 | IND | 12 |
| LFE2-12E-6T144I | 93 | 1.2V | -6 | TQFP | 144 | IND | 12 |
| LFE2-12E-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | IND | 12 |
| LFE2-12E-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | IND | 12 |
| LFE2-12E-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | IND | 12 |
| LFE2-12E-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | IND | 12 |
| LFE2-12E-5F484I | 297 | 1.2V | -5 | fpBGA | 484 | IND | 12 |
| LFE2-12E-6F484I | 297 | 1.2V | -6 | fpBGA | 484 | IND | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-35SE-5F484C | 331 | 1.2V | -5 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-6F484C | 331 | 1.2V | -6 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-7F484C | 331 | 1.2V | -7 | fpBGA | 484 | Com | 35 |
| LFE2-35SE-5F672C | 450 | 1.2V | -5 | fpBGA | 672 | Com | 35 |
| LFE2-35SE-6F672C | 450 | 1.2V | -6 | fpBGA | 672 | Com | 35 |
| LFE2-35SE-7F672C | 450 | 1.2V | -7 | fpBGA | 672 | Com | 35 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-50SE-5F484C | 339 | 1.2V | -5 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-6F484C | 339 | 1.2V | -6 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-7F484C | 339 | 1.2V | -7 | fpBGA | 484 | Com | 50 |
| LFE2-50SE-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | Com | 50 |
| LFE2-50SE-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | Com | 50 |
| LFE2-50SE-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | Com | 50 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-70SE-5F672C | 500 | 1.2V | -5 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-6F672C | 500 | 1.2V | -6 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-7F672C | 500 | 1.2V | -7 | fpBGA | 672 | Com | 70 |
| LFE2-70SE-5F900C | 583 | 1.2V | -5 | fpBGA | 900 | Com | 70 |
| LFE2-70SE-6F900C | 583 | 1.2V | -6 | fpBGA | 900 | Com | 70 |
| LFE2-70SE-7F900C | 583 | 1.2V | -7 | fpBGA | 900 | Com | 70 |

**Industrial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6SE-5T144I | 90 | 1.2V | -5 | TQFP | 144 | Ind | 6 |
| LFE2-6SE-6T144I | 90 | 1.2V | -6 | TQFP | 144 | Ind | 6 |
| LFE2-6SE-5F256I | 190 | 1.2V | -5 | fpBGA | 256 | Ind | 6 |
| LFE2-6SE-6F256I | 190 | 1.2V | -6 | fpBGA | 256 | Ind | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12SE-5T144I | 93 | 1.2V | -5 | TQFP | 144 | Ind | 12 |
| LFE2-12SE-6T144I | 93 | 1.2V | -6 | TQFP | 144 | Ind | 12 |
| LFE2-12SE-5Q208I | 131 | 1.2V | -5 | PQFP | 208 | Ind | 12 |
| LFE2-12SE-6Q208I | 131 | 1.2V | -6 | PQFP | 208 | Ind | 12 |
| LFE2-12SE-5F256I | 193 | 1.2V | -5 | fpBGA | 256 | Ind | 12 |
| LFE2-12SE-6F256I | 193 | 1.2V | -6 | fpBGA | 256 | Ind | 12 |
| LFE2-12SE-5F484I | 297 | 1.2V | -5 | fpBGA | 484 | Ind | 12 |
| LFE2-12SE-6F484I | 297 | 1.2V | -6 | fpBGA | 484 | Ind | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2M100SE-5FN1152C | 520 | 1.2V | -5 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-6FN1152C | 520 | 1.2V | -6 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-7FN1152C | 520 | 1.2V | -7 | Lead-Free fpBGA | 1152 | Com | 100 |
| LFE2M100SE-5FN900C | 416 | 1.2V | -5 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-6FN900C | 416 | 1.2V | -6 | Lead-Free fpBGA | 900 | Com | 100 |
| LFE2M100SE-7FN900C | 416 | 1.2V | -7 | Lead-Free fpBGA | 900 | Com | 100 |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| June 2013 (cont.) | 04.0 (cont.) | DC and Switching Characteristics | sysCLOCK SPLL Timing table – Corrected signal names for $t_{RST}$ parameter. |
| | | | LatticeECP2/M sysCONFIG Port Timing Specifications table – added $t_{SUMCDI}$ and $t_{HMCDI}$ parameters. |
| September 2013 | 04.1 | Architecture | Updated Selectable Master Clock (CCLK) Frequencies during Configuration table. |
| | | DC and Switching Characteristics | Added information on $f_{MAXSPI}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |