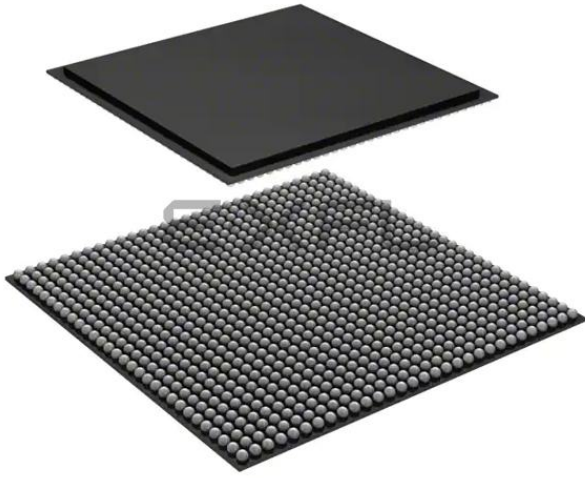




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8500
Number of Logic Elements/Cells	68000
Total RAM Bits	1056768
Number of I/O	583
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70e-5fn900c

Table 1-2. LatticeECP2M (Including “S-Series”) Family Selection

Device	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL+SPLL+DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Packages and SERDES / I/O Combinations					
256-ball fpBGA (17 x 17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23 x 23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27 x 27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31 x 31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35 x 35 mm)				16 / 436	16 / 520

Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

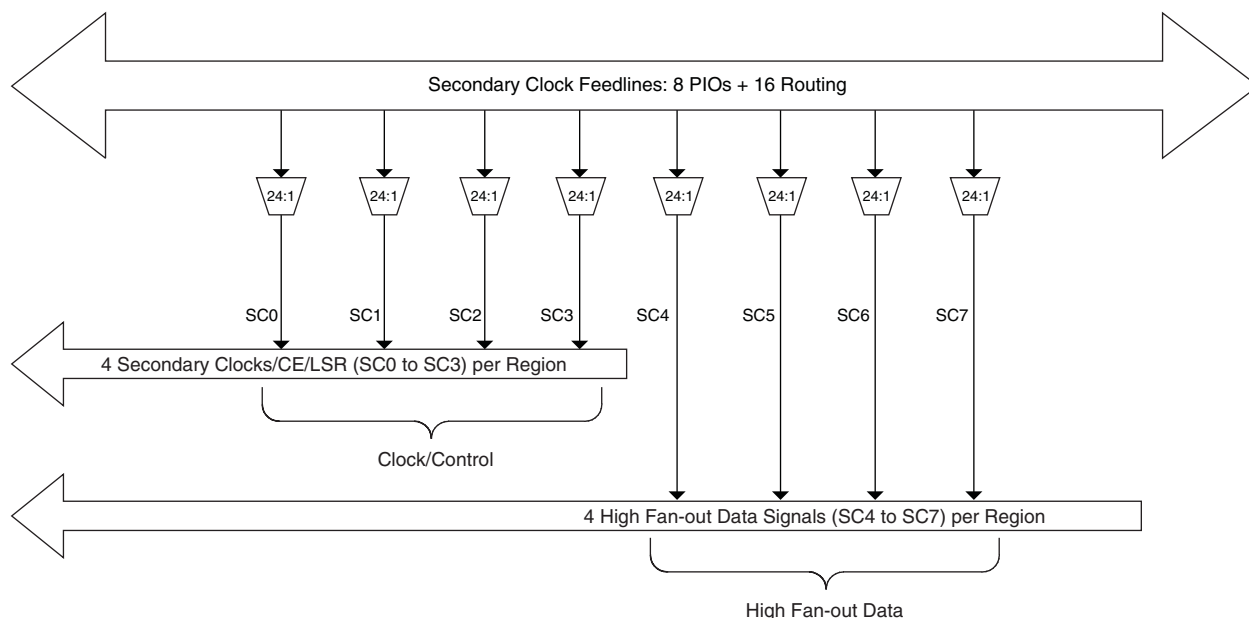
The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption (“S” versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-16. Secondary Clock Selection

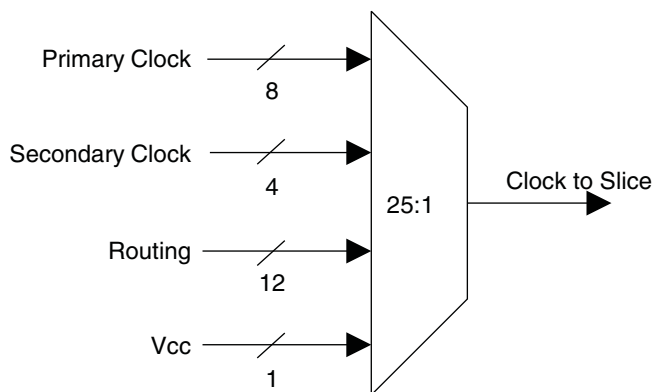


Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

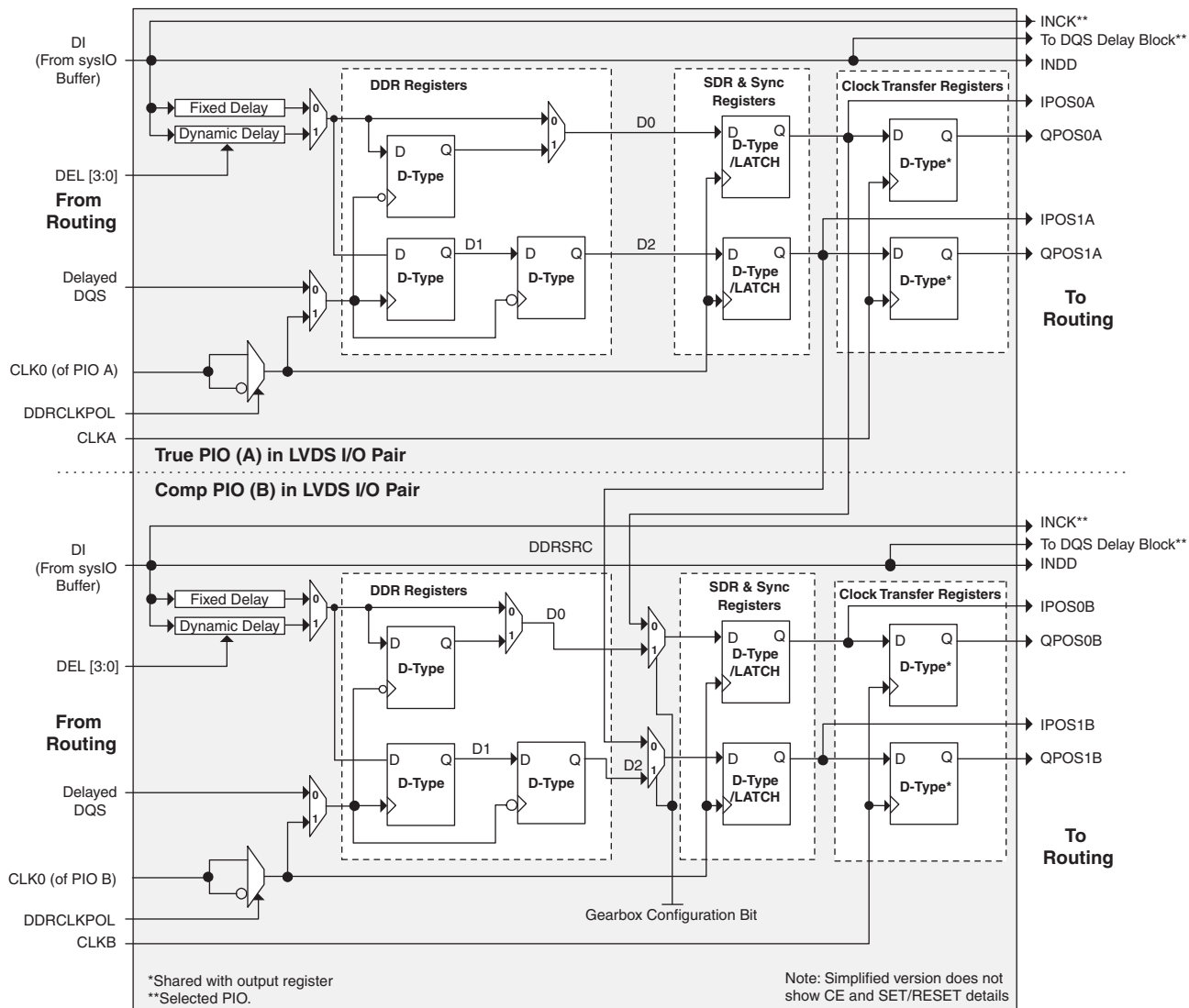
Figure 2-17. Slice0 through Slice2 Clock Selection



By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

Figure 2-29. Input Register Block for Left, Right and Bottom Edges



SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND ¹	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	LFE2M50: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 LFE2M70/LFE2M100: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC ²	LFE2M35: AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 LFE2M50: AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	LFE2M50: G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 LFE2M70/LFE2M100: AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
184	GND	-			GND	-			
185	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T	
186	PT26B	0		C	PT36B	0		C	
187	PT26A	0		T	PT36A	0		T	
188	VCC	-			VCC	-			
189	PT20B	0		C	PT30B	0		C	
190	VCCAUX	-			VCCAUX	-			
191	PT20A	0		T	PT30A	0		T	
192	GND	-			GND	-			
193	PT18B	0		C	PT26B	0		C	
194	PT18A	0		T	PT26A	0		T	
195	VCCIO0	0			VCCIO0	0			
196	PT16B	0		C	PT20B	0		C	
197	PT16A	0		T	PT20A	0		T	
198	VCC	-			VCC	-			
199	PT12B	0		C	PT12B	0		C	
200	PT12A	0		T	PT12A	0		T	
201	GND	-			GND	-			
202	PT8B	0		C	PT8B	0		C	
203	PT8A	0		T	PT8A	0		T	
204	PT6B	0		C	PT6B	0		C	
205	PT6A	0		T	PT6A	0		T	
206	VCCIO0	0			VCCIO0	0			
207	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
208	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J1	J1	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
K3	K3	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
J2	J2	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
GND	GND	GNDIO6	-		
L2	L2	PL38A	6	LDQ42	T (LVDS)*
K2	K2	PL39A	6	LDQ42	T
L3	L3	PL38B	6	LDQ42	C (LVDS)*
K1	K1	PL39B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
L4	L4	PL40A	6	LDQ42	T (LVDS)*
L1	L1	PL41A	6	LDQ42	T
L5	L5	PL40B	6	LDQ42	C (LVDS)*
M1	M1	PL41B	6	LDQ42	C
GND	GND	GNDIO6	-		
N1	N1	PL43A	6	LDQ42	T
N2	N2	PL42A	6	LDQS42	T (LVDS)*
P1	P1	PL43B	6	LDQ42	C
VCCIO	VCCIO	VCCIO6	6		
P2	P2	PL42B	6	LDQ42	C (LVDS)*
R1	R1	PL44A	6	LDQ42	T (LVDS)*
GND	GND	GNDIO6	-		
R2	R2	PL44B	6	LDQ42	C (LVDS)*
N4	N4	TDI	-		
M4	M4	TCK	-		
P3	P3	TDO	-		
N3	N3	TMS	-		
K7	K7	VCCJ	-		
M5	M5	PB2A	5	VREF2_5/BDQ6	T
K6	K6	PB3A	5	BDQ6	
M6	M6	PB2B	5	VREF1_5/BDQ6	C
R3	R3	PB5A	5	BDQ6	T
P4	P4	PB5B	5	BDQ6	C
-	VCC	VCCIO	5		
-	GND	GNDIO5	5		
N5	N5	PB30A	5	BDQ33	T
N6	N6	PB30B	5	BDQ33	C
T2	T2	PB31A	5	BDQ33	T
P6	P6	PB32A	5	BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
T3	T3	PB31B	5	BDQ33	C
R6	R6	PB32B	5	BDQ33	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		
V20	PROGRAMN	8			PROGRAMN	8		
W20	CFG0	8			CFG0	8		
U22	PR28B	8	D1	C	PR42B	8	D1	C
V22	INITN	8			INITN	8		
R16	PR30B	8	WRITEN	C	PR44B	8	WRITEN	C
GNDIO	GNDIO8	-			GNDIO8	-		
W22	CCLK	8			CCLK	8		
R17	PR30A	8	CS1N	T	PR44A	8	CS1N	T
V21	DONE	8			DONE	8		
VCCIO	VCCIO8	8			VCCIO8	8		
U19	PR29B	8	CSN	C	PR43B	8	CSN	C
T17	PR26B	8	D5	C	PR40B	8	D5	C
U20	PR29A	8	D0/SPIFASTN	T	PR43A	8	D0/SPIFASTN	T
U21	PR28A	8	D2	T	PR42A	8	D2	T
GNDIO	GNDIO8	-			GNDIO8	-		
T18	PR26A	8	D6	T	PR40A	8	D6	T
T20	PR27B	8	D3	C	PR41B	8	D3	C
T21	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
T19	PR27A	8	D4	T	PR41A	8	D4	T
VCCIO	VCCIO8	8			VCCIO8	8		
T22	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
R18	PR24B	8	DOUT/CSN	C	PR38B	8	DOUT/CSN	C
R19	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
-	-	-			VCCIO3	3		
GNDIO	GNDIO3	-			GNDIO3	-		
P18	PR22B	3		C (LVDS)*	PR32B	3	RDQ34	C (LVDS)*
R22	PR23B	3		C	PR33B	3	RDQ34	C
P19	PR22A	3		T (LVDS)*	PR32A	3	RDQ34	T (LVDS)*
R21	PR23A	3		T	PR33A	3	RDQ34	T
VCCIO	VCCIO3	3			VCCIO3	3		
R20	PR21B	3	RLM0_GPLL_C_FB_A	C	PR31B	3	RLM0_GPLL_C_FB_A/RDQ34	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
P21	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR18B	3	RLM0_GDLL_C_FB_A	C	PR28B	3	RLM0_GDLL_C_FB_A/RDQ25	C
M22	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLL_C_IN_A**/RDQ25	C (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
N19	NC	-			PR26B	3	RDQ25	C
-	-	-			VCCIO3	3		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GND	GNDIO5	-			GNDIO5	-			
W10	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
Y10	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AA10	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AC8	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD8	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AB8	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AB10	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AE6	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
AF6	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
AA11	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AC9	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AB9	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	
AD9	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y11	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AB11	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
AE7	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
AF7	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AC10	PB20A	5	BDQ24	T	PB20A	5	BDQ24	T	
AD10	PB20B	5	BDQ24	C	PB20B	5	BDQ24	C	
AA12	PB21A	5	BDQ24	T	PB21A	5	BDQ24	T	
W12	PB21B	5	BDQ24	C	PB21B	5	BDQ24	C	
AB12	PB22A	5	BDQ24	T	PB22A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
Y12	PB22B	5	BDQ24	C	PB22B	5	BDQ24	C	
AD12	PB23A	5	BDQ24	T	PB23A	5	BDQ24	T	
AC12	PB23B	5	BDQ24	C	PB23B	5	BDQ24	C	
AC13	PB24A	5	BDQS24	T	PB24A	5	BDQS24	T	
GND	GNDIO5	-			GNDIO5	-			
AA13	PB24B	5	BDQ24	C	PB24B	5	BDQ24	C	
AD13	PB25A	5	BDQ24	T	PB25A	5	BDQ24	T	
AC14	PB25B	5	BDQ24	C	PB25B	5	BDQ24	C	
AE8	PB26A	5	BDQ24	T	PB26A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB26B	5	BDQ24	C	PB26B	5	BDQ24	C	
AB15	PB27A	5	BDQ24	T	PB27A	5	BDQ24	T	
Y13	PB27B	5	BDQ24	C	PB27B	5	BDQ24	C	
AE9	PB28A	5	BDQ24	T	PB28A	5	BDQ24	T	
GND	GNDIO5	-			GNDIO5	-			
AF9	PB28B	5	BDQ24	C	PB28B	5	BDQ24	C	
W13	PB29A	5	BDQ33	T	PB29A	5	BDQ33	T	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO4	-			GNDIO4	-			
AA15	PB42B	4	BDQ42	C	PB60B	4	BDQ60	C	
V15	PB43A	4	BDQ42	T	PB61A	4	BDQ60	T	
U15	PB43B	4	BDQ42	C	PB61B	4	BDQ60	C	
AB16	PB44A	4	BDQ42	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AA16	PB44B	4	BDQ42	C	PB62B	4	BDQ60	C	
AB17	PB45A	4	BDQ42	T	PB63A	4	BDQ60	T	
AA17	PB45B	4	BDQ42	C	PB63B	4	BDQ60	C	
Y15	PB46A	4	BDQ42	T	PB64A	4	BDQ60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W15	PB46B	4	BDQ42	C	PB64B	4	BDQ60	C	
AB20	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T	
AB21	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C	
AA21	PB48A	4	BDQ51	T	PB66A	4	BDQ69	T	
AA20	PB48B	4	BDQ51	C	PB66B	4	BDQ69	C	
AB19	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T	
AB18	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y22	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T	
Y21	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y17	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T	
Y18	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C	
Y16	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T	
W17	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C	
Y19	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T	
Y20	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W19	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T	
W18	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C	
V17	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T	
V18	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W20	CFG2	8			CFG2	8			
V20	CFG1	8			CFG1	8			
V19	CFG0	8			CFG0	8			
V22	PROGRAMN	8			PROGRAMN	8			
W22	CCLK	8			CCLK	8			
U18	INITN	8			INITN	8			
U22	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
U20	PR53B	8	WRITEN***	C	PR68B	8	WRITEN***	C	
U21	PR53A	8	CS1N***	T	PR68A	8	CS1N***	T	
U17	PR52B	8	CSN***	C	PR67B	8	CSN***	C	
U16	PR52A	8	D0/SPIFASTN***	T	PR67A	8	D0/SPIFASTN***	T	
VCCIO	VCCIO8	8			VCCIO8	8			
T16	PR51B	8	D1***	C	PR66B	8	D1***	C	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T17	PR51A	8	D2***	T	PR66A	8	D2***	T	
T22	PR50B	8	D3***	C	PR65B	8	D3***	C	
GNDIO	GNDIO8	-			GNDIO8	-			
R22	PR50A	8	D4***	T	PR65A	8	D4***	T	
T15	PR49B	8	D5***	C	PR64B	8	D5***	C	
R17	PR49A	8	D6***	T	PR64A	8	D6***	T	
T20	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C	
VCCIO	VCCIO8	8			VCCIO8	8			
T21	PR48A	8	DI/CSSPI0N***	T	PR63A	8	DI/CSSPI0N***	T	
R21	PR47B	8	DOU/CSON/CSSPI1N***	C	PR62B	8	DOU/CSON/CSSPI1N***	C	
R20	PR47A	8	BUSY/SISPI***	T	PR62A	8	BUSY/SISPI***	T	
R16	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
R18	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C	
GNDIO	GNDIO3	-			GNDIO3	-			
R19	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T	
P22	PR44B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*	
P21	PR44A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*	
P16	PR43B	3	RLM0_GPLLC_IN_A**	C	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C	
VCCIO	VCCIO3	3			VCCIO3	3			
P17	PR43A	3	RLM0_GPLLT_IN_A**	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T	
P20	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C (LVDS)*	
P19	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57****	T (LVDS)*	
GNDIO	GNDIO3	-			GNDIO3	-			
-	-	-			VCCIO3	3			
P18	PR41B	3	RDQ38	C	PR51B	3	RDQ48	C	
N16	PR41A	3	RDQ38	T	PR51A	3	RDQ48	T	
GNDIO	GNDIO3	-			GNDIO3	-			
N22	PR40B	3	RDQ38	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*	
N21	PR40A	3	RDQ38	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*	
N17	PR39B	3	RDQ38	C	PR49B	3	RDQ48	C	
N18	PR39A	3	RDQ38	T	PR49A	3	RDQ48	T	
VCCIO	VCCIO3	3			VCCIO3	3			
M22	PR38B	3	RDQ38	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*	
M21	PR38A	3	RDQS38	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*	
M16	PR37B	3	RDQ38	C	PR47B	3	RDQ48	C	
GNDIO	GNDIO3	-			GNDIO3	-			
M17	PR37A	3	RDQ38	T	PR47A	3	RDQ48	T	
M20	PR36B	3	RDQ38	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*	
M19	PR36A	3	RDQ38	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*	
M18	PR35B	3	RDQ38	C	PR45B	3	RDQ48	C	
VCCIO	VCCIO3	3			VCCIO3	3			
L16	PR35A	3	RDQ38	T	PR45A	3	RDQ48	T	
L22	PR34B	3	RDQ38	C (LVDS)*	PR44B	3	RDQ48	C (LVDS)*	
L21	PR34A	3	RDQ38	T (LVDS)*	PR44A	3	RDQ48	T (LVDS)*	
K22	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C	
VCCIO	VCCIO3	3			VCCIO3	3			
K21	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T	
L17	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*	

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G5	VCCIO7	7		
J8	VCCIO7	7		
K4	VCCIO7	7		
AA22	VCCIO8	8		
U19	VCCIO8	8		
H11	VCCAUX	-		
H12	VCCAUX	-		
L15	VCCAUX	-		
L8	VCCAUX	-		
M15	VCCAUX	-		
M8	VCCAUX	-		
R11	VCCAUX	-		
R12	VCCAUX	-		
A1	GND	-		
A10	GND	-		
A16	GND	-		
A22	GND	-		
AA19	GND	-		
AA4	GND	-		
AB1	GND	-		
AB22	GND	-		
B13	GND	-		
B19	GND	-		
B4	GND	-		
D16	GND	-		
D2	GND	-		
D21	GND	-		
D7	GND	-		
G19	GND	-		
G4	GND	-		
H10	GND	-		
H13	GND	-		
J14	GND	-		
J9	GND	-		
K10	GND	-		
K11	GND	-		
K12	GND	-		
K13	GND	-		
K15	GND	-		
K20	GND	-		
K3	GND	-		
K8	GND	-		
L10	GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	GND	-		
L12	GND	-		
L13	GND	-		
M10	GND	-		
M11	GND	-		
M12	GND	-		
M13	GND	-		
N10	GND	-		
N11	GND	-		
N12	GND	-		
N13	GND	-		
N15	GND	-		
N20	GND	-		
N3	GND	-		
N8	GND	-		
P14	GND	-		
P9	GND	-		
R10	GND	-		
R13	GND	-		
T19	GND	-		
T4	GND	-		
W16	GND	-		
W2	GND	-		
W21	GND	-		
W7	GND	-		
Y10	GND	-		
Y13	GND	-		
Y15	NC	-		
W15	NC	-		
AB20	NC	-		
AB21	NC	-		
AA21	NC	-		
AA20	NC	-		
AB19	NC	-		
AB18	NC	-		
Y22	NC	-		
Y21	NC	-		
Y17	NC	-		
Y18	NC	-		
Y16	NC	-		
W17	NC	-		
Y19	NC	-		
Y20	NC	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
P8	PL45A	6	LDQ48	T	PL49A	6	LDQ52	T	
R6	PL45B	6	LDQ48	C	PL49B	6	LDQ52	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T1	PL46A	6	LDQ48	T (LVDS)*	PL50A	6	LDQ52	T*	
U1	PL46B	6	LDQ48	C (LVDS)*	PL50B	6	LDQ52	C*	
R7	PL47A	6	LDQ48	T	PL51A	6	LDQ52	T	
T5	PL47B	6	LDQ48	C	PL51B	6	LDQ52	C	
GNDIO	GNDIO6	-			GNDIO6	-			
U3	PL48A	6	LDQS48	T (LVDS)*	PL52A	6	LDQS52	T*	
U4	PL48B	6	LDQ48	C (LVDS)*	PL52B	6	LDQ52	C*	
U5	PL49A	6	LDQ48	T	PL53A	6	LDQ52	T	
VCCIO	VCCIO6	6			VCCIO6	6			
U6	PL49B	6	LDQ48	C	PL53B	6	LDQ52	C	
U2	PL50A	6	LDQ48	T (LVDS)*	PL54A	6	LDQ52	T*	
V1	PL50B	6	LDQ48	C (LVDS)*	PL54B	6	LDQ52	C*	
W2	PL51A	6	LDQ48	T	PL55A	6	LDQ52	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V2	PL51B	6	LDQ48	C	PL55B	6	LDQ52	C	
V4	PL55A	6	LDQ57	T (LVDS)*	PL59A	6		T*	
VCCIO	VCCIO6	6			VCCIO6	6			
V3	PL55B	6	LDQ57	C (LVDS)*	PL59B	6		C*	
-	-	-			GNDIO6	-			
W4	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	PL62A	6	LLM0_GPLLT_IN_A	T*	
GNDIO	GNDIO6	-			GNDIO6	-			
W3	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	PL62B	6	LLM0_GPLLC_IN_A	C*	
W1	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	PL63A	6	LLM0_GPLLT_FB_A	T	
Y1	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	PL63B	6	LLM0_GPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AA1	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*	PL64A	6	LLM0_GDLLT_IN_A	T*	
AB1	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	PL64B	6	LLM0_GDLLC_IN_A	C*	
U7	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T	PL65A	6	LLM0_GDLLT_FB_A	T	
V6	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	PL65B	6	LLM0_GDLLC_FB_A	C	
GNDIO	GNDIO6	-			GNDIO6	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
W5	PL62A	6	LDQ66	T (LVDS)*	PL67A	6	LDQ71	T*	
Y4	PL62B	6	LDQ66	C (LVDS)*	PL67B	6	LDQ71	C*	
U8	PL63A	6	LDQ66	T	PL68A	6	LDQ71	T	
W6	PL63B	6	LDQ66	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y3	PL64A	6	LDQ66	T (LVDS)*	PL69A	6	LDQ71	T*	
AA3	PL64B	6	LDQ66	C (LVDS)*	PL69B	6	LDQ71	C*	
V7	NC	-			PL70A	6	LDQ71	T	
Y5	PL65B	6	LDQ66	C	PL70B	6	LDQ71	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB2	PL66A	6	LDQS66	T (LVDS)*	PL71A	6	LDQS71	T*	
AA4	PL66B	6	LDQ66	C (LVDS)*	PL71B	6	LDQ71	C*	
Y6	PL67A	6	LDQ66	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E13	PT28A	0		T	PT37A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
GNDIO	GNDIO0	-			GNDIO0	-			
J12	PT5B	0		C	PT31B	0		C	
GNDIO	GNDIO0	-			-	-			
VCCIO	VCCIO0	0			VCCIO0	0			
H10	PT5A	0		T	PT31A	0		T	
E12	PT4B	0		C	PT30B	0		C	
D11	PT4A	0		T	PT30A	0		T	
H11	PT3B	0		C	PT29B	0		C	
F11	PT3A	0		T	PT29A	0		T	
C13	VCC	-			ULC_SQ_VCCR0	11			
A12	PT19A	0		T	ULC_SQ_HDINP0	11		T	
B13	NC	-			ULC_SQ_VCCIB0	11			
B12	PT19B	0		C	ULC_SQ_HDINN0	11		C	
C10	VCC	-			ULC_SQ_VCCTX0	11			
A9	PT17A	0		T	ULC_SQ_HDOUTP0	11		T	
A10	NC	-			ULC_SQ_VCCOB0	11			
B9	PT17B	0		C	ULC_SQ_HDOUTN0	11		C	
C9	VCC	-			ULC_SQ_VCCTX1	11			
B8	PT18B	0		C	ULC_SQ_HDOUTN1	11		C	
C8	NC	-			ULC_SQ_VCCOB1	11			
A8	PT18A	0		T	ULC_SQ_HDOUTP1	11		T	
C12	VCC	-			ULC_SQ_VCCR1	11			
B11	PT16B	0		C	ULC_SQ_HDINN1	11		C	
C11	NC	-			ULC_SQ_VCCIB1	11			
A11	PT16A	0		T	ULC_SQ_HDINP1	11		T	
B7	VCCAUX	-			ULC_SQ_VCCAUX33	11			
E7	PT15B	0		C	ULC_SQ_REFCLKN	11		C	
D7	PT15A	0		T	ULC_SQ_REFCLKP	11		T	
C7	VCC	-			ULC_SQ_VCCP	11			
A3	PT12A	0		T	ULC_SQ_HDINP2	11		T	
C3	NC	-			ULC_SQ_VCCIB2	11			
B3	PT12B	0		C	ULC_SQ_HDINN2	11		C	
C2	VCC	-			ULC_SQ_VCCR2	11			
A6	PT14A	0		T	ULC_SQ_HDOUTP2	11		T	
C6	NC	-			ULC_SQ_VCCOB2	11			
B6	PT14B	0		C	ULC_SQ_HDOUTN2	11		C	
C5	VCC	-			ULC_SQ_VCCTX2	11			
B5	PT13B	0		C	ULC_SQ_HDOUTN3	11		C	
A4	NC	-			ULC_SQ_VCCOB3	11			
A5	PT13A	0		T	ULC_SQ_HDOUTP3	11		T	
C4	VCC	-			ULC_SQ_VCCTX3	11			
B2	PT11B	0		C	ULC_SQ_HDINN3	11		C	
B1	NC	-			ULC_SQ_VCCIB3	11			
A2	PT11A	0		T	ULC_SQ_HDINP3	11		T	
C1	VCC	-			ULC_SQ_VCCR3	11			
L12	VCC	-			VCC	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M19	VCC	-		
M20	VCC	-		
N11	VCC	-		
N12	VCC	-		
N19	VCC	-		
N20	VCC	-		
P12	VCC	-		
P19	VCC	-		
R12	VCC	-		
R19	VCC	-		
T12	VCC	-		
T19	VCC	-		
U12	VCC	-		
U19	VCC	-		
V11	VCC	-		
V12	VCC	-		
V19	VCC	-		
V20	VCC	-		
W11	VCC	-		
W12	VCC	-		
W13	VCC	-		
W14	VCC	-		
W15	VCC	-		
W16	VCC	-		
W17	VCC	-		
W18	VCC	-		
W19	VCC	-		
W20	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
D14	VCCIO0	0		
E6	VCCIO0	0		
E9	VCCIO0	0		
F12	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
D17	VCCIO1	1		
E22	VCCIO1	1		
E25	VCCIO1	1		
F19	VCCIO1	1		
K18	VCCIO1	1		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO1	-			GNDIO1	-		
F19	PT59B	1		C	PT68B	1		C
D18	PT59A	1		T	PT68A	1		T
L18	NC	-			PT67B	1		C
K19	NC	-			PT67A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A18	PT57B	1	VREF2_1	C	PT66B	1	VREF2_1	C
B18	PT57A	1	VREF1_1	T	PT66A	1	VREF1_1	T
G18	PT56B	1	PCLKC1_0	C	PT65B	1	PCLKC1_0	C
E18	PT56A	1	PCLKT1_0	T	PT65A	1	PCLKT1_0	T
F18	PT55B	0	PCLKC0_0	C	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G19	PT55A	0	PCLKT0_0	T	PT64A	0	PCLKT0_0	T
H18	PT54B	0	VREF2_0	C	PT63B	0	VREF2_0	C
K18	PT54A	0	VREF1_0	T	PT63A	0	VREF1_0	T
VCCIO	VCCIO0	0			VCCIO0	0		
J18	PT53B	0		C	PT60B	0		C
L17	PT53A	0		T	PT60A	0		T
G17	PT52B	0		C	PT59B	0		C
-	-	-			GNDIO0	-		
J17	PT52A	0		T	PT59A	0		T
H17	PT51B	0		C	PT58B	0		C
-	-	-			VCCIO0	0		
K17	PT51A	0		T	PT58A	0		T
B17	PT50B	0		C	PT57B	0		C
GNDIO	GNDIO0	-			-	-		
A17	PT50A	0		T	PT57A	0		T
D17	PT49B	0		C	PT56B	0		C
VCCIO	VCCIO0	0			-	-		
F17	PT49A	0		T	PT56A	0		T
B16	PT48B	0		C	PT55B	0		C
A16	PT48A	0		T	PT55A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
E17	PT47B	0		C	PT52B	0		C
C17	PT47A	0		T	PT52A	0		T
K16	PT46B	0		C	PT51B	0		C
J15	PT46A	0		T	PT51A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
G16	PT45B	0		C	PT50B	0		C
H15	PT45A	0		T	PT50A	0		T
A15	PT44B	0		C	PT49B	0		C
B15	PT44A	0		T	PT49A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
L16	PT43B	0		C	PT48B	0		C
K15	PT43A	0		T	PT48A	0		T
F16	PT42B	0		C	PT47B	0		C
E16	PT42A	0		T	PT47A	0		T
E15	PT41B	0		C	PT46B	0		C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE12	NC	-			NC	-		
AE13	NC	-			NC	-		
AE19	NC	-			NC	-		
AE21	NC	-			NC	-		
AE22	NC	-			NC	-		
AE23	NC	-			NC	-		
AF11	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
AF24	NC	-			NC	-		
AF8	NC	-			NC	-		
AF9	NC	-			NC	-		
AG10	NC	-			NC	-		
AG11	NC	-			NC	-		
AG24	NC	-			NC	-		
AG25	NC	-			NC	-		
AG26	NC	-			NC	-		
AG3	NC	-			NC	-		
AG7	NC	-			NC	-		
AG8	NC	-			NC	-		
AG9	NC	-			NC	-		
AH10	NC	-			NC	-		
AH11	NC	-			NC	-		
AH13	NC	-			NC	-		
AH24	NC	-			NC	-		
AH25	NC	-			NC	-		
AH26	NC	-			NC	-		
AH27	NC	-			NC	-		
AH5	NC	-			NC	-		
AH6	NC	-			NC	-		
AH7	NC	-			NC	-		
AH8	NC	-			NC	-		
AH9	NC	-			NC	-		
AJ10	NC	-			NC	-		
AJ11	NC	-			NC	-		
AJ13	NC	-			NC	-		
AJ24	NC	-			NC	-		
AJ25	NC	-			NC	-		
AJ26	NC	-			NC	-		
AJ27	NC	-			NC	-		
AJ3	NC	-			NC	-		
AJ4	NC	-			NC	-		
AJ5	NC	-			NC	-		
AJ6	NC	-			NC	-		
AJ7	NC	-			NC	-		
AJ8	NC	-			NC	-		
AJ9	NC	-			NC	-		
AK10	NC	-			NC	-		
AK11	NC	-			NC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100