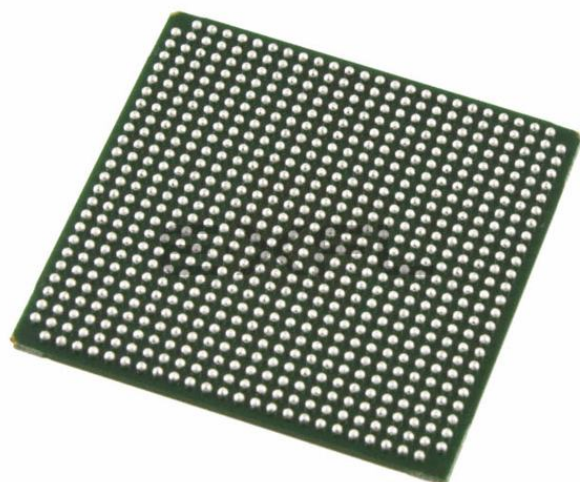




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8500
Number of Logic Elements/Cells	68000
Total RAM Bits	1056768
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70e-6f672i

Table 1-2. LatticeECP2M (Including “S-Series”) Family Selection

Device	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL+SPLL+DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Packages and SERDES / I/O Combinations					
256-ball fpBGA (17 x 17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23 x 23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27 x 27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31 x 31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35 x 35 mm)				16 / 436	16 / 520

Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

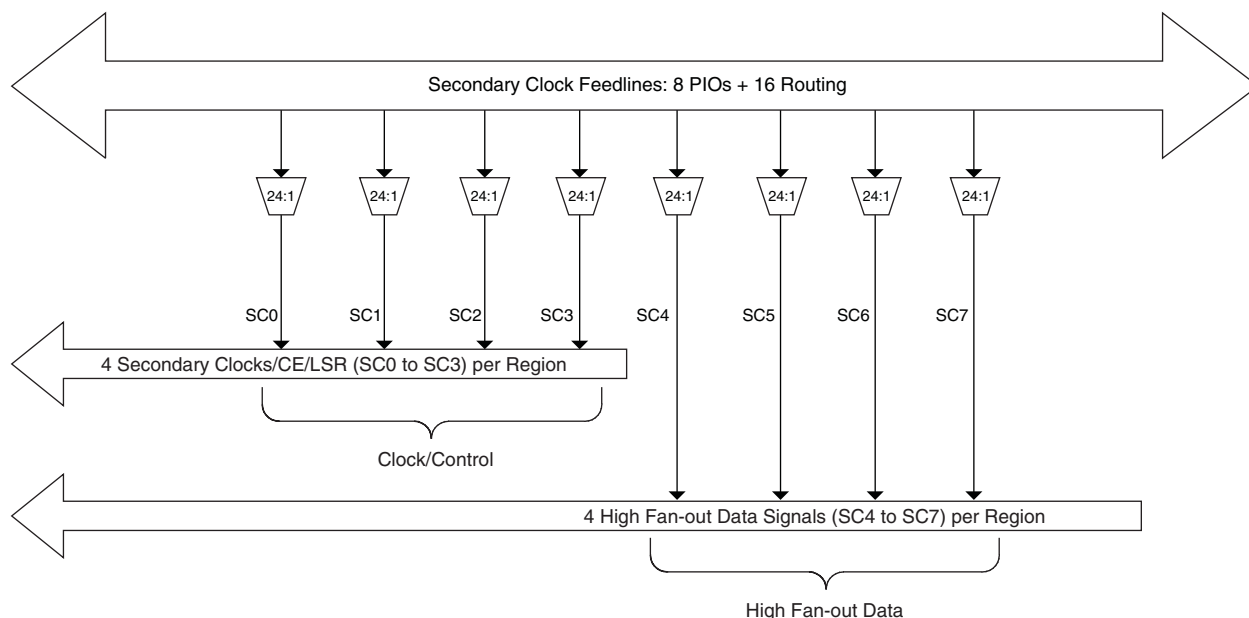
The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption (“S” versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The Diamond design tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-16. Secondary Clock Selection

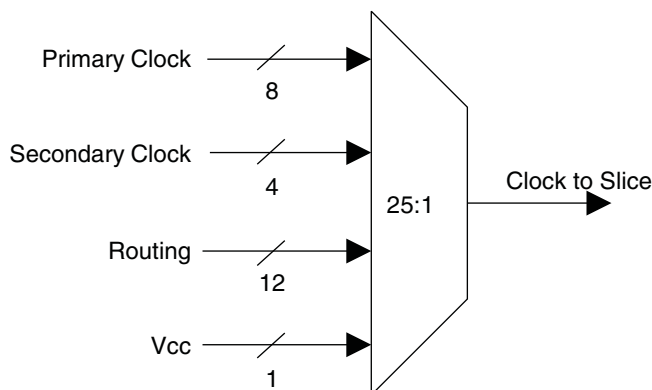


Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection



BLVDS

The LatticeECP2/M devices support the BLVDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

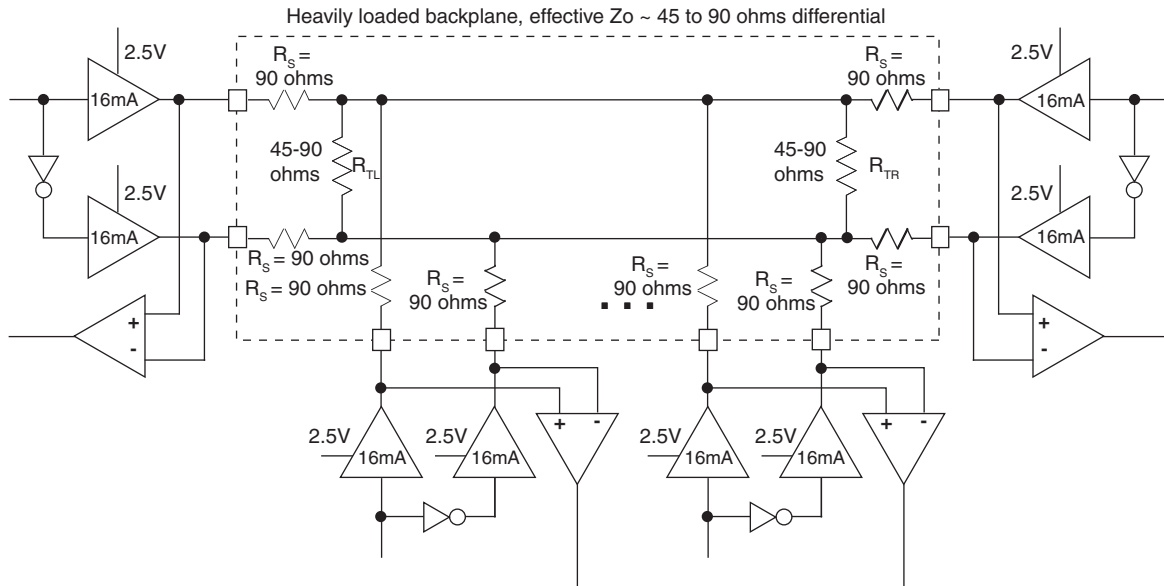


Table 3-3. BLVDS DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage	1.38	1.48	V
V _{OL}	Output Low Voltage	1.12	1.02	V
V _{OD}	Output Differential Voltage	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

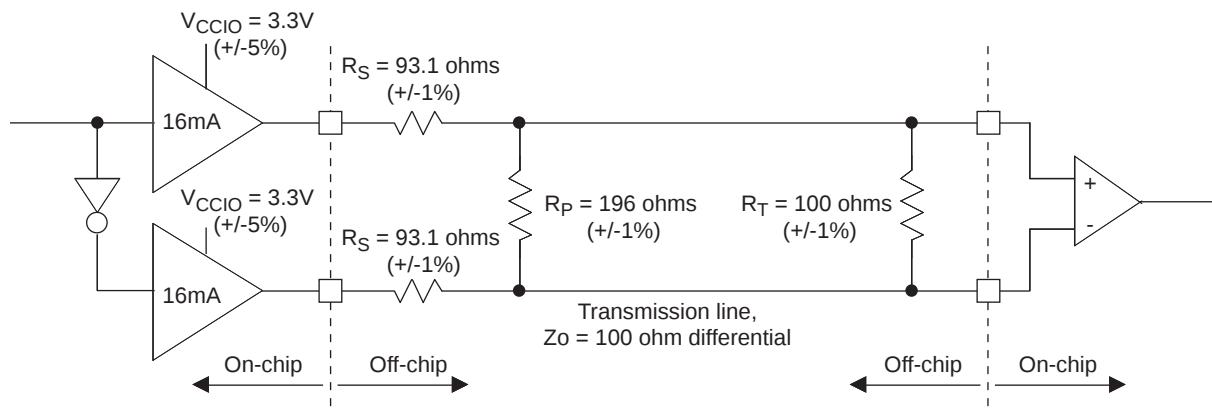


Table 3-4. LVPECL DC Conditions¹

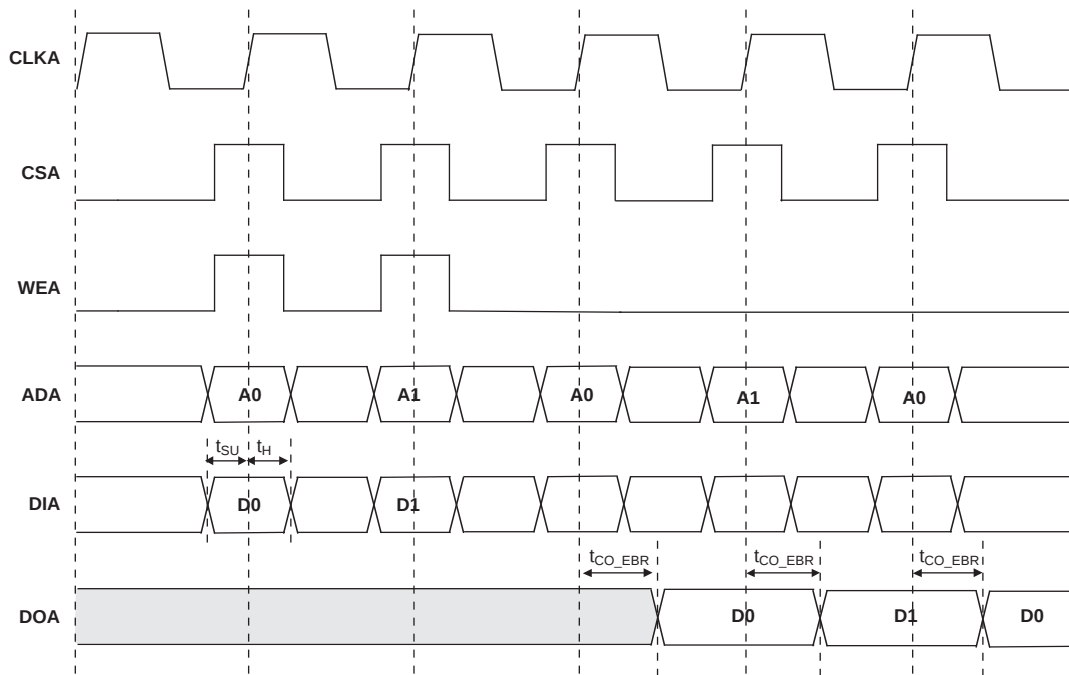
Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

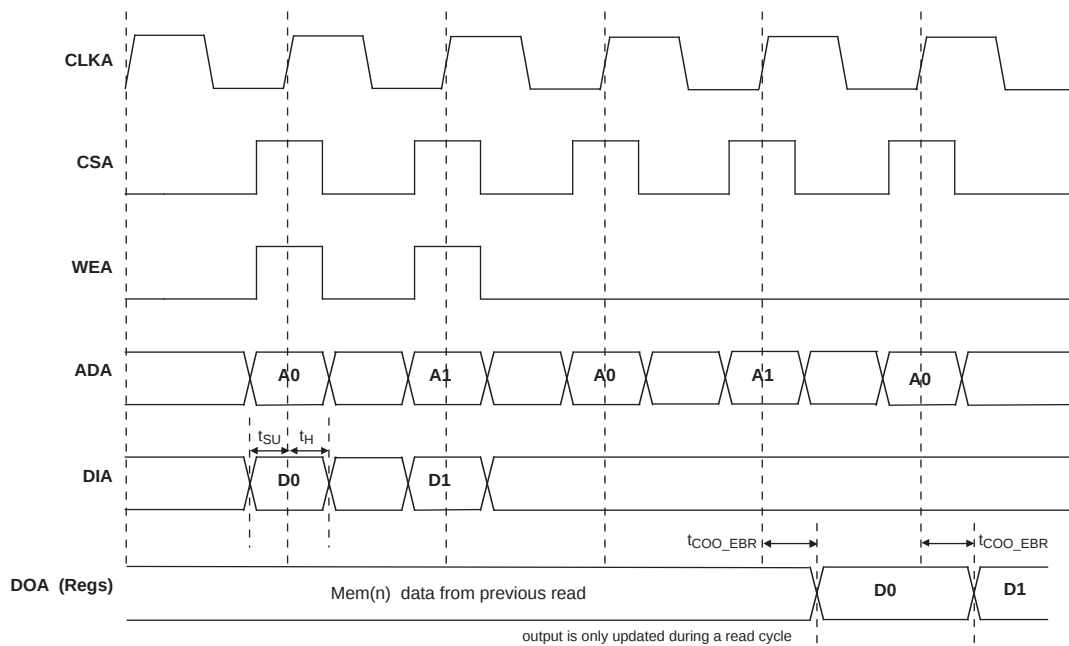
Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers



LatticeECP2/M Family Timing Adders^{1, 2, 3}

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.04	-0.02	0.00	ns
BLVDS25	BLVDS	-0.04	-0.09	-0.15	ns
MLVDS	LVDS	-0.15	-0.15	-0.15	ns
RSDS	RSDS	-0.15	-0.15	-0.15	ns
LVPECL33	LVPECL	0.16	0.15	0.13	ns
HSTL18_I	HSTL_18 class I	0.01	-0.01	-0.04	ns
HSTL18_II	HSTL_18 class II	0.01	-0.01	-0.04	ns
HSTL18D_I	Differential HSTL 18 class I	0.01	-0.01	-0.04	ns
HSTL18D_II	Differential HSTL 18 class II	0.01	-0.01	-0.04	ns
HSTL15_I	HSTL_15 class I	0.01	-0.01	-0.04	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	-0.01	-0.04	ns
SSTL33_I	SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33_II	SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL33D_I	Differential SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33D_II	Differential SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL25_I	SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25_II	SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25D_II	Differential SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL18_I	SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18_II	SSTL_18 class II	-0.01	-0.04	-0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18D_II	Differential SSTL_18 class II	-0.01	-0.04	-0.07	ns
LVTTTL33	LVTTTL	-0.16	-0.16	-0.16	ns
LVC MOS33	LVC MOS 3.3	-0.08	-0.12	-0.16	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	-0.16	-0.17	-0.17	ns
LVC MOS15	LVC MOS 1.5	-0.14	-0.14	-0.14	ns
LVC MOS12	LVC MOS 1.2	-0.04	-0.01	0.01	ns
PCI33	PCI	-0.08	-0.12	-0.16	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁴	0.25	0.19	0.13	ns
LVDS25	LVDS 2.5	0.10	0.13	0.17	ns
BLVDS25	BLVDS 2.5	0.00	-0.01	-0.03	ns
MLVDS	MLVDS 2.5 ⁴	0.00	-0.01	-0.03	ns
RSDS	RSDS 2.5 ⁴	0.25	0.19	0.13	ns
LVPECL33	LVPECL 3.3 ⁴	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18_II	HSTL_18 class II	-0.30	-0.34	-0.37	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.34	-0.37	ns

LatticeECP2M Power Supply and NC

Signal	256 fpBGA	484 fpBGA
V _{CC}	G7, G9, H7, J10, K10, K8	J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
V _{CCIO0}	E7	B5, B9, E7, H9
V _{CCIO1}	E10	D13, E16, H14
V _{CCIO2}	E14, G12	E21, G18, J15, K19
V _{CCIO3}	K12, M14	N19, P15, T18, V21
V _{CCIO4}	M10, P12	AA18, R14, V16, W13
V _{CCIO5}	M7, P5	AA5, R9, V7, W10
V _{CCIO6}	K5, M3	N4, P8, T5, V2
V _{CCIO7}	E3, G5	E2, G5, J8, K4
V _{CCIO8}	T15	AA22, U19
V _{CCJ}	K7	W4
V _{CCAUX}	G8, H10, J7, K9	H11, H12, L15, L8, M15, M8, R11, R12
V _{CCPLL}	G10	R8, H15, H8, R15
SERDES Power ³	C15, B15, C12, A12, C11, C10, C14, C13, B9, C9, C5, C4, C8, C7, A6, C6, B3, C3	C22, B22, C19, A19, C18, C17, C21, C20, B16, C16, C12, C11, C15, C14, A13, C13, B10, C10
GND ¹	A1, A15, A16, A3, A9, B12, B6, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A1, A10, A16, A22, AA19, AA4, AB1, AB22, B13, B19, B4, D16, D2, D21, D7, G19, G4, H10, H13, J14, J9, K10, K11, K12, K13, K15, K20, K3, K8, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, N15, N20, N3, N8, P14, P9, R10, R13, T19, T4, W16, W2, W21, W7, Y10, Y13
NC ²	D10, D11, D12, D13, D14, D4, D5, D6, D7, E11, E6, E8, E9, F10, F7, F8, F9	LFE2M20: D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15 LFE2M35: D14, D15, E14, E15, F13, F14, F15, G12, G13, G14, G15, U6 LFE2M50: Y15, W15, AB20, AB21, AA20, AB19, AB18, Y22, Y21, Y17, Y18, Y16, W17, Y19, Y20, W19, W18, V17, V18, D15, G14, G15, D14, E15, E14, F15, F14, F13, G12, G13

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N16	VCCIO3	3			VCCIO3	3		
P16	VCCIO3	3			VCCIO3	3		
R14	VCCIO4	4			VCCIO4	4		
T12	VCCIO4	4			VCCIO4	4		
T13	VCCIO4	4			VCCIO4	4		
T14	VCCIO4	4			VCCIO4	4		
R9	VCCIO5	5			VCCIO5	5		
T10	VCCIO5	5			VCCIO5	5		
T11	VCCIO5	5			VCCIO5	5		
T9	VCCIO5	5			VCCIO5	5		
N7	VCCIO6	6			VCCIO6	6		
P7	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K12	GND	-			GND	-		
K13	GND	-			GND	-		
K15	GND	-			GND	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
E27	NC	-		
E28	NC	-		
E29	NC	-		
E3	NC	-		
E30	NC	-		
E4	NC	-		
E5	NC	-		
E6	NC	-		
F25	NC	-		
F5	NC	-		
F6	NC	-		
G6	NC	-		
G7	NC	-		
K10	NC	-		
K9	NC	-		
N27	NC	-		
N4	NC	-		
R1	NC	-		
R2	NC	-		
V27	NC	-		
V4	NC	-		
P22	VCCPLL	-		
P8	VCCPLL	-		
T22	VCCPLL	-		
Y7	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO4	-			GNDIO4	-			
AA15	PB42B	4	BDQ42	C	PB60B	4	BDQ60	C	
V15	PB43A	4	BDQ42	T	PB61A	4	BDQ60	T	
U15	PB43B	4	BDQ42	C	PB61B	4	BDQ60	C	
AB16	PB44A	4	BDQ42	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AA16	PB44B	4	BDQ42	C	PB62B	4	BDQ60	C	
AB17	PB45A	4	BDQ42	T	PB63A	4	BDQ60	T	
AA17	PB45B	4	BDQ42	C	PB63B	4	BDQ60	C	
Y15	PB46A	4	BDQ42	T	PB64A	4	BDQ60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W15	PB46B	4	BDQ42	C	PB64B	4	BDQ60	C	
AB20	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T	
AB21	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C	
AA21	PB48A	4	BDQ51	T	PB66A	4	BDQ69	T	
AA20	PB48B	4	BDQ51	C	PB66B	4	BDQ69	C	
AB19	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T	
AB18	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y22	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T	
Y21	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y17	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T	
Y18	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C	
Y16	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T	
W17	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C	
Y19	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T	
Y20	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W19	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T	
W18	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C	
V17	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T	
V18	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W20	CFG2	8			CFG2	8			
V20	CFG1	8			CFG1	8			
V19	CFG0	8			CFG0	8			
V22	PROGRAMN	8			PROGRAMN	8			
W22	CCLK	8			CCLK	8			
U18	INITN	8			INITN	8			
U22	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
U20	PR53B	8	WRITEN***	C	PR68B	8	WRITEN***	C	
U21	PR53A	8	CS1N***	T	PR68A	8	CS1N***	T	
U17	PR52B	8	CSN***	C	PR67B	8	CSN***	C	
U16	PR52A	8	D0/SPIFASTN***	T	PR67A	8	D0/SPIFASTN***	T	
VCCIO	VCCIO8	8			VCCIO8	8			
T16	PR51B	8	D1***	C	PR66B	8	D1***	C	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
-	-	-			VCCIO5	5			
-	-	-			GNDIO5	-			
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T	
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C	
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T	
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C	
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C	
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T	
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C	
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C	
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T	
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C	
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C	
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T	
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C	
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T	
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C	
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T	
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C	
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T	
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C	
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T	
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C	
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T	
GNDIO	GNDIO4	-			GNDIO4	-			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C15	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B15	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C14	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A18	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C18	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B18	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C17	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B17	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A16	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A17	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T	
C16	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B14	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B13	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A14	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C13	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			
-	-	-			GNDIO1	-			
-	-	-			VCCIO1	1			
E17	PT46B	1		C	PT55B	1		C	
D17	PT46A	1		T	PT55A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
F17	PT45B	1		C	PT54B	1		C	
D16	PT45A	1		T	PT54A	1		T	
F19	PT44B	1		C	PT53B	1		C	
F18	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
E16	PT43B	1		C	PT52B	1		C	
D15	PT43A	1		T	PT52A	1		T	
G18	PT42B	1		C	PT51B	1		C	
E15	PT42A	1		T	PT51A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
G17	PT41B	1		C	PT50B	1		C	
E14	PT41A	1		T	PT50A	1		T	
D14	PT40B	1		C	PT49B	1		C	
D13	PT40A	1		T	PT49A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
F15	PT39B	1	VREF2_1	C	PT48B	1	VREF2_1	C	
E12	PT39A	1	VREF1_1	T	PT48A	1	VREF1_1	T	
H17	PT38B	1	PCLKC1_0	C	PT47B	1	PCLKC1_0	C	
E13	PT38A	1	PCLKT1_0	T	PT47A	1	PCLKT1_0	T	
C12	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
G15	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T	
C11	PT36B	0	VREF2_0	C	PT45B	0	VREF2_0	C	
F14	PT36A	0	VREF1_0	T	PT45A	0	VREF1_0	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
M26	PR27A	2	RDQS27	T (LVDS)*	PR37A	2	RDQS37	T (LVDS)*	
L30	PR26B	2	RDQ27	C	PR36B	2	RDQ37	C	
GNDIO	GNDIO2	-			GNDIO2	-			
L29	PR26A	2	RDQ27	T	PR36A	2	RDQ37	T	
L28	PR25B	2	RDQ27	C (LVDS)*	PR35B	2	RDQ37	C (LVDS)*	
L27	PR25A	2	RDQ27	T (LVDS)*	PR35A	2	RDQ37	T (LVDS)*	
H29	PR24B	2	RDQ27	C	PR34B	2	RDQ37	C	
VCCIO	VCCIO2	2			VCCIO2	2			
G29	PR24A	2	RDQ27	T	PR34A	2	RDQ37	T	
L22	PR23B	2	RDQ27	C (LVDS)*	PR33B	2	RDQ37	C (LVDS)*	
M22	PR23A	2	RDQ27	T (LVDS)*	PR33A	2	RDQ37	T (LVDS)*	
F30	PR21B	2		C	PR31B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
F29	PR21A	2		T	PR31A	2	RDQ28	T	
-	-	-			-	-			
-	-	-			-	-			
E30	PR20B	2		C (LVDS)*	PR30B	2	RDQ28	C (LVDS)*	
E29	PR20A	2		T (LVDS)*	PR30A	2	RDQ28	T (LVDS)*	
VCCIO	VCCIO2	2			-	-			
L25	PR19B	2		C	PR29B	2	RDQ28	C	
L26	PR19A	2		T	PR29A	2	RDQ28	T	
-	-	-			VCCIO2	2			
H28	PR18B	2		C (LVDS)*	PR28B	2	RDQ28	C (LVDS)*	
J28	PR18A	2		T (LVDS)*	PR28A	2	RDQS28	T (LVDS)*	
G28	PR16B	2		C	PR27B	2	RDQ28	C	
GNDIO	GNDIO2	-			GNDIO2	-			
G27	PR16A	2		T	PR27A	2	RDQ28	T	
L24	NC	-			PR26B	2	RDQ28	C (LVDS)*	
L23	NC	-			PR26A	2	RDQ28	T (LVDS)*	
D30	NC	-			PR25B	2	RDQ28	C	
-	-	-			VCCIO2	2			
D29	NC	-			PR25A	2	RDQ28	T	
K24	NC	-			PR24B	2	RDQ28	C (LVDS)*	
K25	NC	-			PR24A	2	RDQ28	T (LVDS)*	
J27	NC	-			PR22B	2		C	
-	-	-			GNDIO2	-			
K26	NC	-			PR22A	2		T	
K23	PR15B	2		C (LVDS)*	PR21B	2		C (LVDS)*	
K22	PR15A	2		T (LVDS)*	PR21A	2		T (LVDS)*	
J22	PR14B	2		C	PR20B	2		C	
VCCIO	VCCIO2	-			VCCIO2	2			
J23	PR14A	2		T	PR20A	2		T	
-	-	-			GNDIO2	-			
-	-	-			-	-			
J26	NC	-			PR17B	2	RDQ15	C (LVDS)*	
H26	NC	-			PR17A	2	RDQ15	T (LVDS)*	
H27	NC	-			PR16B	2	RDQ15	C	
G26	NC	-			PR16A	2	RDQ15	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF17	GND	-			GND	-			
AF25	GND	-			GND	-			
AF6	GND	-			GND	-			
AJ10	GND	-			GND	-			
AJ21	GND	-			GND	-			
AJ27	GND	-			GND	-			
AJ4	GND	-			GND	-			
AK1	GND	-			GND	-			
AK13	GND	-			GND	-			
AK18	GND	-			GND	-			
AK24	GND	-			GND	-			
AK30	GND	-			GND	-			
AK7	GND	-			GND	-			
B10	GND	-			GND	-			
B21	GND	-			GND	-			
B27	GND	-			GND	-			
B4	GND	-			GND	-			
D25	GND	-			GND	-			
D6	GND	-			GND	-			
E14	GND	-			GND	-			
E17	GND	-			GND	-			
F22	GND	-			GND	-			
F27	GND	-			GND	-			
F4	GND	-			GND	-			
F9	GND	-			GND	-			
G12	GND	-			GND	-			
G19	GND	-			GND	-			
J24	GND	-			GND	-			
J7	GND	-			GND	-			
K14	GND	-			GND	-			
K15	GND	-			GND	-			
K16	GND	-			GND	-			
K17	GND	-			GND	-			
K27	GND	-			GND	-			
K4	GND	-			GND	-			
L14	GND	-			GND	-			
L15	GND	-			GND	-			
L16	GND	-			GND	-			
L17	GND	-			GND	-			
M23	GND	-			GND	-			
M8	GND	-			GND	-			
N14	GND	-			GND	-			
N15	GND	-			GND	-			
N16	GND	-			GND	-			
N17	GND	-			GND	-			
N27	GND	-			GND	-			
N4	GND	-			GND	-			
P11	GND	-			GND	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D2	PL9A	7	VREF2_7	T
D3	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-		
J8	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
H7	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
E3	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
E4	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
G6	PL13A	7	LDQ15	T (LVDS)*
F5	PL13B	7	LDQ15	C (LVDS)*
E2	PL14A	7	LDQ15	T
D1	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-		
G5	PL15A	7	LDQS15	T (LVDS)*
G4	PL15B	7	LDQ15	C (LVDS)*
K7	PL16A	7	LDQ15	T
K8	PL16B	7	LDQ15	C
E1	PL17A	7	LDQ15	T (LVDS)*
F2	PL17B	7	LDQ15	C (LVDS)*
F1	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-		
G3	PL18B	7	LDQ15	C
GNDIO	GNDIO7	-		
H5	PL25A	7	LDQ23	T (LVDS)*
H4	PL25B	7	LDQ23	C (LVDS)*
J5	PL26A	7	LDQ23	T
J4	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-		
G2	PL28A	7	LDQ32	T (LVDS)*
G1	PL28B	7	LDQ32	C (LVDS)*
L9	PL29A	7	LDQ32	T
L7	PL29B	7	LDQ32	C
K6	PL30A	7	LDQ32	T (LVDS)*
K5	PL30B	7	LDQ32	C (LVDS)*
L8	PL31A	7	LDQ32	T
L6	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-		
H3	PL32A	7	LDQS32	T (LVDS)*
H2	PL32B	7	LDQ32	C (LVDS)*
N8	PL33A	7	LDQ32	T
M9	PL33B	7	LDQ32	C
J3	PL34A	7	LDQ32	T (LVDS)*
-	-	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AF11	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AJ14	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4		
AK14	PB67B	4	PCLKC4_0/BDQ69	C
AK15	PB68A	4	VREF2_4/BDQ69	T
AK16	PB68B	4	VREF1_4/BDQ69	C
AF18	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-		
AD16	PB69B	4	BDQ69	C
AJ15	PB70A	4	BDQ69	T
AG16	PB70B	4	BDQ69	C
AE17	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4		
AC17	PB71B	4	BDQ69	C
AH16	PB72A	4	BDQ69	T
AK17	PB72B	4	BDQ69	C
AG20	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-		
AG21	PB73B	4	BDQ69	C
AG18	PB74A	4	BDQ78	T
AJ16	PB74B	4	BDQ78	C
AF21	PB75A	4	BDQ78	T
AG22	PB75B	4	BDQ78	C
AD17	PB76A	4	BDQ78	T
AF19	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
AH17	PB80A	4	BDQ78	T
AJ17	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4		
AF26	PB82A	4	BDQ78	T
AE25	PB82B	4	BDQ78	C
GNDIO	GNDIO4	-		
AD24	PB92A	4	BDQ96	T
AE24	PB92B	4	BDQ96	C
AD18	PB93A	4	BDQ96	T
AC18	PB93B	4	BDQ96	C
AE18	PB94A	4	BDQ96	T
AG19	PB94B	4	BDQ96	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K26	PR26A	2	RDQ23	T
K23	PR25B	2	RDQ23	C (LVDS)*
K22	PR25A	2	RDQ23	T (LVDS)*
J22	PR24B	2	RDQ23	C
VCCIO	VCCIO2	2		
J23	PR24A	2	RDQ23	T
GNDIO	GNDIO2	-		
VCCIO	VCCIO2	2		
J26	PR17B	2	RDQ15	C (LVDS)*
H26	PR17A	2	RDQ15	T (LVDS)*
H27	PR16B	2	RDQ15	C
G26	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2		
H23	PR15B	2	RDQ15	C (LVDS)*
H24	PR15A	2	RDQS15	T (LVDS)*
D28	PR14B	2	RDQ15	C
GNDIO	GNDIO2	-		
E28	PR14A	2	RDQ15	T
G24	PR13B	2	RDQ15	C (LVDS)*
H25	PR13A	2	RDQ15	T (LVDS)*
D27	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
VCCIO	VCCIO2	2		
E27	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
F26	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*
G25	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
F24	PR9B	2	VREF2_2	C
-	-	-		
GNDIO	GNDIO2	-		
F25	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2		
G23	XRES	1		
C30	URC_SQ_VCCR0	12		
A29	URC_SQ_HDINP0	12		T
B30	URC_SQ_VCCIB0	12		
B29	URC_SQ_HDINN0	12		C
C27	URC_SQ_VCCTX0	12		
A26	URC_SQ_HDOUTP0	12		T
A27	URC_SQ_VCCOB0	12		
B26	URC_SQ_HDOUTN0	12		C
C26	URC_SQ_VCCTX1	12		
B25	URC_SQ_HDOUTN1	12		C
C25	URC_SQ_VCCOB1	12		
A25	URC_SQ_HDOUTP1	12		T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U22	GND	-			GND	-		
U23	GND	-			GND	-		
V12	GND	-			GND	-		
V13	GND	-			GND	-		
V15	GND	-			GND	-		
V16	GND	-			GND	-		
V17	GND	-			GND	-		
V18	GND	-			GND	-		
V19	GND	-			GND	-		
V20	GND	-			GND	-		
V22	GND	-			GND	-		
V23	GND	-			GND	-		
W12	GND	-			GND	-		
W13	GND	-			GND	-		
W15	GND	-			GND	-		
W16	GND	-			GND	-		
W17	GND	-			GND	-		
W18	GND	-			GND	-		
W19	GND	-			GND	-		
W20	GND	-			GND	-		
W22	GND	-			GND	-		
W23	GND	-			GND	-		
W26	GND	-			GND	-		
W31	GND	-			GND	-		
W4	GND	-			GND	-		
W9	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
Y18	GND	-			GND	-		
Y19	GND	-			GND	-		
A11	NC	-			NC	-		
A12	NC	-			NC	-		
A23	NC	-			NC	-		
A24	NC	-			NC	-		
AA11	NC	-			NC	-		
AB11	NC	-			NC	-		
AC26	NC	-			NC	-		
AC30	NC	-			NC	-		
AD11	NC	-			NC	-		
AD12	NC	-			NC	-		
AD13	NC	-			NC	-		
AD14	NC	-			NC	-		
AD15	NC	-			NC	-		
AD19	NC	-			NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD23	NC	-			NC	-		
AE10	NC	-			NC	-		
AE11	NC	-			NC	-		